Advance Information

The RF MOSFET Line

RF Power Field-Effect Transistors

N–Channel Enhancement Mode MOSFETs

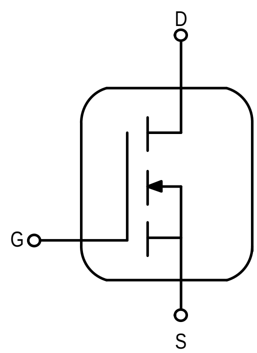
MRF156
MRF156R

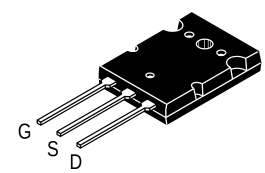
Motorola Preferred Device

Designed for broadband industrial/commercial applications up to 120 MHz. The high power, high gain and broadband performance of this device makes possible solid state transmitters including FM broadcast or TV transmitters. Reverse pin configurations make symmetrical push–pull designs possible.

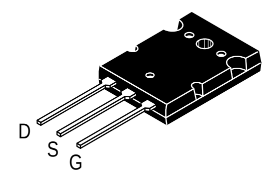
- Specified Characteristics 50 Volts, 30 MHz
- Output Power = 150 Watts
- Power Gain = 20 dB (Typ)
- Drain Efficiency = 50% (Typ)

**150 WATTS, 50 VOLTS
120 MHz, N–CHANNEL
BROADBAND
RF POWER MOSFET**





**MRF156
CASE 340G–02, STYLE 3
(TO–264AA)**



**MRF156R
CASE 340G–02, STYLE 4
(TO–264AA)**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	125	Vdc
Drain–Gate Voltage	V_{DGO}	125	Vdc
Gate–Source Voltage	V_{GS}	± 40	Vdc
Drain Current – Continuous	I_D	16	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.70	W W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	175	°C

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
THERMAL CHARACTERISTICS					
Thermal Resistance, Junction to Case	$R_{\theta JC}$	–	0.6	–	°C/W
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	125	–	–	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50, V, V_{GS} = 0)	I_{DSS}	–	–	5	mAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	–	–	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1	3	6	Vdc
Drain–Source ON–Voltage (V_{GS} = 10 V, I_D = 10 A)	$V_{DS(on)}$	1	3	5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 5 A)	g_{fs}	5	7	–	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	–	450	–	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	–	250	–	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	–	40	–	pF
FUNCTIONAL CHARACTERISTICS					
Common Source Power Gain (V_{DD} = 50 Vdc, P_{out} = 150 W, I_{DQ} = 250 mA, f = 30 MHz)	Gps	–	20	–	dB
Drain Efficiency (V_{DD} = 50 Vdc, P_{out} = 150 W, I_{DQ} = 250 mA, f = 30 MHz)	η	–	50	–	%

TYPICAL CHARACTERISTICS

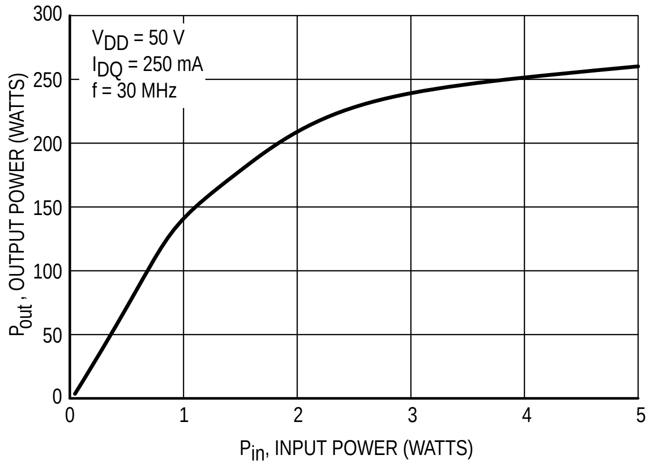


Figure 1. Output Power versus Input Power

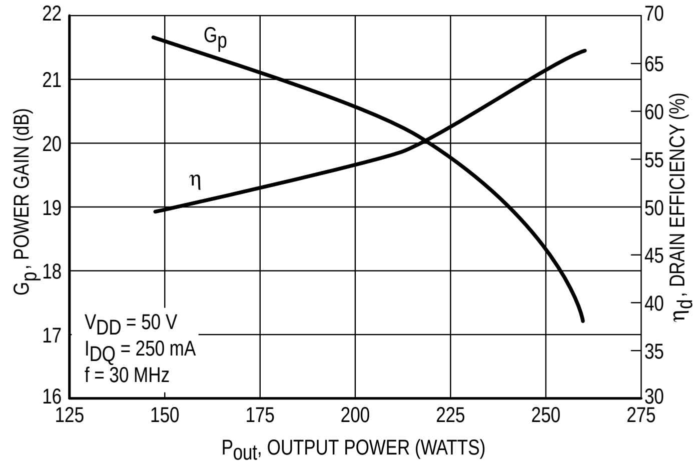


Figure 2. Power Gain and Efficiency versus Output Power

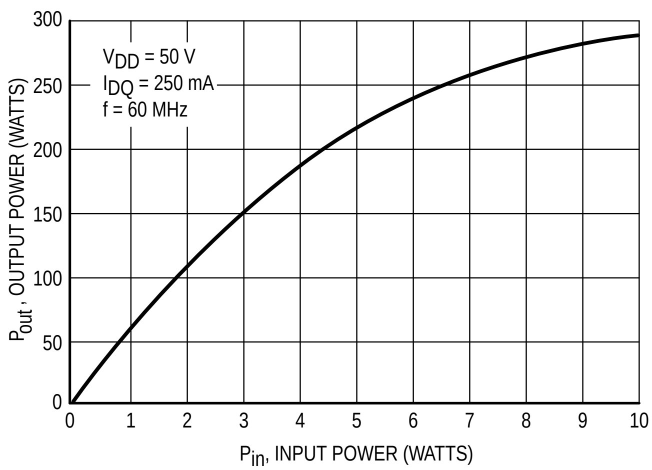


Figure 3. Output Power versus Input Power

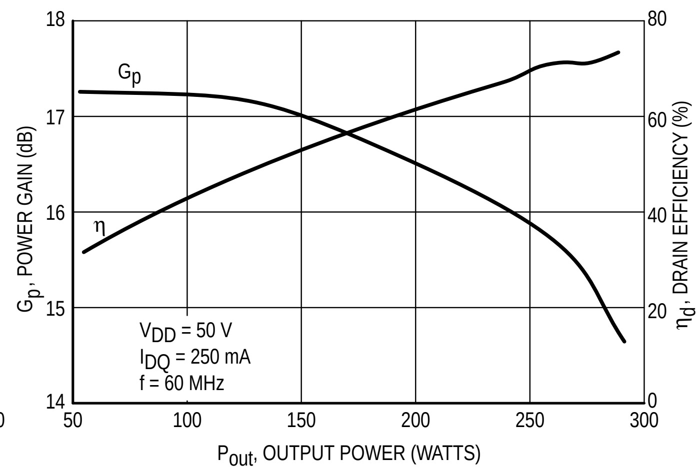


Figure 4. Power Gain and Efficiency versus Output Power

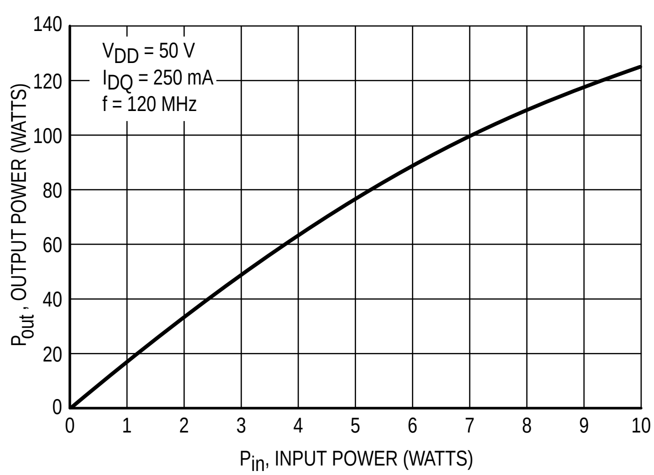


Figure 5. Output Power versus Input Power

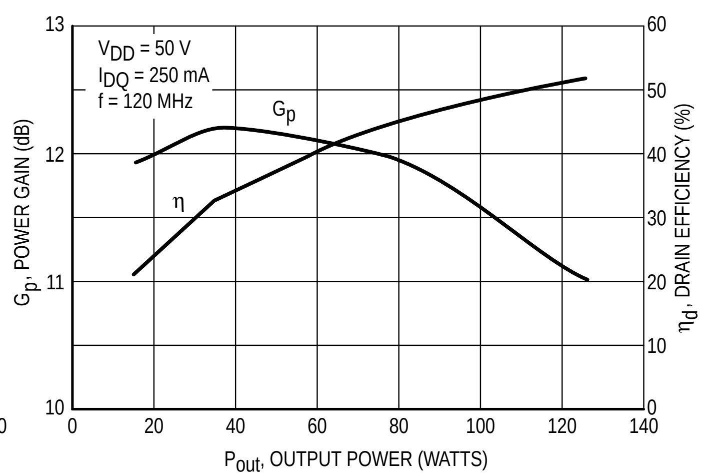


Figure 6. Power Gain and Drain Efficiency versus Output Power

TYPICAL CHARACTERISTICS

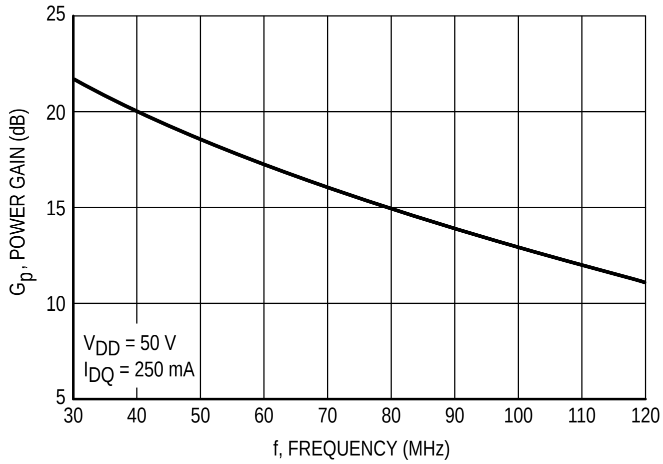


Figure 7. Power Gain versus Frequency

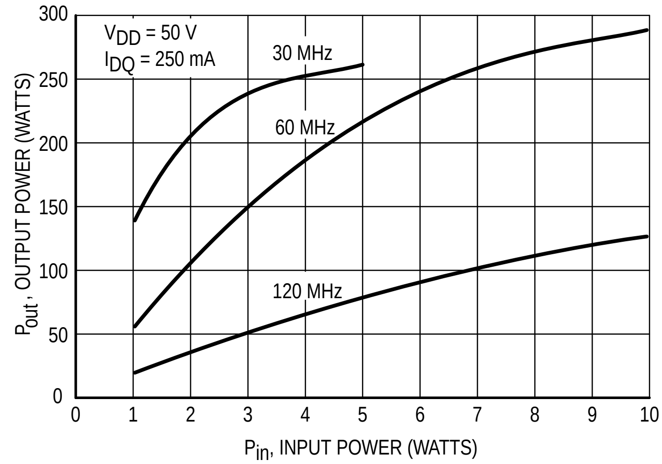
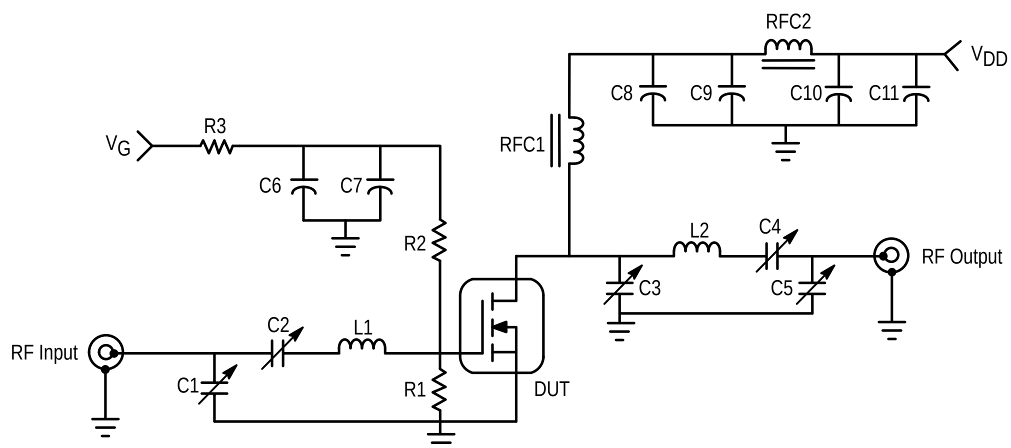
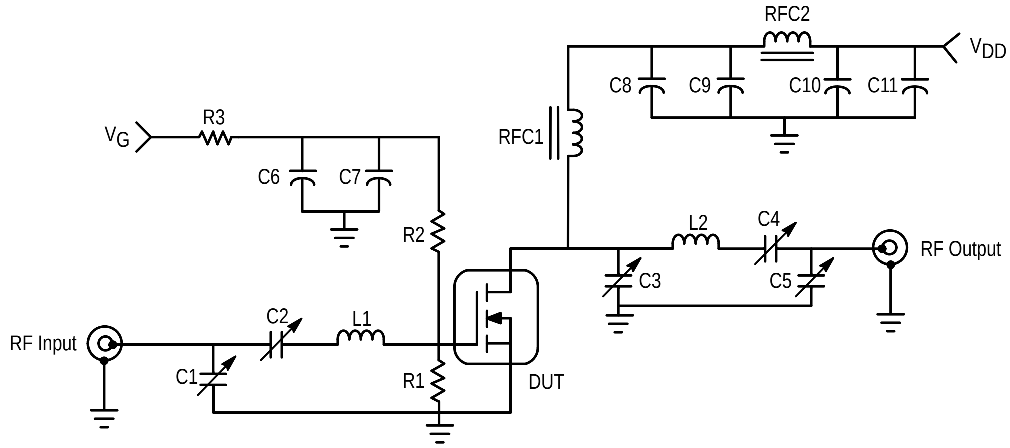


Figure 8. Output Power versus Input Power



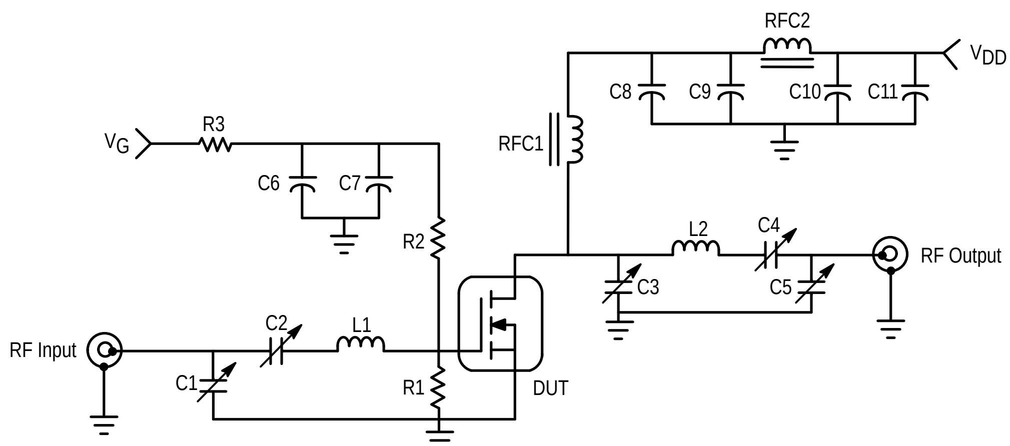
C1, C2, C3	170–780 pF, ARCO 469	L1	3 Turns, 3/8″ Diameter 18 AWG, Enamaled Copper Wire
C4, C5	80–480 pF, ARCO 466	L2	4 Turns, 9/16″ Diameter 12 AWG, Tin Copper Wire
C6, C7, C8	0.1 Chip Capacitor	R1, R2	100 Ω, 1 W
C9, C10	0.01 Ceramic Disk Capacitor	R3	51 Ω, 1 W
C11	10 μF, Electrolytic Capacitor	RFC1, RFC2	VK200 RF Choke

Figure 9. MRF156 30 MHz Test Fixture



C1	170–780 pF, ARCO 469	L1	1.5 Turns, 3/8″ Diameter 18 AWG, Enamaled Copper Wire
C2, C5	90–400 pF, ARCO 429	L2	2 Turns, 9/16″ Diameter 12 AWG, Tin Copper Wire
C3	70–350 pF, ARCO 428	R1, R2	100 Ω, 1 W
C4	80–480 pF, ARCO 466	R3	51 Ω, 1 W
C6, C7, C8	0.1 Chip Capacitor	RFC1, RFC2	VK200 RF Choke
C9, C10	0.01 Ceramic Disk Capacitor		
C11	10 µF, Electrolytic Capacitor		

Figure 10. MRF156 60 MHz Test Fixture



C1, C2, C5	25–280 pF, ARCO 464	L1	1 Turns, 3/8″ Diameter 18 AWG, Enamaled Copper Wire
C3, C4	80–480 pF, ARCO 466	L2	0.5 Turns, 9/16″ Diameter 12 AWG, Tin Copper Wire
C6, C7, C8	0.1 Chip Capacitor	R1, R2	100 Ω, 1 W
C9, C10	0.01 Ceramic Disk Capacitor	R3	51 Ω, 1 W
C11	10 µF, Electrolytic Capacitor	RFC1, RFC2	VK200 RF Choke

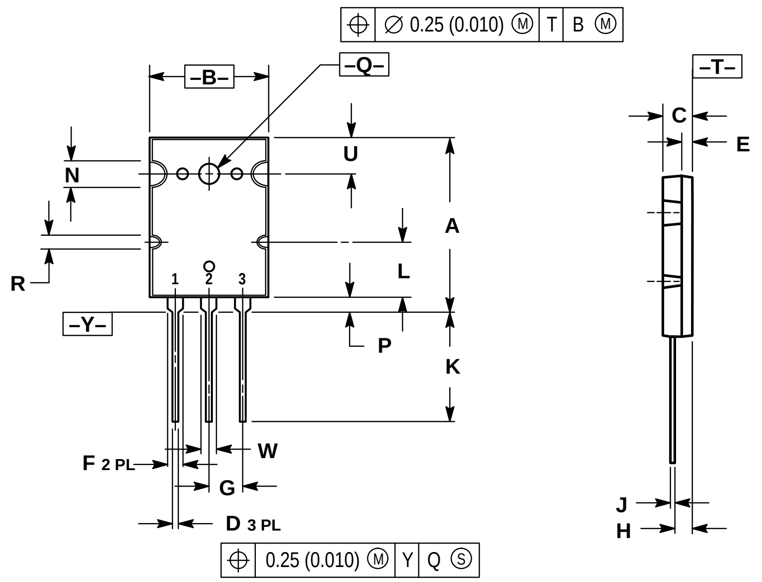
Figure 11. MRF156 120 MHz Test Fixture

Table 1. Large Signal Input/Ouput Impedance (P_{out} = 150 W PEP; V_{DD} = 50 V) I_{DQ} = 250 mA

Frequency (MHz)	Z_{in} Ω		Z_{out} Ω
30	1.83 – j3.23		3.85 + j0.99
60	2.06 – j1.29		4.15 + j1.10
120	4.22 + j2.20		4.42 + j1.18

Z_{out} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency. Gate shunted by 25 Ω.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.8	2.9	1.102	1.142
B	19.3	20.3	0.760	0.800
C	4.7	5.3	0.185	0.209
D	0.93	1.48	0.037	0.058
E	1.9	2.1	0.075	0.083
F	2.2	2.4	0.087	0.102
G	5.45 BSC		0.215 BSC	
H	2.6	3.0	0.102	0.118
J	0.43	0.78	0.017	0.031
K	17.6	18.8	0.693	0.740
L	11.0	11.4	0.433	0.449
N	3.95	4.75	0.156	0.187
P	2.2	2.6	0.087	0.102
Q	3.1	3.5	0.122	0.137
R	2.15	2.35	0.085	0.093
U	6.1	6.5	0.240	0.256
W	2.8	3.2	0.110	0.125

STYLE 3:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 4:
PIN 1. DRAIN
2. SOURCE
3. GATE

CASE 340G–02
ISSUE E
MRF156 (STYLE 3)
MRF156R (STYLE 4)

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