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PowerPC™

Advance Information

PowerPC 604™ RISC Microprocessor Hardware Specifications

The PowerPC 604 microprocessor is an implementation of the PowerPC™ family of reduced instruction set computer (RISC) microprocessors. This document contains pertinent physical characteristics of the 604.

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In this document, the term “604” is used as an abbreviation for the phrase, “PowerPC 604 microprocessor.” The PowerPC 604 microprocessors are available from IBM as PPC604 and from Motorola as MPC604.

IBM Microelectronics

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1.1 Overview

The 604 is an implementation of the PowerPC family of RISC microprocessors. The 604 implements the PowerPC Architecture™ specification as it is specified for 32-bit addressing, which provides 32-bit effective (logical) addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits (single-precision and double-precision).

The 604 is a superscalar processor capable of issuing four instructions simultaneously. As many as six instructions can finish execution in parallel. The 604 has six execution units that can operate in parallel:

- Floating-point unit (FPU)
- Branch processing unit (BPU)
- Load/store unit (LSU)
- Three integer units (IUs):
  - Two single-cycle integer units (SCIUs)
  - One multiple-cycle integer unit (MCIU)

This parallel design, combined with the PowerPC architecture's specification of uniform instructions that allow for rapid execution times, yields high efficiency and throughput. The 604's rename buffers, reservation stations, dynamic branch prediction, and completion unit increase instruction throughput, guarantee in-order completion, and ensure a precise exception model. (Note that the PowerPC architecture specification refers to all exceptions as interrupts.)

The 604 has separate memory management units (MMUs) and separate 16-Kbyte on-chip caches for instructions and data. The 604 implements two 128-entry, two-way set (64-entry per set) associative translation lookaside buffers (TLBs), one for instructions and one for data, and provides support for demand-paged virtual memory address translation and variable-sized block translation. The TLBs and the cache use least-recently used (LRU) replacement algorithms.

Multiprocessor applications are enabled by on-chip snooping logic which maintains data cache coherency. The 604 has a 64-bit external data bus and a 32-bit address bus. The 604 interface protocol allows multiple masters to compete for system resources through a central external arbiter. The 604 supports single-beat and burst data transfers for memory accesses and memory-mapped I/O accesses.

The 604 uses an advanced, 3.3-V CMOS process technology and is fully compatible with TTL devices.

1.1.1 Features

Major features of the 604 are as follows:

- High-performance, superscalar microprocessor
  - As many as four instructions issued per clock
  - As many as six instructions can be executing per clock (including three integer instructions)
  - Single clock cycle execution for most instructions
- Six independent execution units and two register files
  - BPU featuring dynamic branch prediction
    - Speculative execution through two branches
    - 64-entry fully-associative branch target address cache (BTAC)

  - 512-entry branch history table (BHT) with two bits per entry for four levels of prediction—not-taken, strongly not-taken, taken, strongly taken
- Two single-cycle IUs (SCIUs) and one multiple-cycle IU (MCIU)
  - Instructions that execute in the SCIU take one cycle to execute; most instructions that execute in the MCIU take multiple cycles to execute
  - Each SCIU has a two-entry reservation station to avoid stalls
  - The MCIU has a two-entry reservation station and provides early exit (three cycles) for 16- x 32-bit and overflow operations
  - Thirty-two GPRs for integer operands
- Three-stage floating-point unit (FPU)
  - Fully IEEE 754-1985 compliant FPU for both single- and double-precision operations
  - Supports non-IEEE mode for time-critical operations
  - Fully pipelined, single-pass double-precision design
  - Hardware support for denormalized numbers
  - Two-entry reservation station to minimize stalls
  - Thirty-two 64-bit FPRs for single- or double-precision operands
- Load/store unit (LSU)
  - Two-entry reservation station to minimize stalls
  - Single-cycle, pipelined cache access
  - Dedicated adder performs EA calculations
  - Performs alignment and precision conversion for floating-point data
  - Performs alignment and sign extension for integer data
  - Four-entry finish load queue (FLQ) provides load miss buffering
  - Six-entry store queue
  - Supports both big-endian and little-endian modes

- Rename buffers
  - Twelve GPR rename buffers
  - Eight FPR rename buffers
  - Eight condition register (CR) rename buffers
- Completion unit
  - Retires an instruction from the 16-entry reorder buffer when all instructions ahead of it have been completed and the instruction has finished execution
  - Guarantees sequential programming model (precise exception model)
  - Monitors all dispatched instructions and retires them in order
  - Tracks unresolved branches and removes speculatively executed, dispatched, and fetched instructions if branch is mispredicted
  - Retires as many as four instructions per clock

- Separate on-chip instruction and data caches (Harvard architecture)
  - 16-Kbyte, four-way set-associative instruction and data caches
  - LRU replacement algorithm
  - 32-byte (eight word) cache block size
  - Physically indexed; physical tags (note that the PowerPC architecture refers to physical address space as real address space)
  - Cache write-back or write-through operation programmable on a per page or per block basis
  - Instruction cache can provide four instructions per clock; data cache can provide two words per clock
  - Caches can be disabled in software
  - Caches can be locked
  - Parity checking performed on both caches
  - Data cache coherency (MESI) maintained in hardware
  - Secondary data cache support provided
  - Instruction cache coherency maintained in software
  - Provides a no-DRTRY/data streaming mode, which allows consecutive burst read data transfers to occur without intervening dead cycles. This mode also disables data retry operations.
- Separate memory management units (MMUs) for instructions and data
  - Address translation facilities for 4-Kbyte page size, variable block size, and 256-Mbyte segment size
  - Both TLBs are 128-entry and two-way set associative
  - TLBs are hardware reloadable
  - Separate IBATs and DBATs (four each) also defined as SPRs
  - Separate instruction and data translation lookaside buffers (ITLBs and DTLBs respectively)
  - LRU replacement algorithm
  - Hardware table search (caused by TLB misses) through hashed page tables
  - 52-bit virtual address; 32-bit physical address
- Bus interface features include the following:
  - Selectable processor-to-bus clock frequency ratios (1:1, 1.5:1, 2:1, and 3:1)
  - A 64-bit split-transaction external data bus with burst transfers
  - Support for address pipelining and limited out-of-order bus transactions
  - Additional signals and signal redefinition for direct-store operations
- Multiprocessing support features include the following:
  - Hardware enforced, four-state cache coherency protocol (MESI) for data cache. Bits in the instruction cache indicate whether a cache block is valid or invalid.
  - Separate port into data cache tags for bus snooping
  - Load/store with reservation instruction pair for atomic memory references, semaphores, and other multiprocessor operations

- Power management
  - — NAP mode supports full shut down and snooping
  - — Operating voltage of 3.3V ± 10%
- Performance monitor can be used to help in debugging system designs and improving software efficiency, especially in multiprocessor systems.
- In-system testability and debugging features through JTAG boundary-scan capability

1.2 General Parameters

Technology	0.5 µm CMOS, four-layer metal
Chip size	196 mm^2, 12.4 mm x 15.8 mm
Packages	Surface mount 304-pin wire-bond CQFP
	Surface mount 304-pin C4-CQFP
	Surface mount 255-lead ceramic ball grid array (BGA)
Voltage	3.3 V ± 5%
Maximum Power Dissipation	TBD

1.3 Electrical and Thermal Characteristics

This section provides both the AC and DC electrical specifications and thermal characteristics for the 604. The following specifications are preliminary and subject to change without notice. For the most recent specifications, contact your local Motorola or IBM sales office.

1.3.1 DC Electrical Characteristics

Table 1 and Table 2 provide the absolute maximum rating and thermal characteristics for the 604.

Table 1. PowerPC 604 Microprocessor Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Supply voltage	Vdd	–0.3 to 3.6	V
Input voltage	V_{in}	–0.3 to 5.5	V
Storage temperature range	T_{stg}	–55 to 150	°C

Notes:

1. Functional operating conditions are given in DC Electrical Specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** Input voltage must not be greater than the supply voltage by more than 2.5 V during power-on reset.

Table 2. PowerPC 604 Microprocessor Thermal Characteristics

Characteristic	Symbol	Value	Rating
Wire-bond CQFP package thermal resistance, junction to case	θ_{JC}	1.2	°C/W
C4-CQFP package thermal resistance, junction to case	θ_{JC}	0.03	°C/W
BGA package thermal resistance, junction to case	θ_{JC}	0.03	°C/W

Notes:
1. For the BGA package the θ_{JC} measurement is made from junction to the bare silicon die.
2. $T_j = T_A + P_D \times \theta_{JA}$, where $\theta_{JA} = \theta_{JC} + \theta_{CA}$.

Table 3 provides the DC electrical characteristics for the 604.

Table 3. PowerPC 604 Microprocessor DC Electrical Specifications

Vdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \le T_j \le 105$ °C, Input capacitance = 10 pF maximum

Characteristic	Symbol	Min	Max	Unit
Input high voltage (all inputs except SYSCLK)	V_{IH}	2	5.5	V
Input low voltage (all inputs except SYSCLK)	V_{IL}	0	0.8	V
SYSCLK input high voltage	CV_{IH}	2.4	5.5	V
SYSCLK input low voltage	CV_{IL}	0	0.4	V
Output high voltage, $I_{OH} = -9$ mA	V_{OH}	2.4	—	V
Output Low Voltage, $I_{OL} = 14$ mA	V_{OL}	—	0.4	V

Table 4 provides the power dissipation numbers for the 604.

Table 4. PowerPC 604 Microprocessor Power Dissipation

CPU Clock: SYSCLK		Bus Frequency (SYSCLK)					Unit
		25 MHz	33.3 MHz	40 MHz	50 MHz	66.7 MHz	
Full-On Mode							
1:1	Typical	TBD	TBD	TBD	TBD	TBD	W
	Max.	TBD	TBD	TBD	TBD	TBD	W
1.5:1	Typical	TBD	TBD	TBD	TBD	TBD	W
	Max.		TBD	TBD	TBD	TBD	W
2:1	Typical		TBD	TDB	TBD	TBD	W
	Max.	TBD	TBD	TBD	TBD	TBD	W
3:1	Typical	TBD	TBD	TBD			W
	Max.	TBD	TBD	TBD			W

Table 4. PowerPC 604 Microprocessor Power Dissipation

CPU Clock: SYSCLK	Bus Frequency (SYSCLK)					Unit
	25 MHz	33.3 MHz	40 MHz	50 MHz	66.7 MHz	
Nap Mode						
1:1 Typical	TBD	TBD	0.66	0.73	0.9	W
1.5:1 Typical		TBD	TBD	TBD	TBD	W
2:1 Typical	0.73	0.9	1.1	1.4	TBD	W
3:1 Typical	TBD	TBD	TBD			W

1.3.2 AC Electrical Characteristics

This section provides the clock AC electrical characteristics for the 604.

1.3.2.1 Input AC Specifications

Table 5 provides the clock AC timing specifications as defined in Figure 1. These specifications are for 25, 33.33, 40, 50, and 66.67 MHz bus clock (SYSCLK) frequencies. For 30MHz and 60 MHz bus clock frequencies, use the 33.33 and 66.67 MHz timings respectively.

Table 5. PowerPC 604 Microprocessor Clock AC Timing Specifications

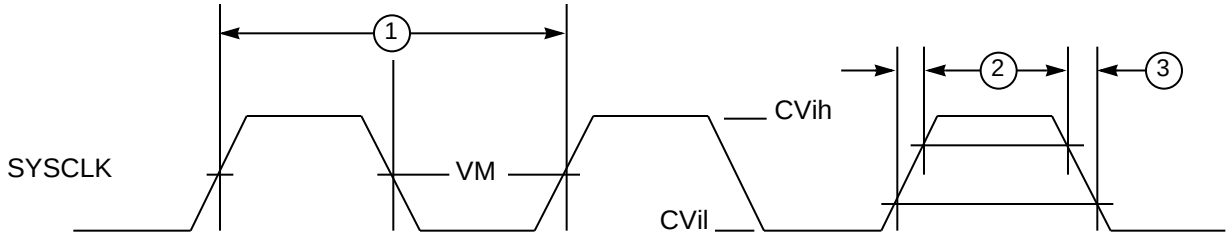
Vdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \le T_j \le 105$ °C

NUM	Characteristic	25 MHz		33.33 MHz		40 MHz		50 MHz		66.67 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
	Frequency of operation	20.0	25.0	25.0	33.33	33.33	40.0	40.0	50.0	50.0	66.67	MHz	
1	SYSCLK cycle time	40.0	50.0	30.0	40.0	25.0	30.0	20.0	25.0	15.0	20.0	ns	
2, 3	SYSCLK rise and fall time	1.0	2.0	1.0	2.0	1.0	2.0	1.0	2.0	1.0	2.0	ns	1
4	SYSCLK duty cycle measured at 1.5V	40.0	60.0	40.0	60.0	40.0	60.0	40.0	60.0	40.0	60.0	%	
5	SYSCLK short-term jitter (cycle-to-cycle)	—	±50	—	±50	—	±50	—	±50	—	±50	ps	
6	604 internal PLL relock time	—	100	—	100	—	100	—	100	—	100	µs	2, 3

Notes:

1. Rise and fall times for the SYSCLK input are measured from 0.4 V to 2.4 V.
2. During reset, the $\overline{\text{HRESET}}$ signal has to be held for stated relock time for the PLL to achieve a lock.
3. Relock timing is guaranteed by design and is not tested.

Figure 1 provides the SYSCLK input timing diagram.



VM = Midpoint Voltage (1.4 V)

Figure 1. SYSCLK Input Timing Diagram

Table 6 provides the input AC timing specifications for the 604 as defined in Figure 2. These specifications are for 25, 33.33, 40, 50, and 66.67 MHz bus clock (SYSCLK) frequencies. For 30 MHz and 60 MHz bus clock frequencies, use the 33.33 MHz and 66.67 MHz timings respectively.

Table 6. PowerPC 604 Microprocessor Input AC Timing Specifications

Vdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \le T_j \le 105$ °C

NUM	Characteristic	25 MHz		33.33 MHz		40 MHz		50 MHz		66.67 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
10	$\overline{\text{ARTRY}}$ valid to SYSCLK (setup)	7.5	—	6.5	—	6.0	—	5.0	—	4.5	—	ns	
11	$\overline{\text{TS}}$, $\overline{\text{XATS}}$, valid to SYSCLK (setup)	7.5	—	6.5	—	6.0	—	5.0	—	4.5	—	ns	
12	$\overline{\text{ABB}}$ valid to SYSCLK (setup)	7.5	—	6.5	—	6.0	—	5.0	—	4.5	—	ns	
13	$\overline{\text{SHD}}$ valid to SYSCLK (setup)	7.5	—	6.5	—	6.0	—	5.0	—	4.5	—	ns	
14	$\overline{\text{AACK}}$, $\overline{\text{BG}}$ valid to SYSCLK (setup)	7.5	—	6.5	—	6.0	—	5.0	—	4.5	—	ns	
15	SYSCLK to $\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{TS}}$, $\overline{\text{XATS}}$, $\overline{\text{AACK}}$, and $\overline{\text{BG}}$ invalid (hold)	0	—	0	—	0	—	0	—	0	—	ns	
16	$\overline{\text{DRTRY}}$ valid to SYSCLK (setup)	7.5	—	6.5	—	6.0	—	5.0	—	4.5	—	ns	
17	$\overline{\text{TA}}$ valid to SYSCLK (setup)	7.5	—	6.5	—	6.0	—	5.0	—	4.5	—	ns	
18	$\overline{\text{DBWO}}$ valid to SYSCLK (setup)	7.5	—	6.5	—	6.0	—	5.0	—	4.5	—	ns	
19	$\overline{\text{DBG}}$ and $\overline{\text{DBB}}$ valid to SYSCLK (setup)	7.5	—	6.5	—	6.0	—	5.0	—	4.5	—	ns	
20	$\overline{\text{TEA}}$ and $\overline{\text{DBDIS}}$ valid to SYSCLK (setup)	7.5	—	6.5	—	6.0	—	5.0	—	4.5	—	ns	

Table 6. PowerPC 604 Microprocessor Input AC Timing Specifications (Continued)

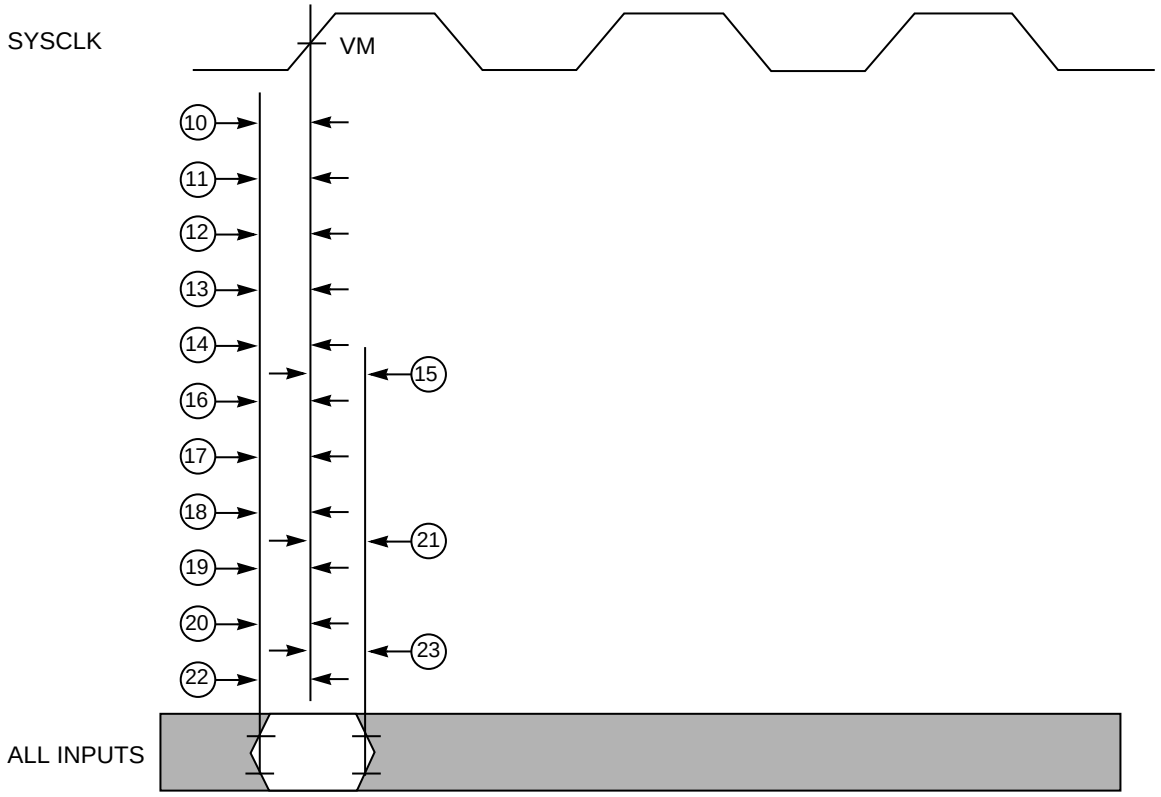
Vdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \le T_j \le 105$ °C

NUM	Characteristic	25 MHz		33.33 MHz		40 MHz		50 MHz		66.67 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
21	SYSCLK to $\overline{\text{DRTRY}}$, $\overline{\text{TA}}$, $\overline{\text{DBG}}$, $\overline{\text{DBB}}$, $\overline{\text{TEA}}$, $\overline{\text{DBDIS}}$, and $\overline{\text{DBWO}}$ invalid (hold)	0	—	0	—	0	—	0	—	0	—	ns	
22	All other inputs valid to SYSCLK (setup)	6.5	—	5.5	—	5.0	—	4.0	—	3.5	—	ns	1
23	SYSCLK to all other inputs invalid (hold)	0	—	0	—	0	—	0	—	0	—	ns	1
24	Mode select input valid to $\overline{\text{HRESET}}$ (input setup) (for $\overline{\text{DRTRY}}$)	8 * t_{sysclk}	—	8 * t_{sysclk}	—	8 * t_{sysclk}	—	8 * t_{sysclk}	—	8 * t_{sysclk}	—	ns	2,3, 4,5
25	$\overline{\text{HRESET}}$ to mode select input invalid (input hold) (for $\overline{\text{DRTRY}}$)	0	—	0	—	0	—	0	—	0	—	ns	2,3, 4,5

Notes:

1. All other input signals include the following signals—all inputs except $\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{TS}}$, $\overline{\text{XATS}}$, $\overline{\text{AACK}}$, $\overline{\text{BG}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TA}}$, $\overline{\text{DBG}}$, $\overline{\text{DBB}}$, $\overline{\text{DBWO}}$, $\overline{\text{DBDIS}}$, $\overline{\text{TEA}}$, and JTAG inputs.
2. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$. See Figure 3.
3. t_{sysclk} is the period of the external clock (SYSCLK) in nanoseconds.
4. These values are guaranteed by design, and are not tested.
5. Note this is for configuration of the fast-L2 mode. The $\overline{\text{DRTRY}}$ signal must be held negated during fast-L2 mode.

Figure 2 provides the input timing diagram for the 604.



VM = Midpoint Voltage (1.4V)

Figure 2. PowerPC 604 Microprocessor Input Timing Diagram

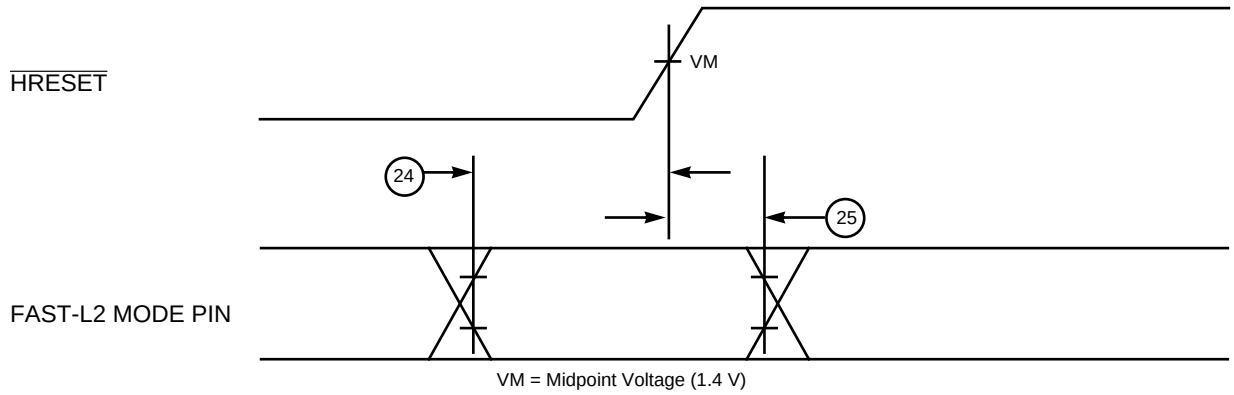


Figure 3. Fast-L2 Mode Select Input Timing Diagram

1.3.2.2 Output AC Specifications

Table 7 provides the output AC timing specifications for the 604 (shown in Figure 4). These specifications are for 25, 33.33, 40, 50, and 66 MHz bus clock (SYSCLK) frequencies. For 30 and 60 MHz bus clock frequencies, use the 33.33 and 66.67 MHz timings respectively.

Table 7. PowerPC 604 Microprocessor Output AC Timing Specifications

Vdd = 3.3 ± 5% V dc, GND = 0 V dc, C_L = 50 pF, $0 \le T_j \le 105$ °C

NUM	Characteristic	25 MHz		33.33 MHz		40 MHz		50 MHz		66.67 MHz		Unit	NOTES
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
26a	SYSCLK to $\overline{TS}$ and $\overline{XATS}$ output valid (for 5.5 V to 0.8 V)	—	14.5	—	13.0	—	11.0	—	10.0	—	9.0	ns	2
26b	SYSCLK to $\overline{TS}$ and $\overline{XATS}$ output valid (for 3.6 V to 0.8 V)	—	13.5	—	12.0	—	10.0	—	9.0	—	8.0	ns	
27a	SYSCLK to $\overline{ARTRY}$, $\overline{SHD}$ output valid (for 5.5 V to 0.8 V)	—	14.5	—	13.0	—	11.0	—	10.0	—	9.0	ns	2
27b	SYSCLK to $\overline{ARTRY}$, $\overline{SHD}$ output valid (for 3.6 V to 0.8 V)	—	13.5	—	12.0	—	10.0	—	9.0	—	8.0	ns	
28a	SYSCLK to $\overline{ABB}$ and $\overline{DBB}$ output valid (for 5.5 V to 0.8 V)	—	14.5	—	13.0	—	11.0	—	10.0	—	9.0	ns	2
28b	SYSCLK to $\overline{ABB}$ and $\overline{DBB}$ output valid (for 3.6 V to 0.8 V)	—	13.5	—	12.0	—	10.0	—	9.0	—	8.0	ns	
29a	SYSCLK to all other signals output valid (for 5.5 V to 0.8 V)	—	16.5	—	15.0	—	13.0	—	12.0	—	11.0	ns	2
29b	SYSCLK to all other signals output valid (for 3.6 V to 0.8 V)	—	15.0	—	13.0	—	11.5	—	10.5	—	9.5	ns	
30	SYSCLK to output invalid (output hold)	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns	1
31	SYSCLK to output high impedance (all signals except $\overline{ARTRY}$, $\overline{SHD}$, $\overline{ABB}$, $\overline{DBB}$, $\overline{TS}$, and $\overline{XATS}$)	—	15.0	—	13.0	—	11.5	—	10.5	—	9.5	ns	
31a	SYSCLK to output high impedance $\overline{TS}$, $\overline{XATS}$	—	13.5	—	12.0	—	10.0	—	9.0	—	8.0	ns	
32a	Precharge width for $\overline{ABB}$, $\overline{DBB}$ (1:1 and 2:1 PLL mode)	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	t_{sysclk}	3,4

Table 7. PowerPC 604 Microprocessor Output AC Timing Specifications (Continued)

Vdd = 3.3 ± 5% V dc, GND = 0 V dc, C_L = 50 pF, $0 \le T_j \le 105$ °C

NUM	Characteristic	25 MHz		33.33 MHz		40 MHz		50 MHz		66.67 MHz		Unit	NOTES
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
32b	Precharge width for $\overline{ABB}$, $\overline{DBB}$ (3:1 PLL mode)	—	0.66	—	0.66	—	0.66	—	0.66	—	0.66	t_{sysclk}	3,4
32c	Precharge width for $\overline{ABB}$, $\overline{DBB}$ (3:2 PLL mode)	—	0.33	—	0.33	—	0.33	—	0.33	—	0.33	t_{sysclk}	3,4
33a	SYSCLK to $\overline{ABB}$ and $\overline{DBB}$ high impedance after precharge (1:1 and 2:1 PLL mode)	—	0.5 * t_{sysclk} + 13.5	—	0.5 * t_{sysclk} + 12.0	—	0.5 * t_{sysclk} + 10.0	—	0.5 * t_{sysclk} + 9.0	—	0.5 * t_{sysclk} + 8.0	ns	3
33b	SYSCLK to $\overline{ABB}$ and $\overline{DBB}$ high impedance after precharge (3:1 PLL mode)	—	0.66* t_{sysclk} + 13.5	—	0.66* t_{sysclk} + 12.0	—	0.66* t_{sysclk} + 10.0	—	0.66* t_{sysclk} + 9.0	—	0.66* t_{sysclk} + 8.0	ns	3
33c	SYSCLK to $\overline{ABB}$ and $\overline{DBB}$ high impedance after precharge (3:2 PLL mode)	—	0.33* t_{sysclk} + 13.5	—	0.33* t_{sysclk} + 12.0	—	0.33* t_{sysclk} + 10.0	—	0.33* t_{sysclk} + 9.0	—	0.33* t_{sysclk} + 8.0	ns	3
34	SYSCLK to $\overline{ARTRY}$ and $\overline{SHD}$ high impedance before precharge	—	13.5	—	12.0	—	10.0	—	9.0	—	8.0	ns	
35a	SYSCLK to $\overline{ARTRY}$, and $\overline{SHD}$ precharge enable (1:1 and 2:1 PLL mode)	—	0.5* t_{sysclk} + 13.5	—	0.5* t_{sysclk} + 12.0	—	0.5* t_{sysclk} + 10.0	—	0.5* t_{sysclk} + 9.0	—	0.5* t_{sysclk} + 8.0	ns	3
35b	SYSCLK to $\overline{ARTRY}$, and $\overline{SHD}$ precharge enable (3:1 PLL mode)	—	0.33* t_{sysclk} + 13.5	—	0.33* t_{sysclk} + 12.0	—	0.33* t_{sysclk} + 10.0	—	0.33* t_{sysclk} + 9.0	—	0.33* t_{sysclk} + 8.0	ns	3
35c	SYSCLK to $\overline{ARTRY}$, and $\overline{SHD}$ precharge enable (3:2 PLL mode)	—	0.33* t_{sysclk} + 13.5	—	0.33* t_{sysclk} + 12.0	—	0.33* t_{sysclk} + 10.0	—	0.33* t_{sysclk} + 9.0	—	0.33* t_{sysclk} + 8.0	ns	3
36a	Precharge width for $\overline{ARTRY}$ and $\overline{SHD}$ (1:1, 2:1, and 3:2 PLL modes)	1.0		1.0		1.0		1.0		1.0		t_{sysclk}	3,4

Table 7. PowerPC 604 Microprocessor Output AC Timing Specifications (Continued)

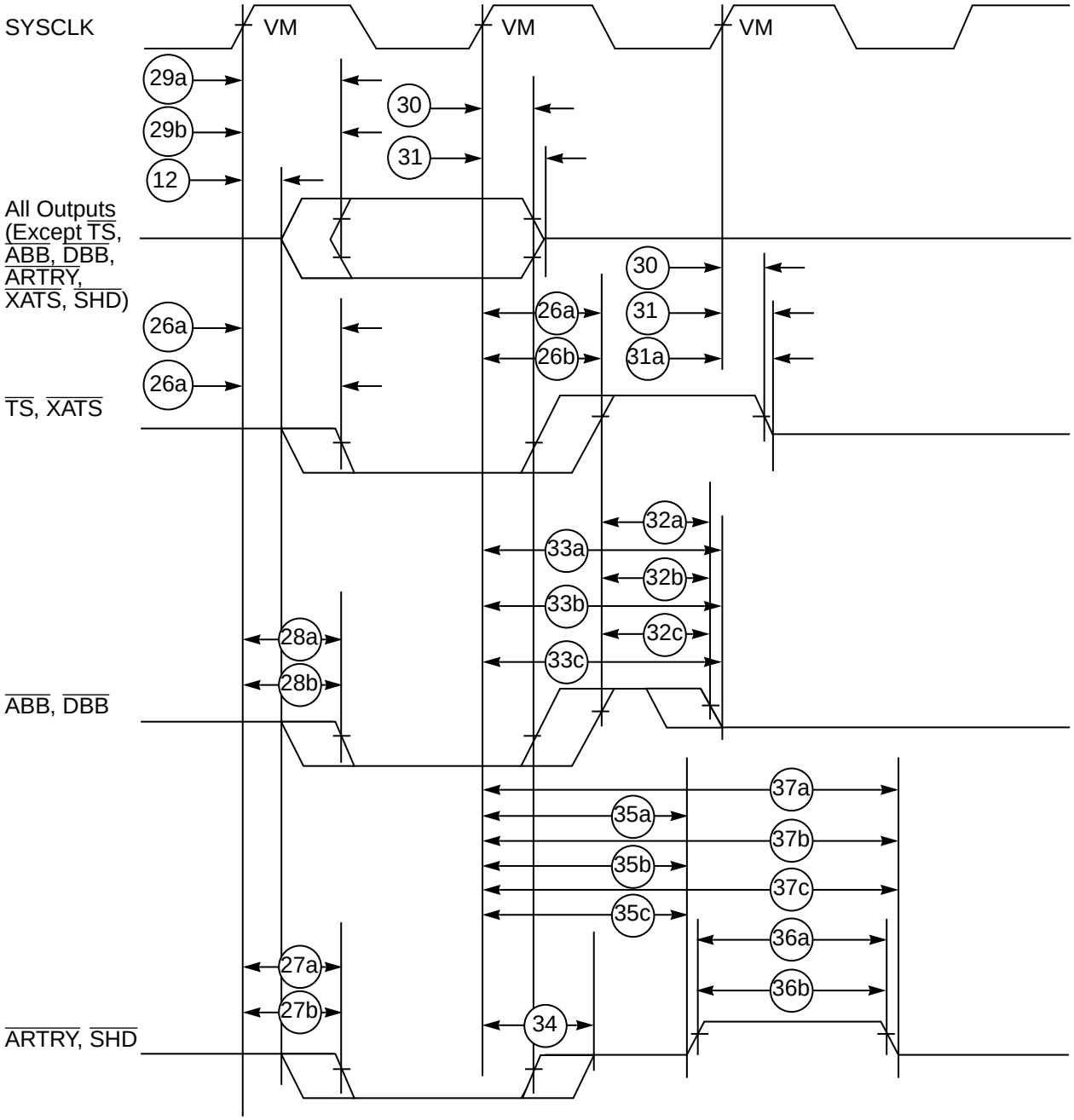
Vdd = 3.3 ± 5% V dc, GND = 0 V dc, C_L = 50 pF, $0 \le T_j \le 105$ °C

NUM	Characteristic	25 MHz		33.33 MHz		40 MHz		50 MHz		66.67 MHz		Unit	NOTES
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
36b	Precharge width for $\overline{\text{ARTRY}}$ and $\overline{\text{SHD}}$ (3:1 PLL mode)	0.66		0.66		0.66		0.66		0.66		t_{sysclk}	3,4
37a	SYSCLK to $\overline{\text{ARTRY}}$ and $\overline{\text{SHD}}$ high impedance after precharge (1:1 and 2:1 PLL mode)	—	1.5* t_{sysclk} + 13.5	—	1.5* t_{sysclk} + 12.0	—	1.5* t_{sysclk} + 10.0	—	1.5* t_{sysclk} + 9.0	—	1.5* t_{sysclk} + 8.0	ns	3
37b	SYSCLK to $\overline{\text{ARTRY}}$ and $\overline{\text{SHD}}$ high impedance after precharge (3:1 PLL mode)	—	1.0 * t_{sysclk} + 13.5	—	1.0 * t_{sysclk} + 12.0	—	1.0 * t_{sysclk} + 10.0	—	1.0 * t_{sysclk} + 9.0	—	1.0 * t_{sysclk} + 8.0	ns	3
37c	SYSCLK to $\overline{\text{ARTRY}}$ and $\overline{\text{SHD}}$ high impedance after precharge (3:2 PLL mode)	—	1.33 * t_{sysclk} + 13.5	—	1.33 * t_{sysclk} + 12.0	—	1.33 * t_{sysclk} + 10.0	—	1.33 * t_{sysclk} + 9.0	—	1.33 * t_{sysclk} + 8.0	ns	3
38a	Rise time ($\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	TBD		TBD		TBD		TBD		TBD		ns	4
38b	Rise time (all signals except $\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	TBD		TBD		TBD		TBD		TBD		ns	4
38c	Fall time ($\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	TBD		TBD		TBD		TBD		TBD		ns	4
38d	Fall time (all signals except $\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	TBD		TBD		TBD		TBD		TBD		ns	4

Notes:

1. This minimum parameter assumes C_L = 0 pF.
2. SYSCLK to output valid (5.5 V to 0.8 V) includes the extra delay associated with discharging the external voltage from 5.5 V to 0.8 V instead of from 3.6 V to 0.8 V (5-V CMOS levels instead of 3.3-V CMOS levels).
3. t_{sysclk} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). When the unit is given as t_{sysclk} the numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
4. These specifications are nominal values.

Figure 4 provides the output timing diagram for the 604.



Notes: VM = Midpoint Voltage (1.4 V)
All output specifications are measured from 0.8 V or 2.0 V of the signal in question to the 1.4 V of the rising edge of the input SYSCLK.

Figure 4. PowerPC 604 Microprocessor Output Timing Diagram

1.3.3 PLL Power Supply Filtering

The AVDD power signal is provided on the 604 to provide power to the clock generation phase-lock loop. To ensure stability of the internal clock, the power supplied to the AVDD input signal should be filtered using a circuit similar to the one shown in Figure 5. Note that the capacitors should be placed as close as possible to the AVDD input signal.

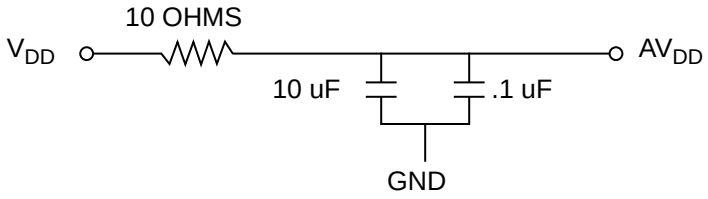


Figure 5. PLL Power Supply Filter Circuit

1.3.4 JTAG AC Timing Specifications

Table 8 provides the JTAG AC timing specifications.

Table 8. JTAG AC Timing Specifications (Independent of SYSCLK)

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	16	MHz	
1	TCK cycle time	62.5	—	ns	
2	TCK clock pulse width measured at 1.5 V	25	—	ns	
3	TCK rise and fall times	0	3	ns	
4	$\overline{\text{TRST}}$ setup time to TCK rising edge	13	—	ns	2
5	$\overline{\text{TRST}}$ assert time	40	—	ns	
6	Boundary-scan input data setup time	0	—	ns	
7	Boundary-scan input data hold time	27	—	ns	
8	TCK to output data valid	4	25	ns	
9	TCK to output high impedance	3	24	ns	
10	TMS, TDI data setup time	0	—	ns	
11	TMS, TDI data hold time	25	—	ns	
12	TCK to TDO data valid	4	24	ns	1
13	TCK to TDO high impedance	3	15	ns	1

Notes:

1. Load capacitance = 20 pF.
2. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes.

Figure 6 provides the JTAG clock input timing diagram.

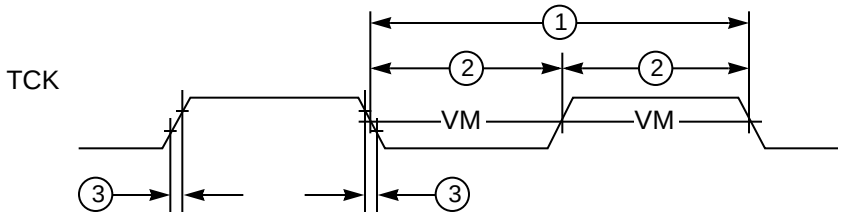


Figure 6. Clock Input Timing Diagram

Figure 7 provides the $\overline{\text{TRST}}$ timing diagram.

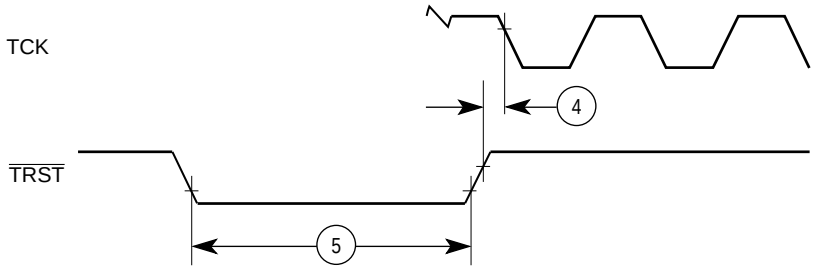


Figure 7. $\overline{\text{TRST}}$ Timing Diagram

Figure 8 provides the boundary-scan timing diagram.

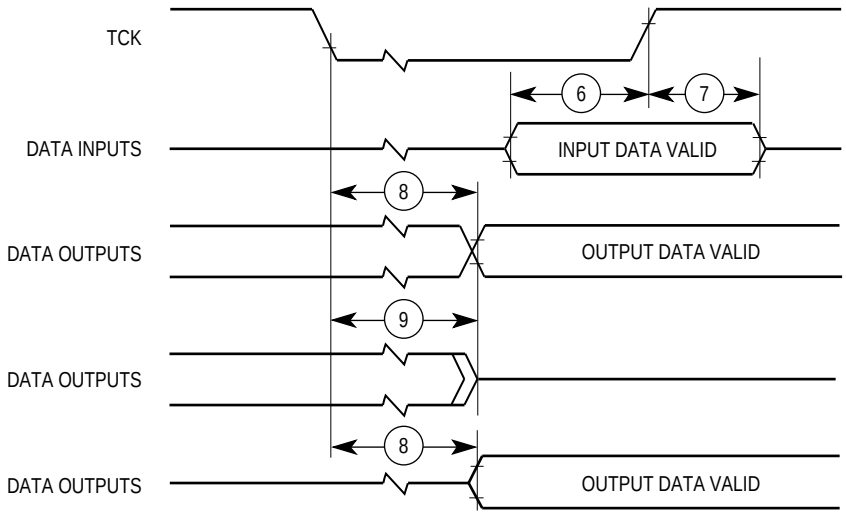


Figure 8. Boundary-Scan Timing Diagram

Figure 9 provides the test access port timing diagram.

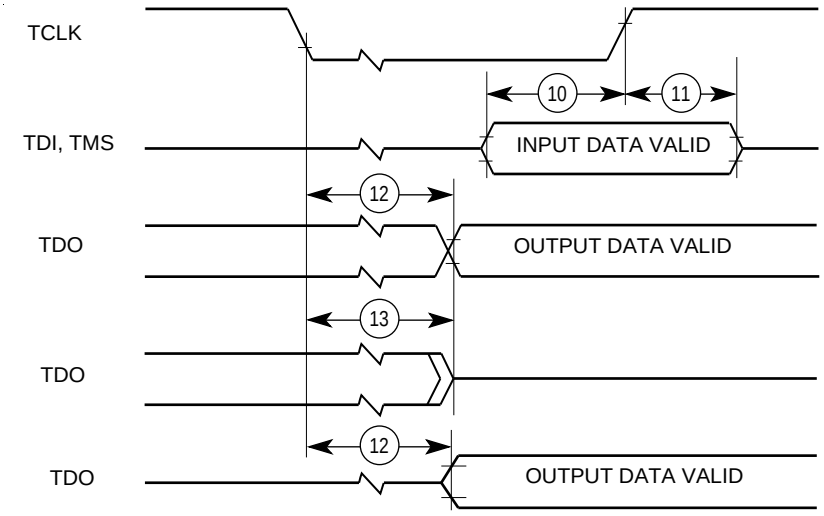


Figure 9. Test Access Port Timing Diagram

1.4 PowerPC 604 Microprocessor Pin Assignments

The following sections contain the pinout diagrams for the 604. Note that the 604 is currently offered in three packages—wire-bond CQFP, C4-CQFP, and ball grid array (BGA). Motorola offers a wire-bond CQFP, a C4-CQFP, and a BGA package. IBM offers a C4-CQFP and a BGA package. Both IBM and Motorola CQFP and BGA packages have identical pinouts.

1.4.1 Pinout Diagram for the CQFP Package

Figure 10 contains the pinout diagram of the CQFP package for the 604. The IBM and Motorola CQFP packages are similar except that the die is visible on the IBM package.

Figure 10 contains the top view of the CQFP package for the 604.

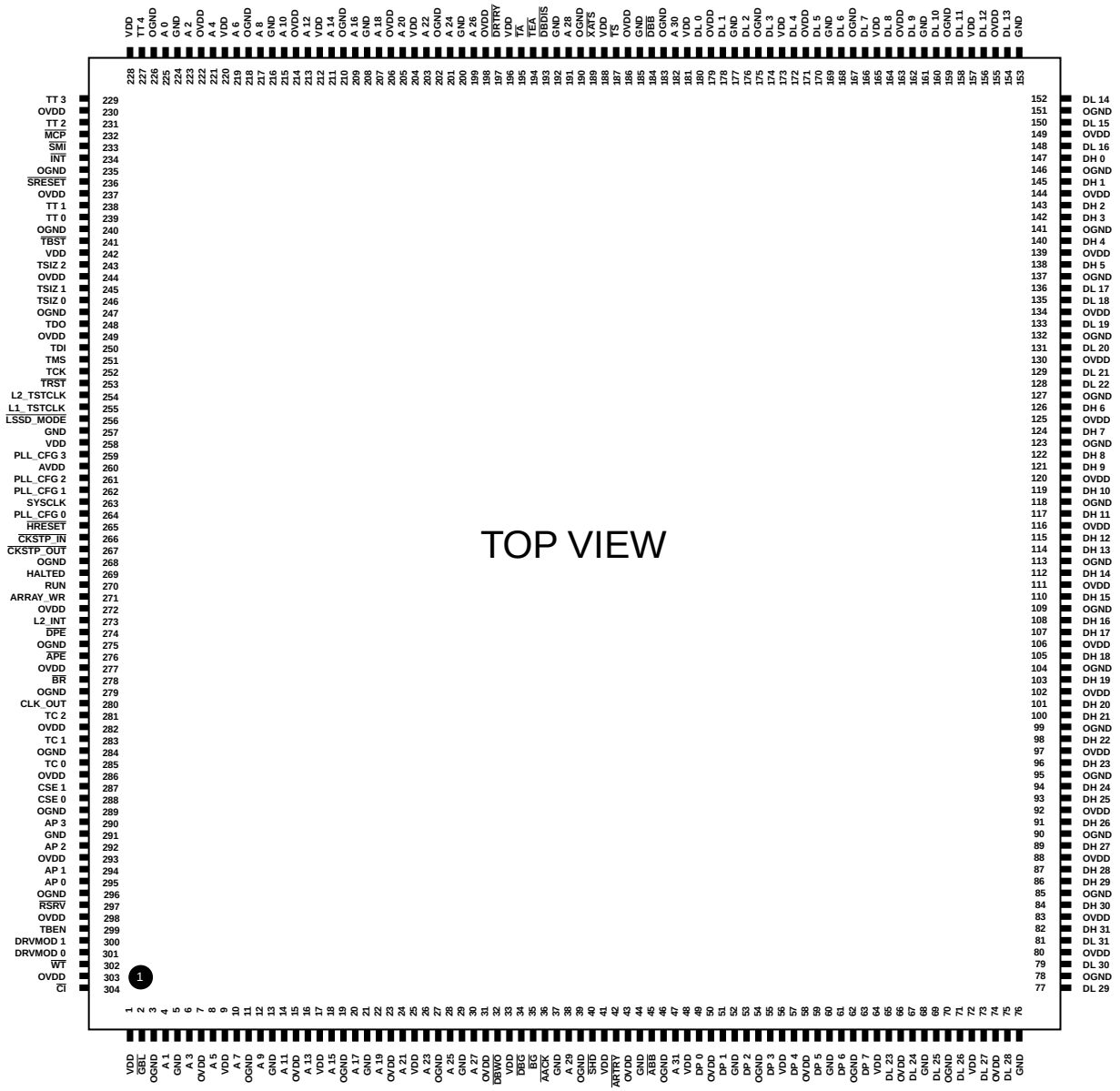
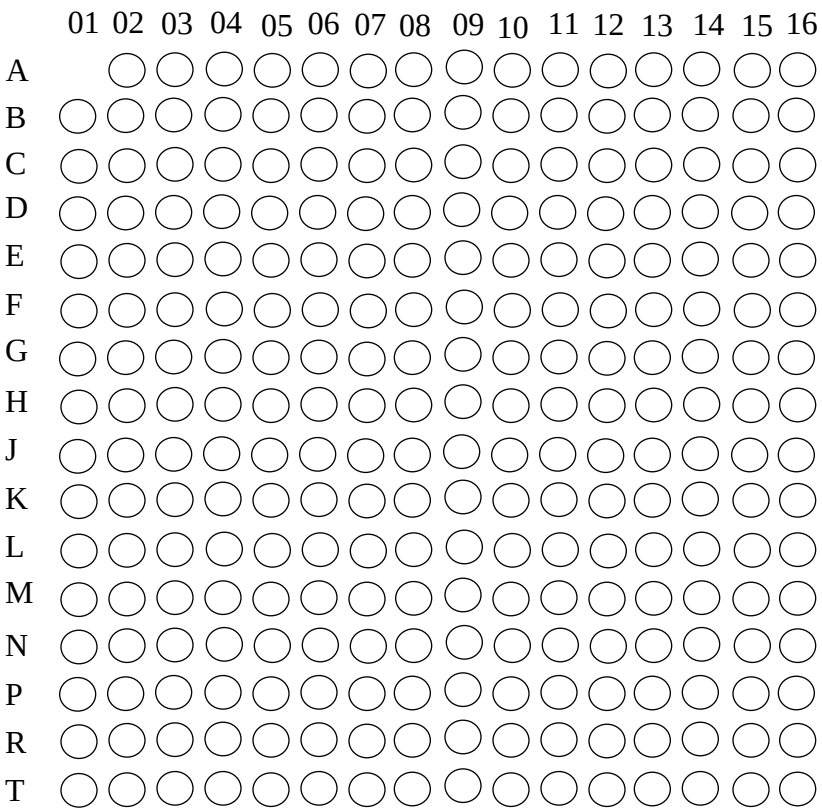


Figure 10. Pinout Diagram of the CQFP Package

1.4.2 Pinout Diagram for the BGA Package

Figure 11 (in part A) shows the pinout of the BGA package as viewed from the top surface. Part B shows the side profile of the BGA package to indicate the direction of the top surface view.

Part A



Part B

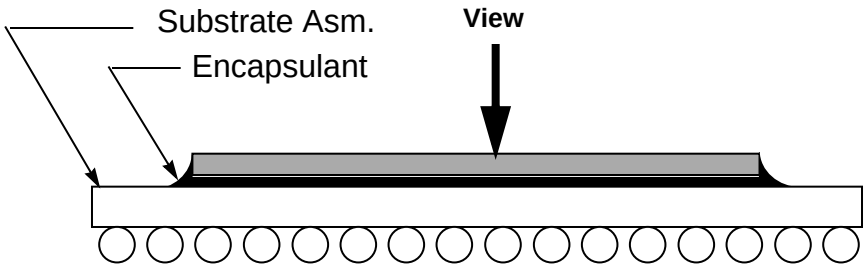


Figure 11. Pinout of the BGA Package as Viewed from the Top Surface

1.5 PowerPC 604 Microprocessor Pinout Listings

The following sections contain the pinout listings for the 604 CQFP and BGA packages.

1.5.1 Pinout Listing for the CQFP Package

Table 9 provides the pinout listing for the 604 CQFP package.

Table 9. Pinout Listing for the CQFP Package

Signal Name	Pin Number	Active	I/O
A0–A31	225, 4, 223, 6, 221, 8, 219, 10, 217, 12, 215, 14, 213, 16, 211, 18, 209, 20, 207, 22, 205, 24, 203, 26, 201, 28, 199, 30, 191, 38, 182, 47	High	I/O
$\overline{\text{AACK}}$	36	Low	Input
$\overline{\text{ABB}}$	45	Low	I/O
AP0–AP3	295, 294, 292, 290	High	I/O
$\overline{\text{APE}}$	276	Low	Output
ARRAY_WR[1]	271	Low	Input
$\overline{\text{ARTRY}}$	42	Low	I/O
AVDD	260	—	—
$\overline{\text{BG}}$	35	Low	Input
$\overline{\text{BR}}$	278	Low	Output
$\overline{\text{CI}}$	304	Low	Output
$\overline{\text{CKSTP\_IN}}$	266	Low	Input
$\overline{\text{CKSTP\_OUT}}$	267	Low	Output
CLK_OUT	280	—	Output
CSE0–CSE1	288, 287	High	Output
$\overline{\text{DBB}}$	184	Low	I/O
$\overline{\text{DBG}}$	34	Low	Input
$\overline{\text{DBDIS}}$	193	Low	Input
$\overline{\text{DBWO}}$	32	Low	Input
DH0–31	147, 145, 143, 142, 140, 138, 126, 124, 122, 121, 119, 117, 115, 114, 112, 110, 108, 107, 105, 103, 101, 100, 98, 96, 94, 93, 91, 89, 87, 86, 84, 82	High	I/O
DL0–DL31	180, 178, 176, 174, 172, 170, 168, 166, 164, 162, 160, 158, 156, 154, 152, 150, 148, 136, 135, 133, 131, 129, 128, 65, 67, 69, 71, 73, 75, 77, 79, 81	High	I/O
DP0–DP7	49, 51, 53, 55, 57, 59, 61, 63	High	I/O

Table 9. Pinout Listing for the CQFP Package (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{\text{DPE}}$	274	Low	Output
$\overline{\text{DRTRY}}$	197	Low	Input
DRVMOD0–DRVMOD1[2]	301, 300	High	Input
$\overline{\text{GBL}}$	2	Low	I/O
GND	5, 13, 21, 29, 37, 44, 52, 60, 68, 76, 153, 161, 169, 177, 185, 192, 200, 208, 216, 224, 257, 291	—	—
HALTED	269	High	Output
$\overline{\text{HRESET}}$	265	Low	Input
$\overline{\text{INT}}$	234	Low	Input
L1_TSTCLK[1]	255	Low	Input
L2_INT	273	High	Input
L2_TSTCLK[1]	254	Low	Input
$\overline{\text{LSSD\_MODE}}$ [1]	256	Low	Input
$\overline{\text{MCP}}$	232	Low	Input
OGND	3, 11, 19, 27, 39, 46, 54, 62, 70, 78, 85, 90, 95, 99, 104, 109, 113, 118, 123, 127, 132, 137, 141, 146, 151, 159, 167, 175, 183, 190, 202, 210, 218, 226, 235, 240, 247, 268, 275, 279, 284, 289, 296	—	—
OVDD	7, 15, 23, 31, 43, 50, 58, 66, 74, 80, 83, 88, 92, 97, 102, 106, 111, 116, 120, 125, 130, 134, 139, 144, 149, 155, 163, 171, 179, 186, 198, 206, 214, 222, 230, 237, 244, 249, 272, 277, 282, 286, 293, 298, 303	—	—
PLL_CFG0–PLL_CFG3	264, 262, 261, 259	High	Input
$\overline{\text{RSRV}}$	297	Low	Output
RUN	270	High	Input
$\overline{\text{SHD}}$	40	Low	I/O
$\overline{\text{SMI}}$	233	Low	Input
$\overline{\text{SRESET}}$	236	Low	Input
SYSCLK	263	—	Input
$\overline{\text{TA}}$	195	Low	Input
TBEN	299	High	Input
$\overline{\text{TBST}}$	241	Low	I/O
TC0–TC2	285, 283, 281	High	Output

Table 9. Pinout Listing for the CQFP Package (Continued)

Signal Name	Pin Number	Active	I/O
TCK	252	High	Input
TDI	250	High	Input
TDO	248	High	Output
$\overline{\text{TEA}}$	194	Low	Input
TMS	251	High	Input
$\overline{\text{TRST}}$	253	Low	Input
$\overline{\text{TS}}$	187	Low	I/O
TSIZ0–TSIZ2	246, 245, 243	High	I/O
TT0–TT4	239, 238, 231, 229, 227	High	I/O
$\overline{\text{WT}}$	302	Low	Output
VDD	1, 9, 17, 25, 33, 41, 48, 56, 64, 72, 157, 165, 173, 181, 188, 196, 204, 212, 220, 228, 242, 258	—	—
$\overline{\text{XATS}}$	189	Low	I/O

Notes:
1. These are test signals for factory use only and must be pulled up to VDD for normal machine operation.
2. These are drive mode signals that must be pulled up to VDD to operate in accordance with these specifications.

1.5.2 Pinout Listing for the BGA Package

Table 10 provides the pinout listing for the 604 BGA package.

Table 10. Pinout Listing for the BGA Package

Signal Name	Pin Number	Active	I/O
A0–A31	C16, E04, D13, F02, D14, G01, D15, E02, D16, D04, E13, GO2, E15, H01, E16, H02, F13, J01, F14, J02, F15, H03, F16, F04, G13, K01, G15, K02, H16, M01, J15, P01	High	I/O
$\overline{\text{AACK}}$	L02	Low	Input
$\overline{\text{ABB}}$	K04	Low	I/O
AP0–AP3	C01, B04, B03, B02	High	I/O
$\overline{\text{APE}}$	A04	Low	Output
ARRAY_WR [1]	B07	Low	Input
$\overline{\text{ARTRY}}$	J04	Low	I/O
AVDD	A10	—	—
$\overline{\text{BG}}$	L01	Low	Input

Table 10. Pinout Listing for the BGA Package (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{BR}$	B06	Low	Output
$\overline{CI}$	E01	Low	Output
$\overline{CKSTP\_IN}$	D08	Low	Input
$\overline{CKSTP\_OUT}$	A06	Low	Output
CLK_OUT	D07	—	Output
CSE0–CSE1	B01, B05	High	Output
$\overline{DBB}$	J14	Low	I/O
$\overline{DBG}$	N01	Low	Input
$\overline{DBDIS}$	H15	Low	Input
$\overline{DBWO}$	G04	Low	Input
DH0–31	P14, T16, R15, T15, R13, R12, P11, N11, R11,T12, T11, R10, P09, N09, T10, R09, T09, P08, N08, R08, T08, N07, R07, T07, P06, N06, R06, T06, R05, N05, T05, T04	High	I/O
DL0–DL31	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P03, N03, N04, R03, T01, T02, P04, T03, R04	High	I/O
DP0–DP7	M02, L03, N02, L04, R01, P02, M04, R02	High	I/O
$\overline{DPE}$	A05	Low	Output
$\overline{DRTRY}$	G16	Low	Input
DRVMOD0–DRVMOD1[2]	D05, C03	High	Input
$\overline{GBL}$	F01	Low	I/O
GND	C05, C12, E03, E06, E08, E09, E11, E14, F05, F07, F10, F12, G06, G08, G09, G11, H05, H07, H10, H12, J05, J07, J10, J12, K06, K08, K09, K11, L05, L07, L10, L12, M03, M06, M08, M09, M11, M14, P05, P12	—	—
HALTED	B08	High	Output
$\overline{HRESET}$	A07	Low	Input
$\overline{INT}$	B15	Low	Input
L1_TSTCLK [1]	D11	Low	Input
L2_INT	D06	High	Input
L2_TSTCLK [1]	D12	Low	Input
$\overline{LSSD\_MODE}$ [1]	B10	Low	Input
$\overline{MCP}$	C13	Low	Input
OVDD [3]	F06, F08, F09, F11, G07, G10, H06, H08, H09, H11, J06, J08, J09, J11, K07, K10, L06, L08, L09, L11	—	—
PLL_CFG(0–3)	A08, B09, A09, D09	High	Input

Table 10. Pinout Listing for the BGA Package (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{\text{RSRV}}$	D01	Low	Output
RUN	C08	High	Input
$\overline{\text{SHD}}$	H04	Low	I/O
$\overline{\text{SMI}}$	A16	Low	Input
$\overline{\text{SRESET}}$	B14	Low	Input
SYSCLK	C09	—	Input
$\overline{\text{TA}}$	H14	Low	Input
TBEN	C02	High	Input
$\overline{\text{TBST}}$	A14	Low	I/O
TC0–TC2	A02, A03, C06	High	Output
TCK	C11	High	Input
TDI	A11	High	Input
TDO	A12	High	Output
$\overline{\text{TEA}}$	H13	Low	Input
TMS	B11	High	Input
$\overline{\text{TRST}}$	C10	Low	Input
$\overline{\text{TS}}$	J13	Low	I/O
TSIZ0–TSIZ2	A13, D10, B12	High	I/O
TT0–TT4	B13, A15, B16, C14, C15	High	I/O
$\overline{\text{WT}}$	D02	Low	Output
VDD[3]	C07, E05, E07, E10, E12, G03, G05, G12, G14, K03, K05, K12, K14, M05, M07, M10, M12, P07, P10	—	—
$\overline{\text{XATS}}$	J16	Low	I/O

Note:

1. These are test signals for factory use only and must be pulled up to VDD for normal machine operation.
2. These are drive mode signals that must be pulled up to VDD to operate in accordance to these specifications.
3. In the 604 BGA package, there is no electrical distinction between the OVDD and the VDD pins. These signals are internally shorted together. The OVDD and VDD signals have been listed separately to maintain compatibility with future parts.

1.6 PowerPC 604 Microprocessor Package Description

The following sections provide the package parameters and the mechanical dimensions for the 604.

1.6.1 Wire-Bond CQFP Package Description

The following sections provide the package parameters and mechanical dimensions for the Motorola wire-bond CQFP package.

1.6.1.1 Package Parameters

The package parameters are as provided in the following list. The package type is 40 mm, 304-pin ceramic quad flat pack.

Package outline	40 mm
Interconnects	304
Pitch	0.5 mm
Lead plating	100% Sn
Maximum module height	4.15 mm
Co-planarity specification	0.1 mm

1.6.1.2 Mechanical Dimensions

Figure 12 shows the mechanical dimensions for the wire-bond CQFP package.

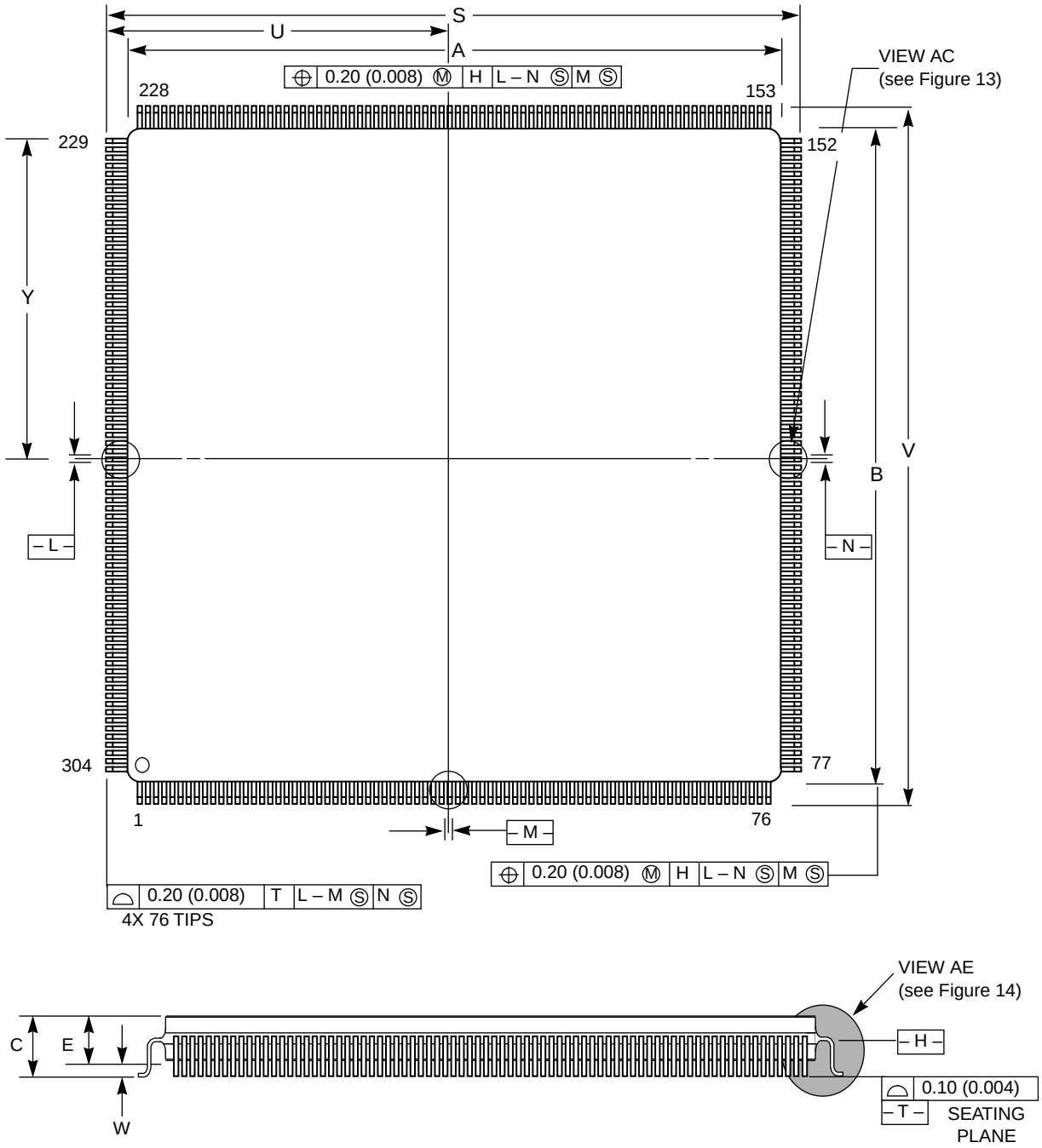


Figure 12. Mechanical Dimensions of the Wire-Bond CQFP Package

Figure 13 and Figure 14 provide a more detailed representation of portions of the wire-bond CQFP package.

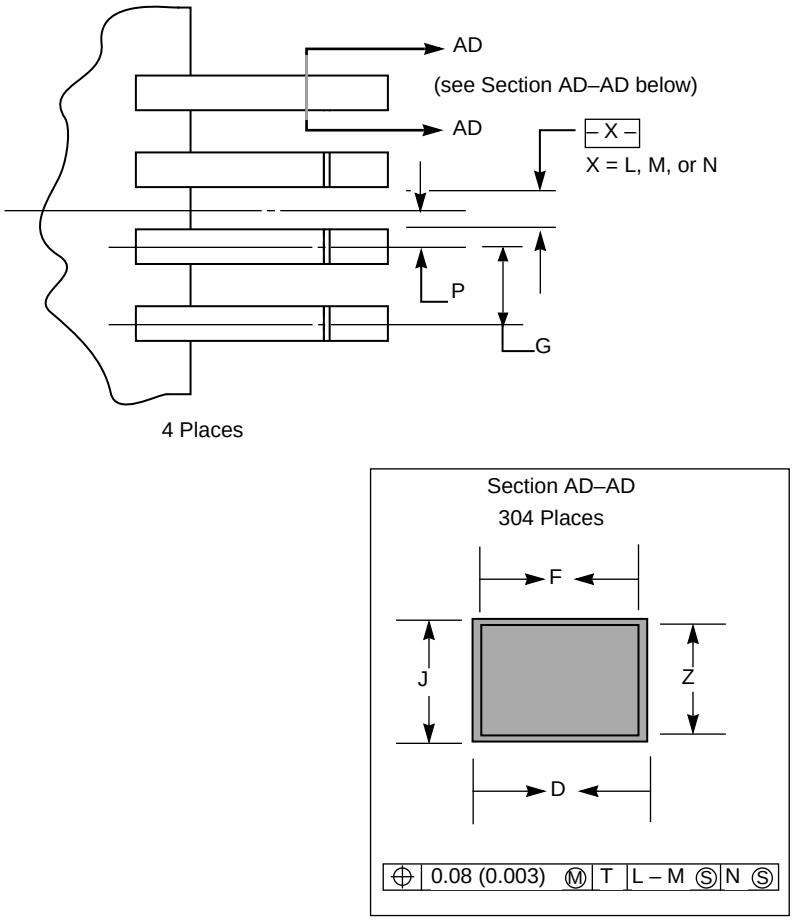


Figure 13. Wire-Bond CQFP Mechanical Dimensions—View AC

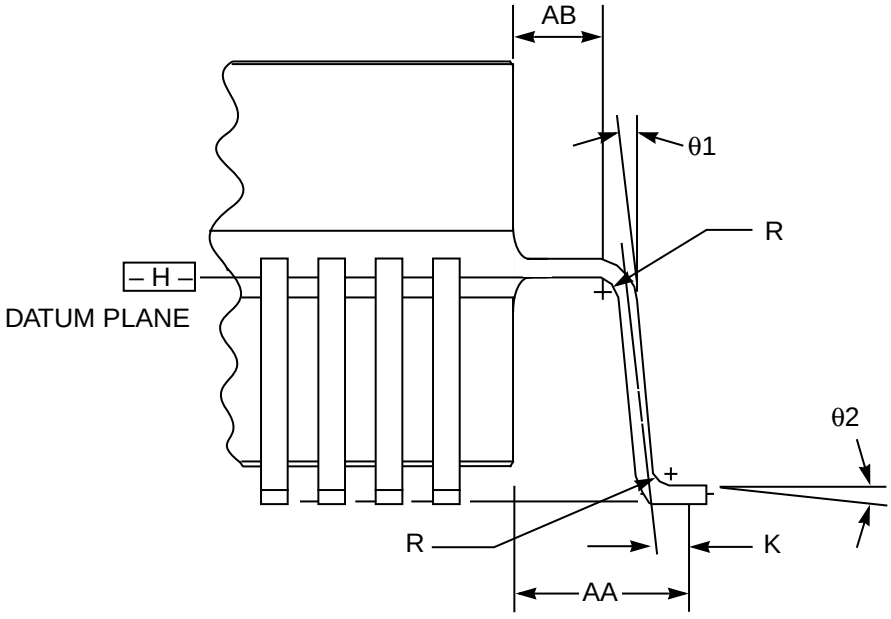


Figure 14. Wire-Bond CQFP Mechanical Dimensions—View AE

Table 11 lists the mechanical dimensions values for the Motorola wire-bond CQFP package.

Table 11. Wire-Bond CQFP Mechanical Dimensions Values

Dim	Millimeters	
	Min	Max
A	38.86	39.75
B	38.86	39.75
C	—	4.15
D	0.18	0.27
E	3.00	3.70
F	0.17	0.23
G	0.50 BSC	
J	0.13	0.175
K	0.45	0.55
P	0.25 BSC	
R	0.15 REF	
S	42.60 BSC	
U	21.30 BSC	
V	42.60 BSC	
W	0.25	—
Y	21.30 BSC	
Z	0.12	0.13
AA	1.80 REF	
AB	0.95 REF	
q1	2°	6°
θ2	1°	7°

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M–1982.
2. Controlling dimension—millimeter.
3. Datum plane – H – is located at bottom of lead and is coincident with the lead where the lead exits the ceramic body at the bottom of the parting line.
4. Datums – L –, – M –, and – N – to be determined at datum plane – H –.
5. Dimensions S and V to be determined at seating plane – T –.
6. Dimensions A and B define maximum ceramic body dimensions including glass protrusion and top and bottom mismatch.

1.6.2 C4-CQFP Package Description

The following sections provide the package parameters and mechanical dimensions for the C4-CQFP package.

1.6.2.1 Motorola C4-CQFP Package Parameters

The package parameters for the Motorola C4-CQFP are as provided in the following list. The package type is 40 mm, 304-pin ceramic quad flat pack.

Package outline	40 mm
Interconnects	304
Pitch	0.5 mm
Lead plating	Ni Au
C4 encapsulation	EPX 5341
Maximum module height	3.25 mm
Co-planarity specification	0.10 mm

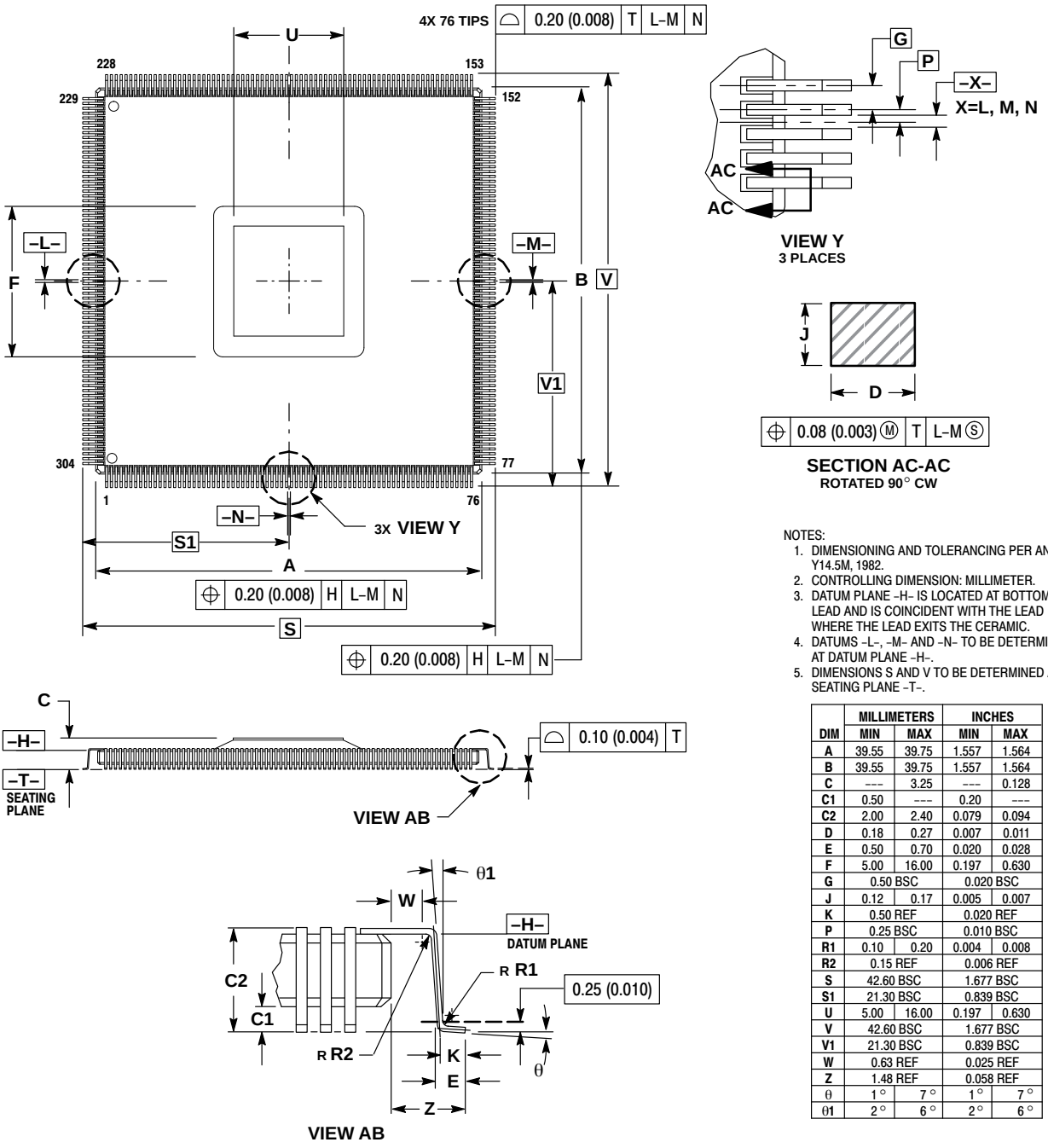
1.6.2.2 IBM C4-CQFP Package Parameters

The package parameters for the IBM C4-CQFP are as provided in the following list. The package type is 40 mm, 304-pin ceramic quad flat pack.

Package outline	40 mm
Interconnects	304
Pitch	0.5 mm
Lead plating	Ni Au
Lead encapsulation	HYSOL 4323
c4 encapsulation	EPX 5341
Maximum module height	3.1 mm
Co-planarity specification	0.08 mm

1.6.2.3 Mechanical Dimensions of the Motorola C4-CQFP Package

Figure 15 shows the mechanical dimensions of the Motorola C4-CQFP package.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE CERAMIC.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	39.55	39.75	1.557	1.564
B	39.55	39.75	1.557	1.564
C	---	3.25	---	0.128
C1	0.50	---	0.20	---
C2	2.00	2.40	0.079	0.094
D	0.18	0.27	0.007	0.011
E	0.50	0.70	0.020	0.028
F	5.00	16.00	0.197	0.630
G	0.50 BSC		0.020 BSC	
J	0.12	0.17	0.005	0.007
K	0.50 REF		0.020 REF	
P	0.25 BSC		0.010 BSC	
R1	0.10	0.20	0.004	0.008
R2	0.15 REF		0.006 REF	
S	42.60 BSC		1.677 BSC	
S1	21.30 BSC		0.839 BSC	
U	5.00	16.00	0.197	0.630
V	42.60 BSC		1.677 BSC	
V1	21.30 BSC		0.839 BSC	
W	0.63 REF		0.025 REF	
Z	1.48 REF		0.058 REF	
θ	1°	7°	1°	7°
θ1	2°	6°	2°	6°

Figure 15. Mechanical Dimensions of the Motorola C4-CQFP Package

1.6.2.4 Mechanical Dimensions of the IBM C4-CQFP Package

Figure 16 shows the mechanical dimensions for the IBM C4-CQFP.

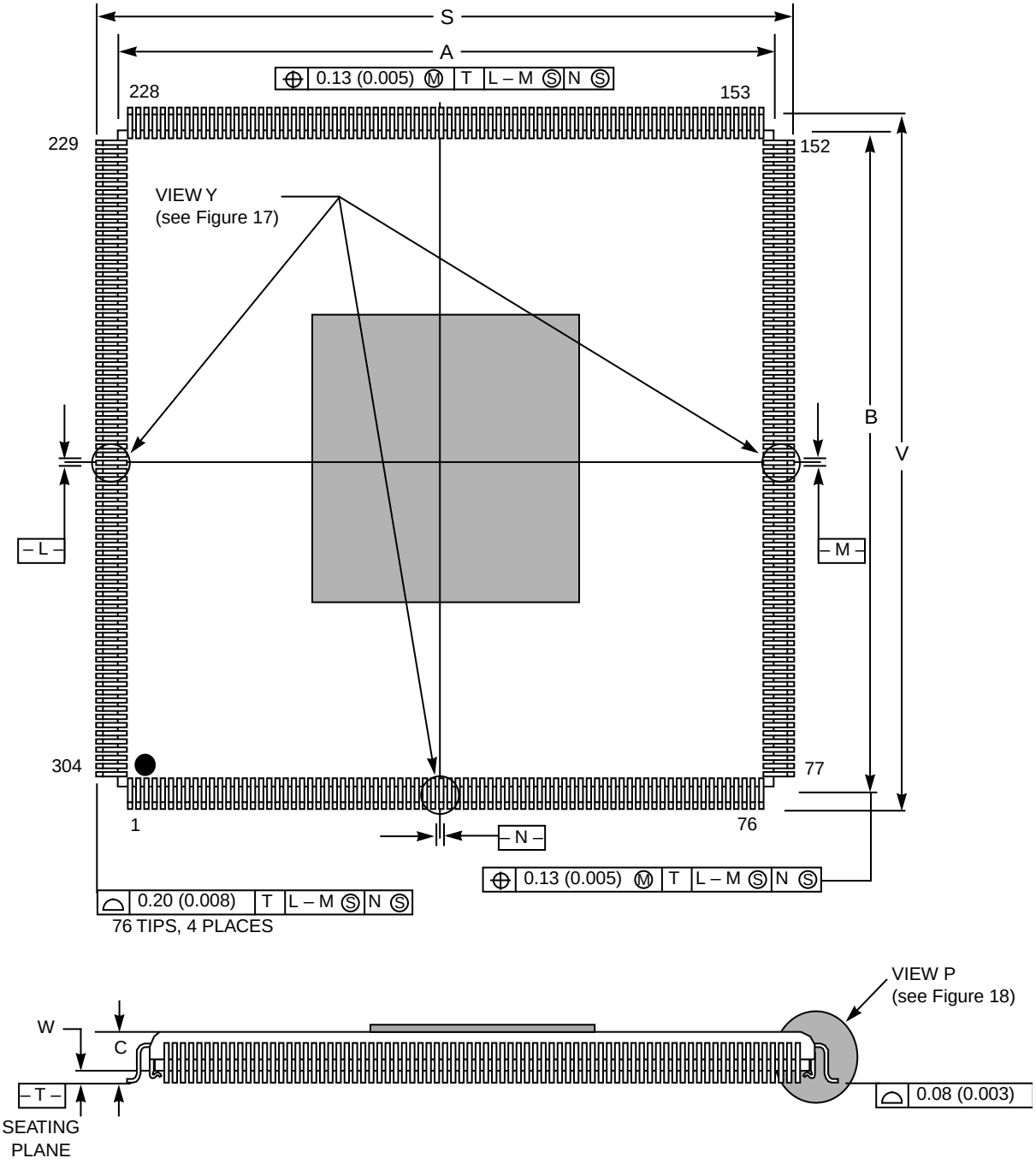


Figure 16. Mechanical Dimensions of the IBM C4-CQFP Package

Figure 17 and Figure 18 provide a more detailed representation of portions of IBM C4-CQFP package.

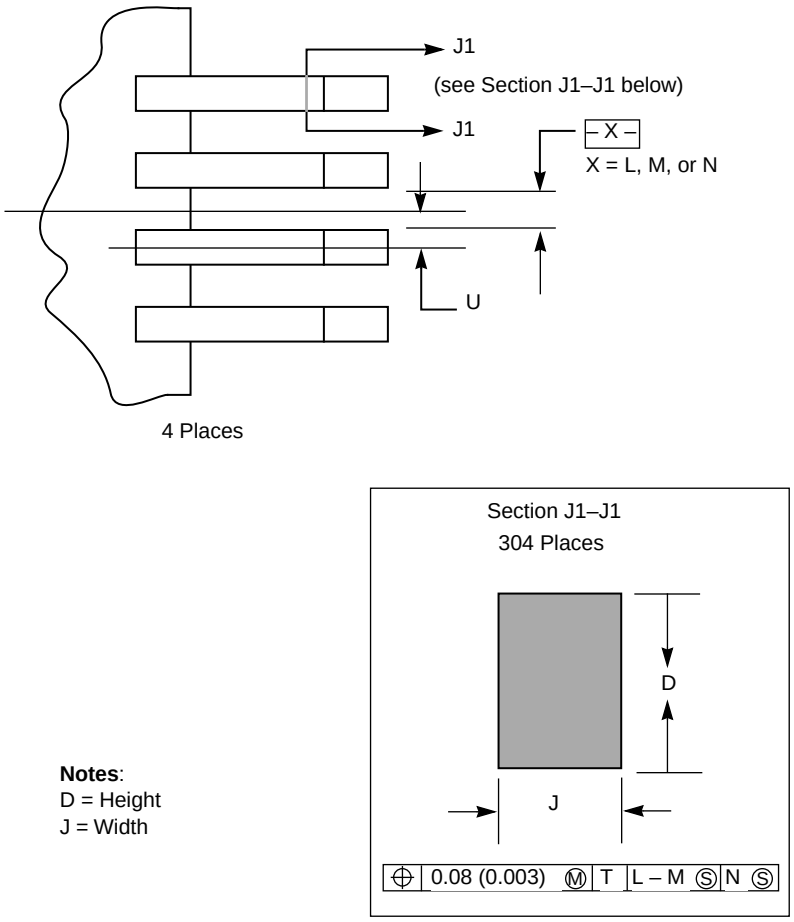


Figure 17. IBM C4-CQFP Mechanical Dimensions—View Y

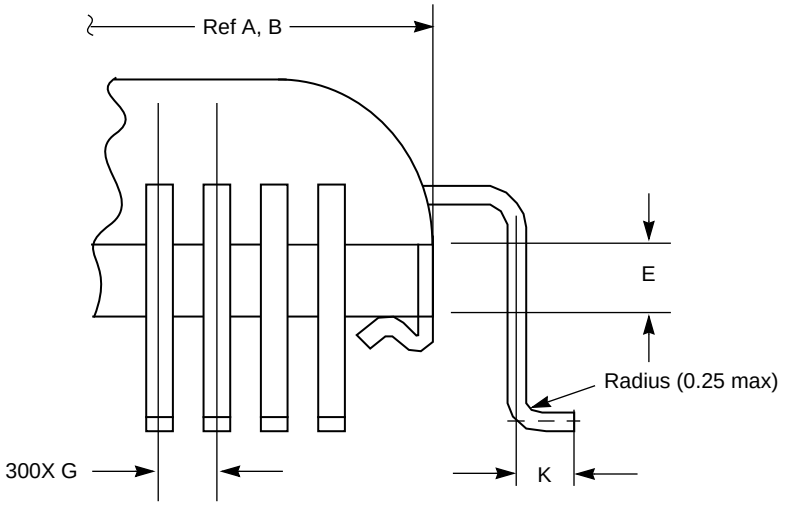


Figure 18. IBM C4-CQFP Mechanical Dimensions—View P

Table 11 lists the mechanical dimensions values for the IBM C4-CQFP package.

Table 12. Mechanical Dimensions Values

Dim	Millimeters	
	Min	Max
A	39.80	40.20
B	39.80	40.20
C	3.05	3.15
D	0.18	0.28
E	0.585	0.685
G	0.45	0.55
J	0.12	0.20
K	0.40	0.60
S	42.4	42.8
V	42.4	42.8
W	0.30	0.40

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982.
2. Controlling dimension—millimeter.
3. Datums – L –, –M –, and – N – to be determined at seating plane.
4. Dimensions S and V to be determined at seating plane – T–.
5. Dimensions A and B to outside of lead clip.

1.6.3 BGA Package Description

The following sections provide the package parameters and mechanical dimensions for the IBM and Motorola BGA packages.

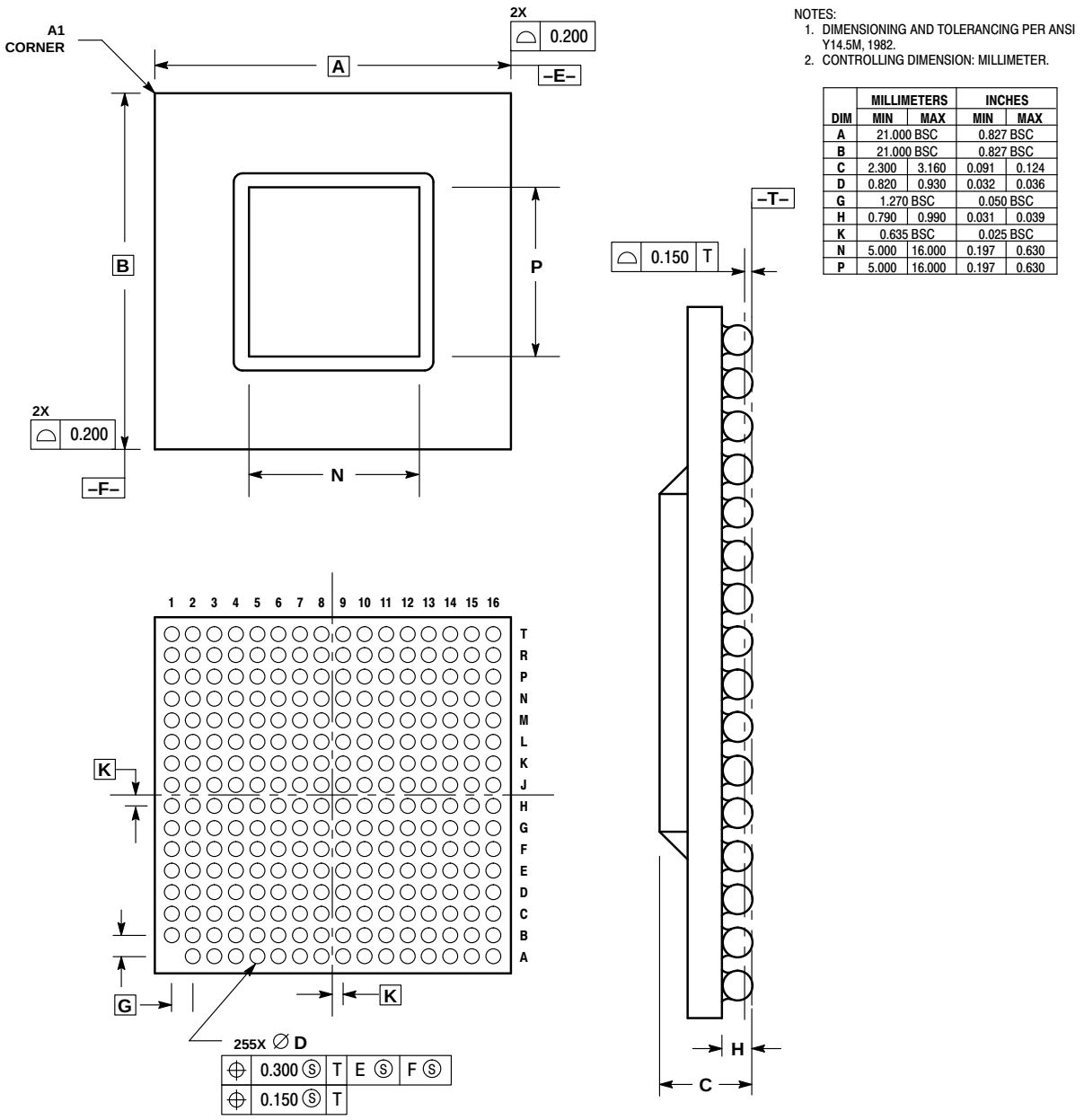
1.6.3.1 Package Parameters

The package parameters are as provided in the following list. The package type is 21 mm, 256-lead ceramic ball grid array (BGA).

Package outline	21 mm
Interconnects	255
Pitch	1.27 mm
Maximum module height	3.16 mm

1.6.3.2 Mechanical Dimensions of the BGA Package

Figure 19 provides the mechanical dimensions and bottom surface nomenclature of the IBM and Motorola BGA package.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	21.000 BSC		0.827 BSC	
B	21.000 BSC		0.827 BSC	
C	2.300	3.160	0.091	0.124
D	0.820	0.930	0.032	0.036
G	1.270 BSC		0.050 BSC	
H	0.790	0.990	0.031	0.039
K	0.635 BSC		0.025 BSC	
N	5.000	16.000	0.197	0.630
P	5.000	16.000	0.197	0.630

Figure 19. Mechanical Dimensions and Bottom Surface Nomenclature of the BGA Package

1.7 Ordering Information

This section provides the part numbering nomenclature for the 604. Note that the individual part numbers correspond to a specific combination of 604 internal/bus frequencies, which must be observed to ensure proper operation of the device. For available frequency combinations, contact your local Motorola or IBM sales office.

In addition to the processor frequency and bus ratio, the part numbering scheme also consists of a part modifier. The part modifier allows for the availability of future enhanced parts (that is, lower voltage, lower power, higher performance, etc.). Currently the only 604 part available for ordering is the original production design.

Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

1.7.1 Motorola Part Number Key

Figure 20 provides the Motorola part numbering nomenclature for the 604.

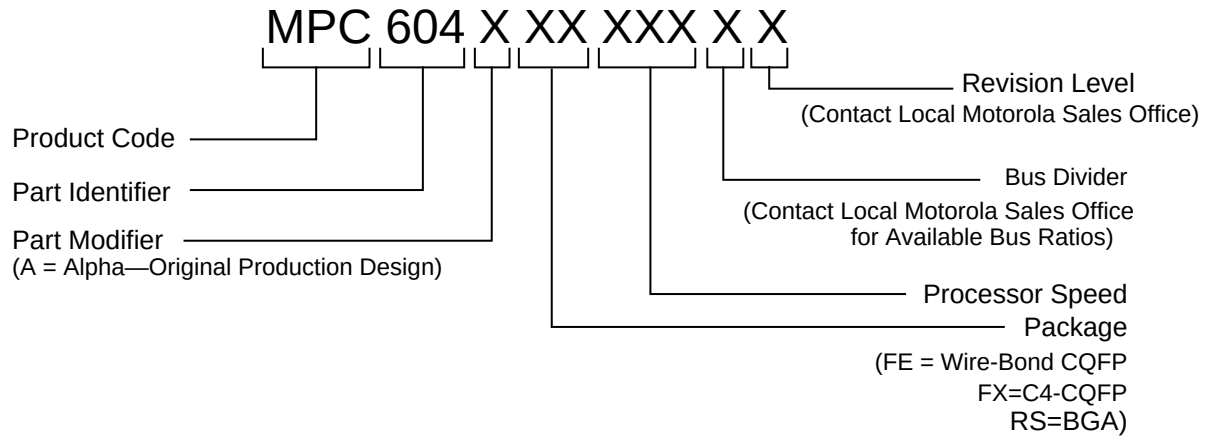


Figure 20. Motorola Part Number Key

1.7.2 IBM Part Number Key

Figure 16 provides the IBM part numbering nomenclature for the 604.

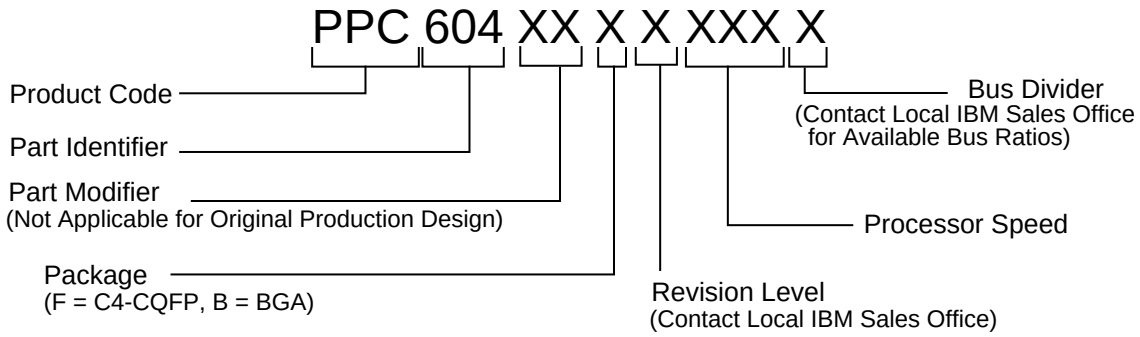


Figure 21. IBM Part Number Key

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