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PowerPC™

Advance Information

PowerPC 601™ RISC Microprocessor Hardware Specifications

The PowerPC 601 microprocessor is the first implementation of the PowerPC™ family of reduced instruction set computer (RISC) microprocessors. This document contains pertinent physical characteristics of the 601 and 601v. For functional characteristics of the processor, refer to the *PowerPC 601 RISC Microprocessor User's Manual*.

This document contains the following topics:

In this document, the terms PowerPC 601 RISC microprocessor, 601, and 601v are used to denote the first microprocessor from the PowerPC Architecture™ family. The PowerPC 601 microprocessors are available from IBM as PPC601 and from Motorola as MPC601.

IBM Microelectronics

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1.1 PowerPC 601 Microprocessor Overview

The 601 is the first implementation of the PowerPC family of RISC microprocessors. The 601 implements the 32-bit portion of the PowerPC architecture, which provides 32-bit effective addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits. For 64-bit PowerPC implementations, the PowerPC architecture provides 64-bit integer data types, 64-bit addressing, and other features required to complete the 64-bit architecture.

The 601 is a superscalar processor capable of issuing and retiring three instructions per clock, one to each of three execution units. Instructions can complete out of order for increased performance; however, the 601 makes execution appear sequential.

The 601 integrates three execution units—an integer unit (IU), a branch processing unit (BPU), and a floating-point unit (FPU). The ability to execute three instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for 601-based systems. Most integer instructions execute in one clock cycle. The FPU is pipelined so a single-precision multiply-add instruction can be issued every clock cycle.

The 601 provides an on-chip, 32-Kbyte, eight-way set-associative, physically addressed, unified instruction and data cache and an on-chip memory management unit (MMU). The MMU contains a 256-entry, two-way set-associative, unified translation lookaside buffer (UTLB) and provides support for demand-paged virtual memory address translation and variable-sized block translation. Both the UTLB and the cache use least recently used (LRU) replacement algorithms.

The 601 has a 64-bit data bus and a 32-bit address bus. The 601 interface protocol allows multiple masters to compete for system resources through a central external arbiter. Additionally, on-chip snooping logic maintains cache coherency in multiprocessor applications. The 601 supports single-beat and burst data transfers for memory accesses; it also supports both memory-mapped I/O and direct-store addressing.

The 601 uses an advanced CMOS (complementary metal-oxide semiconductor) process technology and maintains full interface compatibility with TTL devices. The 601v is functionally equivalent to the 601, but operates with reduced internal voltages and with reduced power dissipation.

1.1.1 PowerPC 601 Microprocessor Features

Major features of the 601 and 601v are as follows:

- High-performance, superscalar microprocessor
  - — As many as three instructions in execution per clock (one to each of the three execution units)
  - — Single clock cycle execution for most instructions
  - — Pipelined FPU for all single-precision and most double-precision operations
- Three independent execution units and two register files
- High instruction and data throughput
  - — Zero-cycle branch capability
  - — Programmable static branch prediction on unresolved conditional branches
  - — Instruction unit capable of fetching eight instructions per clock from the cache
  - — An eight-entry instruction queue that provides lookahead capability
  - — Interlocked pipelines with feed-forwarding that control data dependencies in hardware
  - — Unified 32-Kbyte cache—eight-way set-associative, physically addressed; LRU replacement algorithm

  - — Memory unit with a two-element read queue and a three-element write queue
  - — Run-time reordering of loads and stores
  - — Address translation facilities for 4-Kbyte page size, variable block size, and 256-Mbyte segment size
  - — A 256-entry, two-way set-associative UTLB
  - — Four-entry BAT array providing 128-Kbyte to 8-Mbyte blocks
  - — Four-entry, first-level ITLB
  - — Hardware table search (caused by UTLB misses) through hashed page tables
  - — 52-bit virtual address; 32-bit physical address
- Facilities for enhanced system performance
  - — Bus interface can run at integer factor of operating frequency
  - — A 64-bit split-transaction external data bus with burst transfers
  - — Support for address pipelining and limited out-of-order bus transactions
  - — Snooped copy-back queues for cache block (sector) copy-back operations
  - — Bus extensions for I/O controller interface operations
  - — Multiprocessing support features that include the following:
    - – Hardware enforced, four-state cache coherency protocol (MESI)
    - – Separate port into cache tags for bus snooping

1.2 General Parameters

Table 1 provides a summary of the general parameters of the 601 and 601v.

Table 1. General Parameters of the PowerPC 601 Microprocessor

Characteristic	50, 66, 80 MHz	100 MHz (601v)
Technology	0.65 μm CMOS 4-level metal	0.5 μm CMOS 5-level metal
Package	304-pin C4FP Surface mount	304-pin C4FP Surface mount
Power supplies	3.6 V (5%)	2.5 V ± 5% (core) 5.0 V ± 5% (I/O)
Chip size	10.95 mm x 10.95 mm	8.6 mm x 8.6 mm
Maximum input rating	Chip can sustain 50 mA into any pin.	Chip can sustain 50 mA into any pin.

The “v” in 601v denotes that this processor operates at different power supply voltages than other versions of the 601.

1.3 PowerPC 601 Microprocessor Electrical Specifications

This section provides both the AC and DC electrical specifications for the 601 and 601v. The following specifications are preliminary and subject to change without notice.

1.3.1 PowerPC 601 Microprocessor DC Electrical Characteristics

Table 2 provides the maximum ratings for the 601 and 601v.

Table 2. Maximum Ratings

Rating	Symbol	Value		Unit
601 and 601v chip performance	F_{max}	50, 66, 80	100 (601v)	MHz
Supply voltage (core logic)	Vdd_{INT}	3.9	2.9	V
Supply voltage (I/O circuits)	$Vdd_{I/O}$	3.9	5.5	V
Input voltage ($Vdd_{I/O}$ = 3.6 V)	V_{in}	$Vdd_{I/O}$ + 2.1	—	V
Input voltage ($Vdd_{I/O}$ = 5.0 V)	V_{in}	—	$Vdd_{I/O}$ + 0.7	V
Maximum operating junction temperature	T_j	TBD	TBD	°C
Operating junction temperature range for AC specs	T_j	10 to 85	10 to 85	°C
Storage temperature range	T_{stg}	1 °C to 60 °C, 5% to 80% relative humidity		°C

Note: The 601v (100 MHz) requires two power supplies—Vdd_{INT} and $Vdd_{I/O}$. The $Vdd_{I/O}$ level should not exceed the Vdd_{INT} level by 2.5 volts. Vdd_{INT} should not be raised greater than 0.5 volts above $Vdd_{I/O}$. It is recommended that $Vdd_{I/O}$ and Vdd_{INT} be brought up and powered down simultaneously.

Table 3 provides the DC electrical characteristics for the 601 and 601v.

Table 3. DC Electrical Characteristics

Characteristic	Notes	Symbol	Min	Max	Unit
Input high voltage		V_{IH}	2	5.5	V
Input low voltage		V_{IL}	GND	0.8	V
Input leakage current $GND < V_{in} < Vdd_{I/O}$ + 1.0 V $Vdd_{I/O}$ + 1.0 V < V_{in} < $Vdd_{I/O}$ + 1.9 V	$Vdd_{I/O}$ = 3.6 V Note 1	 I_{in} I_{in}	 — —	 10 100	 µA µA
Input leakage current (601v) $GND < V_{in} < Vdd_{I/O}$ + 0.6 V	$Vdd_{I/O}$ = 5.0 V Note 1	I_{in}	—	10	µA
Hi-Z (off-state) leakage current (601—50, 66, 80 MHz) $GND < V_{in} < Vdd_{I/O}$ $Vdd_{I/O} < V_{in} < Vdd_{I/O}$ + 0.6 V $Vdd_{I/O}$ + 0.6 V < V_{in} < $Vdd_{I/O}$ + 1.9 V	@ 85 °C T_j $Vdd_{I/O}$ = 3.6 V Note 2	 I_{TSI} I_{TSI} I_{TSI}	 — — —	 10 1000 100	 µA µA µA

Table 3. DC Electrical Characteristics (Continued)

Characteristic	Notes	Symbol	Min	Max	Unit
Hi-Z (off-state) leakage current (601—100 MHz) $GND<V_{in}<Vdd_{I/O}$ $Vdd_{I/O}<V_{in}<Vdd_{I/O}+0.25$ V	@ 85 °C T_j $Vdd_{I/O}$ = 5.0 V	 I_{TSI} I_{TSI}	 — —	 10 1000	 µA µA
Signal input current V_{IL} = 0.8 V and V_{IH} = 2.0 V		I_{IL}, I_{IH}	—	100	µA
Output high voltage I_{OH} = –10 mA or I_{OH} = –20 mA (SC_DRIVE enabled)		V_{OH}	2.4	—	V
Output low voltage (601—50, 66, 80 MHz) I_{OL} = 10 mA I_{OL} = 20 mA (SC_DRIVE enabled)	 Note 3	 V_{OL} V_{OL}	 — —	 0.45 0.55	 V V
Output low voltage (601—100MHz) I_{OL} = 10 mA I_{OL} = 20 mA (SC_DRIVE enabled)	 Note 3	 V_{OL} V_{OL}	 — —	 0.50 0.60	 V V
2X_PCLK input low voltage	Note 4	V_{il2XP}	0	0.6	V
2X_PCLK input high voltage	Note 4	V_{ih2XP}	1.8	5.5	V
Capacitance[5] V_{in} = 0 V, f = 1 MHz F_{max} = 50, 66, and 80 MHz F_{max} = 100 MHz	 Note 5	 C_{in} C_{in}	 — —	 10 15	 pF pF
Power dissipation (ambient)	50 MHz	P_D	—	5.6 (Typical) 6.5 (Worst case)	W
Power dissipation (ambient)	66 MHz	P_D	—	7.0 (Typical) 8.2 (Worst case)	W
Power dissipation (ambient)	80 MHz	P_D	—	8.0 (Typical) 9.2 (Worst case)	W
Power dissipation (ambient)	100 MHz Note 6	P_D	—	4.0 (Typical) 6.0 (Worst case)	W
Vdd_{INT} average power supply current	100 MHz	Idd_{INT}		1835 (Worst case)	mA
$Vdd_{I/O}$ average power supply current	100 MHz	$Idd_{I/O}$		180 (Worst case)	mA

Notes:

1. The 601v (100 MHz) requires 5.0 V $Vdd_{I/O}$, and will not operate properly at 3.6 V. The 601 (50, 66, and 80 MHz) requires a common supply of 3.6 V for both Vdd_{INT} and $Vdd_{I/O}$.
2. Not applicable when $Vdd_{I/O}$ = 5.0 V (601v, 100 MHz)
3. Double drive (I_{OH} and I_{OL} = 20 mA) is only available for the following signals—$\overline{DBB}$, $\overline{ABB}$, $\overline{TS}$, $\overline{XATS}$, $\overline{ARTRY}$, and $\overline{SHD}$, and is enabled by asserting SC_DRIVE.
4. Unique 2X_PCLK input voltages only apply for a 601v (100 MHz) processor.
5. Capacitance is periodically sampled rather than 100% tested.
6. Typical power dissipation measured at Vdd_{INT} = 2.5 V, $Vdd_{I/O}$ = 5.0 V while running SPECfp92 suite. System thermal designs should accommodate worst case power dissipation.

1.3.2 PowerPC 601 Microprocessor AC Electrical Characteristics

This section provides the AC electrical characteristics for the 601 and 601v.

1.3.2.1 Input AC Specifications

Table 4 provides the clock AC timing specifications as defined in Figure 1.

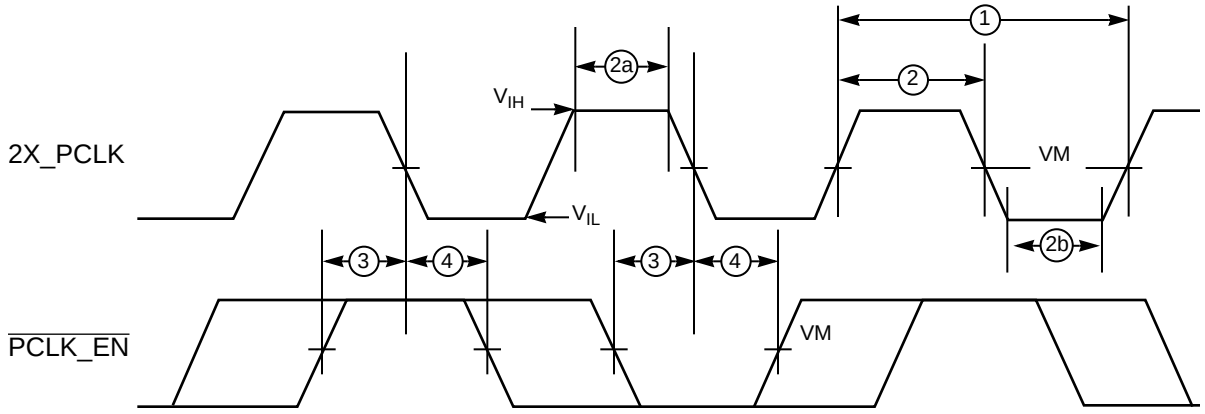
Table 4. Clock AC Timing Specifications

$Vdd_{I/O}$ = Nominal ± 5%, Vdd_{INT} = 3.6 V ± 5% or 2.5 V ± 5% V (601v, 100 MHz), GND = 0 V dc, T_j MAX = 85 °C

Num	Characteristic	50 MHz		66 MHz		80 MHz		100 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
	Frequency of operation	rtc[1]	50	rtc[1]	66	rtc[1]	80	rtc[1]	100	MHz
	2X_PCLK rising edge jitter	—	—	—	—	—	—	—	±150[2]	ps
1	2X_PCLK cycle time	10	—	7.5	—	6.25	—	5.0	—	ns
2/1	2X_PCLK duty cycle measured at 1.4 V	35	65	35	65	35	65	40	60	%
2a	2X_PCLK minimum pulse width at 1.8 V	—	—	—	—	—	—	1.45[3]	—	ns
2b	2X_PCLK minimum pulse width at 0.6 V	—	—	—	—	—	—	1.27[3]	—	ns
3	$\overline{\text{PCLK\_EN}}$ setup to falling edge of 2X_PCLK	0.8[4]	—	0.7[4]	—	0.7[4]	—	0.7[4]	—	ns
4	$\overline{\text{PCLK\_EN}}$ hold from falling edge of 2X_PCLK	1.8[4]	—	1.8[4]	—	1.5[4]	—	1.5[4]	—	ns

Notes: 1. Actual minimum gated by real time clock frequency

2. Maximum allowable sum of cycle-to-cycle or long-term jitter
3. Guaranteed by design/characterization
4. $\overline{\text{PCLK\_EN}}$ is measured from the 1.4 V level of the signal in question to the 1.4 V level of the input 2X_PCLK.



Notes: V_{IH} = 2.0 V, V_{IL} = 0.8 V. For the 2X_PCLK of the 601v (100 MHz), V_{IH} = 1.8 V, V_{IL} = 0.6 V.
The timing diagram should only be referenced in regard to the edge-to-edge measurement of the timing specifications. It is not intended as a functional description of the input and output signals. Refer to the *PowerPC 601 RISC Microprocessor User's Manual* for functional descriptions and their related diagrams for device operation.

Figure 1. PowerPC 601 Microprocessor Clock Input Timing Diagram

Table 5 provides the input AC timing specifications as defined in Figure 2.

Table 5. Input AC Timing Specifications

$Vdd_{I/O}$ = Nominal ± 5%, Vdd_{INT} = 3.6 V ± 5% or 2.5 V ± 5% V (601v, 100 MHz), GND = 0 V dc, T_j MAX = 85 °C

Num	NOTE	Characteristic	50 MHz		66 MHz		80 MHz[5]		100 MHz[6] (601v)		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
9.0	1	$\overline{\text{BCLK\_EN}}$ setup to rising edge of 2X_PCLK (qualified with $\overline{\text{PCLK\_EN}}$ being low)	14	—	10	—	7.7	—	7.8	—	ns
10.0	1	$\overline{\text{BCLK\_EN}}$ hold from rising edge of 2X_PCLK (qualified with $\overline{\text{PCLK\_EN}}$ being low)	0.0	—	0.0	—	0.0	—	0.0	—	ns
9.1	1,2	Input setup to rising edge of 2X_PCLK for the following signals: $\overline{\text{ARTRY}}$, $\overline{\text{DBWO}}$, $\overline{\text{TS}}$, $\overline{\text{XATS}}$.	2.7	—	2.5	—	2.7	—	2.7	—	ns
10.1	1,2	Input hold from rising edge of 2X_PCLK for the following signals: $\overline{\text{ARTRY}}$, $\overline{\text{DBWO}}$, $\overline{\text{TS}}$, $\overline{\text{XATS}}$	1.8	—	1.5	—	1.8	—	1.8	—	ns
9.2	1,2	Input setup to rising edge of 2X_PCLK for the following signals: $\overline{\text{ABB}}$, $\overline{\text{AACK}}$, $\overline{\text{BG}}$, $\overline{\text{TA}}$, $\overline{\text{DBB}}$, $\overline{\text{DBG}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TEA}}$	2.7	—	2.5	—	2.7	—	2.7	—	ns
10.2	1,2	Input hold from rising edge of 2X_PCLK for the following signals: $\overline{\text{ABB}}$, $\overline{\text{AACK}}$, $\overline{\text{BG}}$, $\overline{\text{TA}}$, $\overline{\text{DBB}}$, $\overline{\text{DBG}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TEA}}$	1.8	—	1.5	—	1.8	—	1.8	—	ns

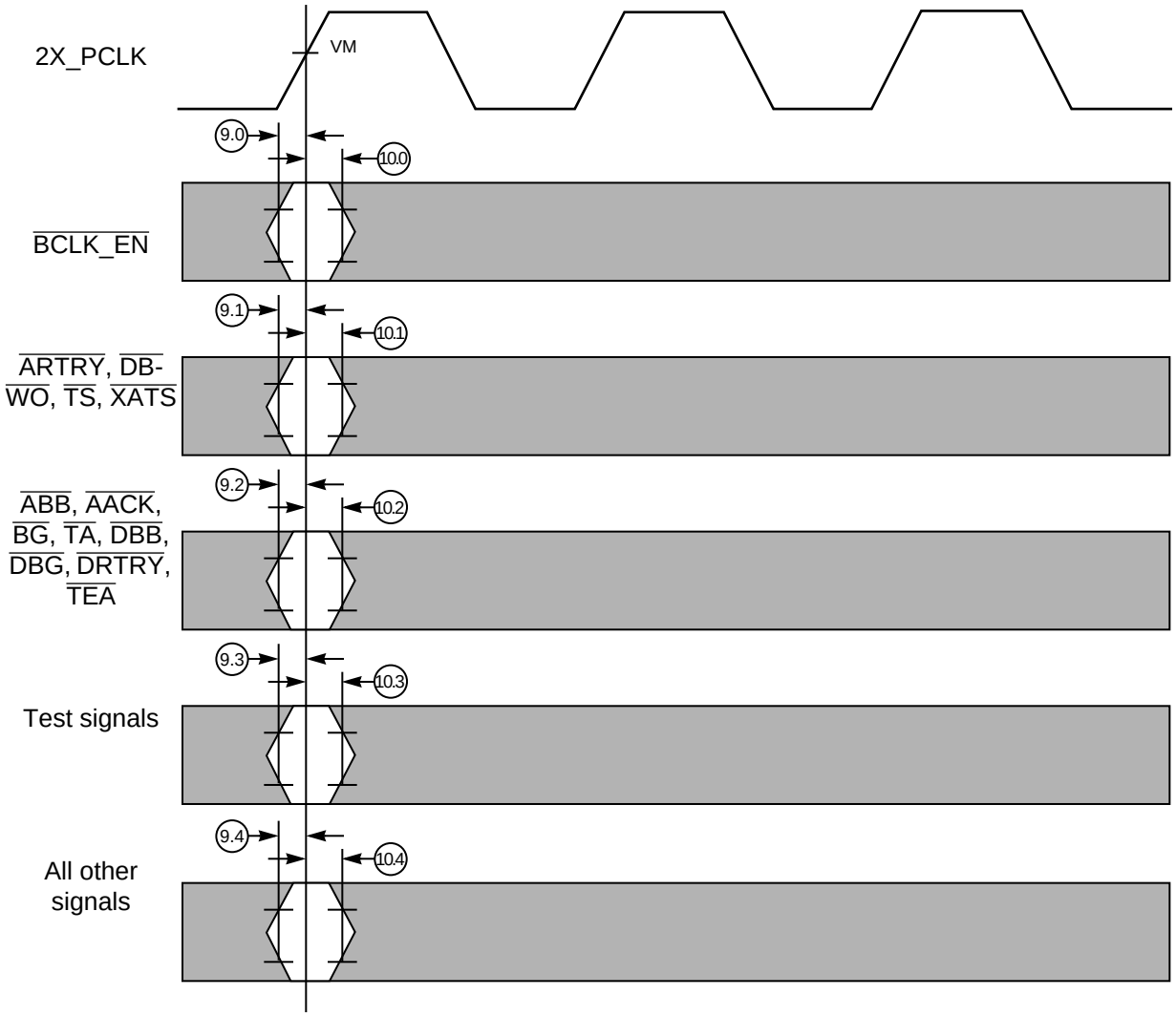
Table 5. Input AC Timing Specifications (Continued)

$Vdd_{I/O}$ = Nominal ± 5%, Vdd_{INT} = 3.6 V ± 5% or 2.5 V ± 5% V (601v, 100 MHz), GND = 0 V dc, T_j MAX = 85 °C

Num	NOTE	Characteristic	50 MHz		66 MHz		80 MHz[5]		100 MHz[6] (601v)		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
9.3	1,3	Input setup to rising edge of 2X_PCLK for test signals	2.5	—	2.5	—	2.5	—	2.5	—	ns
10.3	1,3	Input hold from rising edge of 2X_PCLK for test signals	4.0	—	3.5	—	4.0	—	4.0	—	ns
9.4	1,2,4	Input setup to rising edge of 2X_PCLK for all other signals	2.5	—	2.5	—	2.5	—	2.5	—	ns
10.4	1,2,4	Input hold from rising edge of 2X_PCLK for all other signals	2.0	—	1.7	—	2.0	—	2.0	—	ns

Input AC timing notes:

1. All input specs are measured from the TTL level of the signal in question to the 1.4 V level of the input 2X_PCLK rising edge, except for $\overline{\text{PCLK\_EN}}$.
2. Input setup and hold times are measured relative to the bus transition point. An internal clock phase is generated by having the $\overline{\text{PCLK\_EN}}$ negated and then asserted on two consecutive falling edges of the 2X_PCLK. On the assertion of this internal clock, if the $\overline{\text{BCLK\_EN}}$ is asserted, then a bus transition will occur on the next rising edge of the 2X_PCLK.
3. Test signals include: $\overline{\text{SYS\_QUIESC}}$, RESUME, SCAN_CTL, SCAN_CLK, and SCAN_SIN.
4. Signals included are: TSIZ0–TSIZ2, $\overline{\text{TBST}}$, $\overline{\text{GBL}}$, TT0–TT3, A0–A31, AP0–AP3, DH0–DH31, DL0–DL31, DP0–DP7, and $\overline{\text{SHD}}$.
5. This specification is for an 80-MHz processor with the interface running at half the processor frequency (40 MHz).
6. This specification is for a 100-MHz 601v processor with the interface running at half the processor frequency (50 MHz).



Notes: 1. The timing diagram should only be referenced in regard to the edge-to-edge measurement of the timing specifications. It is not intended as a functional description of the input and output signals. Refer to the *PowerPC 601 RISC Microprocessor User's Manual* for functional descriptions and their related diagrams for device operation.

2. VM = Midpoint voltage (1.4 V)

Figure 2. PowerPC 601 Microprocessor Input Timing Diagram

1.3.2.2 Output AC Specifications

The output specifications of the 601 and 601v for both driving high and driving low depend on the capacitive loading on each output and the drive capability enabled for that output. Additionally, the timing specifications for outputs driving low depend on the voltage swing required to drive to 0.8 V (either 5.5–0.8 V or 3.6–0.8 V).

Table 7 provides the output AC timing specifications (shown in Figure 3) as absolute values for a theoretical 0 pF load. In order to derive the actual timing specifications guaranteed for a given set of conditions (capacitive loading, drive capability, and voltage swing), the loading factors provided in Table 6 must be used. The actual specifications are defined as follows:

$t_{pd\ (actual)} = t_{table} + (\text{loading factor} * C_{load})$

where:

$t_{pd\ (actual)}$ = the specification guaranteed
t_{table} = the value from Table 7
C_{load} = the capacitive loading on that signal in the system **(minimum of 20 pF must be used)**

For example, if an output buffer for a 50-MHz device is driving a load of 100 pF, the output propagation delay, due to the capacitive load, driving high would be calculated as follows:
$t_{pd\ (actual)}$ = 10.5 ns + (100 pF * 0.047 ns/pF) = 15.2 ns.

Table 6. Loading Factors for Output Signals

Loading Factor for Selected Buffer Size	50 MHz		66 MHz		80 MHz		100 MHz (601v)	
	Normal[1]	Double[2]	Normal[1]	Double[2]	Normal[1]	Double[2]	Normal[1]	Double[2]
Driving low (5.5 V to 0.8 V)	0.088	0.053	0.080	0.048	0.072	0.043	0.072	0.039
Driving low (3.6 V to 0.8V)	0.060	0.036	0.055	0.033	0.051	0.030	0.049	0.029
Driving high (0.0 V to 2.0 V)	0.047	0.028	0.042	0.025	0.037	0.022	0.035	0.018

Notes: 1. Normal mode means that SC_DRIVE is negated.
2. Double drive is only available for the following signals: $\overline{ABB}$, $\overline{DBB}$, $\overline{SHD}$, $\overline{ARTRY}$, $\overline{TS}$, and $\overline{XATS}$. Double drive is enabled by strapping the SC_DRIVE pin to Vdd. (Double drive mode increases the capacitive drive capability of the signal by enabling a second driver.)

Table 7. Output AC Timing Specifications (Theoretical 0 pF load)

$Vdd_{I/O}$ = Nominal ± 5%, Vdd_{INT} = 3.6 V ± 5% or 2.5 V ± 5% V (601v, 100 MHz), GND = 0 V dc, T_j MAX = 85 °C
Actual specifications must be derived for a minimum of 20 pF capacitive load (see Table 6).

Num	Note	Characteristic	50 MHz		66 MHz		80 MHz[8]		100 MHz[9] (601v)		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
20.0	1–4, 7	2X_PCLK rising edge to $\overline{SHD}$, $\overline{ARTRY}$, $\overline{ABB}$, $\overline{DBB}$, $\overline{TS}$, $\overline{XATS}$ output driven (output enable time)	3	—	3	—	3	—	1.9	—	ns
20.1	1, 7	2X_PCLK rising edge to all other outputs driven (output enable time)	3	—	3	—	3	—	1.9	—	ns
21.0	1–4	2X_PCLK rising edge to $\overline{SHD}$, $\overline{ARTRY}$, $\overline{ABB}$, $\overline{DBB}$, $\overline{TS}$, $\overline{XATS}$ output valid	—	8.5	—	7.5	—	8.5	—	8.5	ns
21.1	1	2X_PCLK rising edge to all other outputs valid	—	10.5	—	8.5	—	10.5	—	10.5	ns
22.0	1, 2, 5, 7	2X_PCLK to $\overline{TS}$, $\overline{XATS}$ output invalid (output hold)	3	—	3	—	3	—	1.6	—	ns
22.1	1, 7	2X_PCLK to all other outputs invalid (output hold)	3	—	3	—	3	—	1.2	—	ns
23.0	1, 2, 5	2X_PCLK rising edge to $\overline{TS}$, $\overline{XATS}$ output high impedance	—	8.5	—	7.5	—	8.5	—	8.5	ns
23.1	1	2X_PCLK rising edge to all other outputs high impedance	—	10.5	—	8.5	—	10.5	—	10.5	ns
24	1–3	2X_PCLK rising edge to $\overline{SHD}$, $\overline{ARTRY}$ precharge enable	1	8.5	1	7.5	1	8.5	0.7	8.5	ns
25	1–3	2X_PCLK rising edge to $\overline{SHD}$, $\overline{ARTRY}$ precharge disable	—	21.0	—	16.0	—	21.0	—	21.0	ns
26, 29	5	Width of precharge for $\overline{SHD}$, $\overline{ARTRY}$, $\overline{ABB}$, $\overline{DBB}$	11	—	9	—	7	—	6.0	—	ns

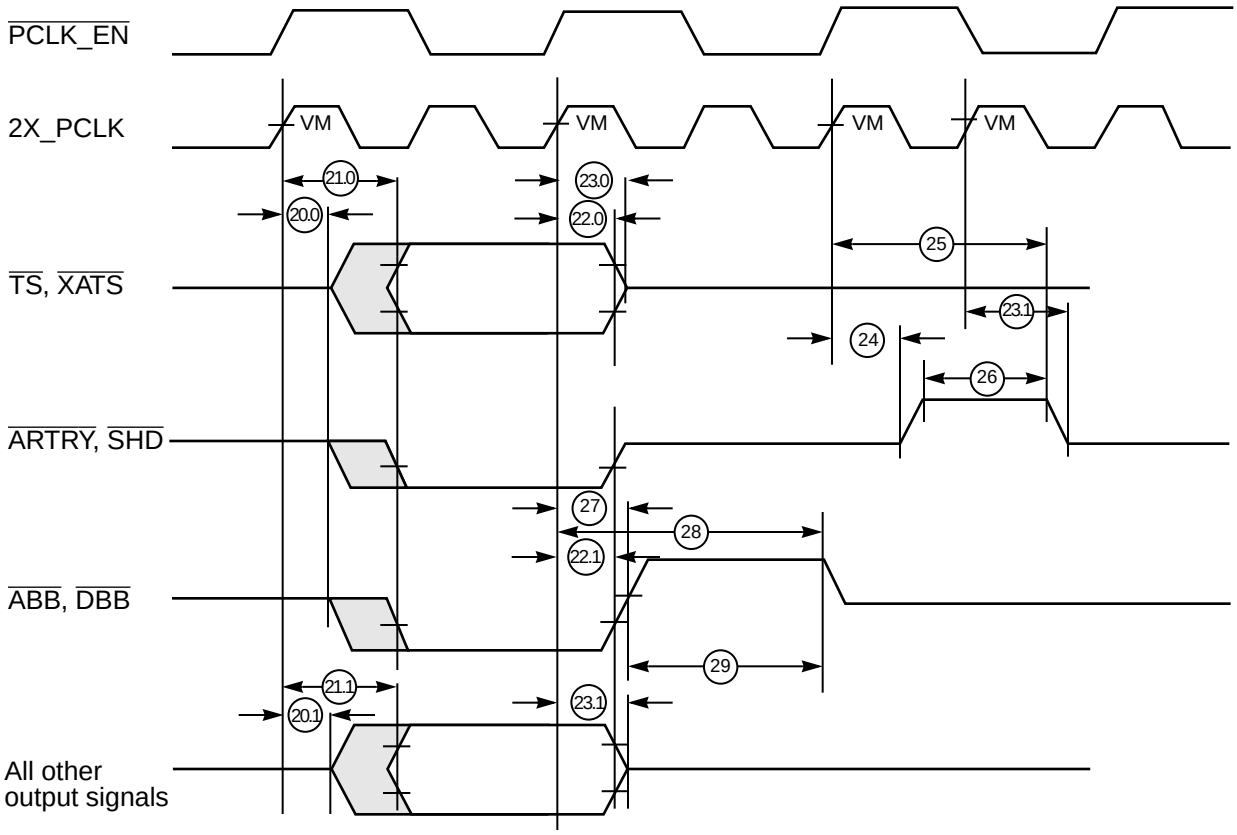
Table 7. Output AC Timing Specifications (Theoretical 0 pF load) (Continued)

$Vdd_{I/O}$ = Nominal ± 5%, Vdd_{INT} = 3.6 V ± 5% or 2.5 V ± 5% V (601v, 100 MHz), GND = 0 V dc, T_j MAX = 85 °C
Actual specifications must be derived for a minimum of 20 pF capacitive load (see Table 6).

Num	Note	Characteristic	50 MHz		66 MHz		80 MHz[8]		100 MHz[9] (601v)		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
27	1–2, 7	2X_PCLK rising edge to $\overline{ABB}$, $\overline{DBB}$ precharge enable	3	8.5	3	7.5	3	8.5	1.9	8.5	ns
28	6	2X_PCLK rising edge to $\overline{ABB}$, $\overline{DBB}$ disable	—	21.0	—	16	—	21.0	—	21.0	ns

Output AC timing notes:

1. All output specs are measured from the 1.4 V level of the 2X_PCLK input to the TTL level of the signal in question. Note that functional timing is derived from the rising edge of 2X_PCLK gated by $\overline{PCLK\_EN}$ and $\overline{BCLK\_EN}$, as described above.
2. The shared outputs $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, $\overline{SHD}$, $\overline{ARTRY}$, and $\overline{XATS}$ signals require pull-up resistors to hold them negated when there is no bus master driving.
3. Because $\overline{SHD}$ and $\overline{ARTRY}$ may be asserted by more than one device at the same time, they are negated in a unique fashion. They are tri-stated in the second bus clock cycle after $\overline{AACK}$ assertion. In the next cycle, they are precharged for one 2X_PCLK period regardless of $\overline{BCLK\_EN}$. This protocol prevents driver contention on these signals. This precharge may be disabled by setting HID0 (bit 29).
4. Double drive is only available for the following signals: $\overline{ABB}$, $\overline{DBB}$, $\overline{SHD}$, $\overline{ARTRY}$, $\overline{TS}$, and $\overline{XATS}$. Double drive is enabled by strapping the SC_DRIVE pin to Vdd. (Double drive mode increases the capacitive drive capability of the signal by enabling a second driver.)
5. If the chip is operated at a frequency less than that which is specified, the width of precharge will be approximately one 2X_PCLK period plus 1 ns.
6. $\overline{ABB}$ and $\overline{DBB}$ disable assumes continuous clock operation. If clock operations are stopped, the disable may extend until clock operations are restarted.
7. Minimum output enable and output hold times are guaranteed by design.
8. This specification is for an 80-MHz processor with the interface running at half the processor frequency (40 MHz).
9. This specification is for a 100-MHz 601v processor with the interface running at half the processor frequency (50 MHz).



Note: The diagram should only be referenced in regard to the edge-to-edge measurement of the timing specifications. It is not intended as a functional description of the input and output signals. Refer to the *PowerPC 601 RISC Microprocessor User's Manual* for functional descriptions and their related diagrams for device operation.

Figure 3. PowerPC 601 Microprocessor Output Timing Diagram

1.4 PowerPC 601 Microprocessor Thermal Management Information

This section provides thermal management information for the 601 and 601v.

The 601 will meet its electrical specifications when operated at a maximum T_j (junction temperature) of 85 ^oC. To ensure that the processor does not exceed its maximum operating temperature, the proper heat sink and heat sink interface material must be selected. Table 8 provides θ_{JH} (thermal resistance from junction to heat sink) for three typical heat sink to chip interfaces. Note that θ_{jH} is dependent on the chip size.

Table 8. θ_{JH} for Three Typical Heat Sink to Chip Interfaces

Chip Size	θ_{jH} #1	θ_{jH} #2	θ_{jH} #3	$\theta_{constriction}$
10.95 x 10.95 mm—(601)	0.95 °C/Watt	2.9 °C/Watt	0.66 °C/Watt	0.2 °C/Watt
8.6 x 8.6 mm—(601v)	1.54 °C/Watt	4.7 °C/Watt	1.07 °C/Watt	0.3 °C/Watt

θ_{JH} #1 is 0.038 inches of AI Epoxy, k-1.06 W/mK with 80% coverage
θ_{JH} #2 is Chomerics tape, 0.139 mm thick, k = 0.4 W/mK, 100% coverage
θ_{JH} #3 is 0.003 inches of Thermoset grease, k =1.2 W/mK, 80% coverage

1.4.1 Heat Sink Selection

Estimate the required heat sink performance using the following expression:

$$\theta_{HA} = [((T_j - T_a) / P) - \theta_{JH} - \theta_{const}] / cf$$

Where:

θ_{HA} = Thermal resistance from heat sink base to air
T_j = Junction temperature—maximum = 85 °C
P = Device power dissipation (see Table 3)
θ_{JH} = Thermal resistance from junction to heat sink
θ_{const} = Constriction resistance into heat sink
cf = Altitude correction factor (7000 ft. elevation)
T_a = Ambient temperature

For a conservative sizing, the maximum values of T_j, T_a, and power (P) should be used in the above expression. A more accurate sizing can be made by taking into account the statistical variation of these variables. However, that type of analysis is beyond the scope of this reference.

1.4.2 Thermal Management Example

The following example provides the information necessary to make a heat sink selection. For a typical desktop application which uses an 80-MHz 601 (8 W typical, 9.2 W worst case power) and has a maximum ambient air temperature of 40 ^{o}C, the allowable thermal resistance of the heat sink (θ_{HA}) can be determined.

Thermal resistance (junction to case) = θ_{JH} = 0.95 °C/Watt (junction to case)
(assuming AI epoxy interface)
Maximum T_j (junction temperature) = 85 ^{o}C
Maximum ambient air temperature T_a = 40 ^{o}C
cf = 1.15 (correction factor for 7000-ft. elevation)

θ_{HA} = [((T_j – T_a) / chip power) – θ_{JH} – $\theta_{constriction}$] x 1/cf
θ_{HA} = [((85 ^{o}C – 40 ^{o}C)/ 9.2 W) – 0.95 °C/Watt – 0.2 °C/Watt)] x 1/1.15
θ_{HA} = 3.25 °C/Watt (It is the maximum thermal resistance of the heat sink required to maintain 85 ^{o}C maximum junction temperature.)

1.4.3 Estimation of T_j

Factors such as air-ducting and preheating can significantly affect the thermal performance of the processor. As such, the processor operating temperature should be verified for each application.

Since the processor junction temperature is not readily measurable, it is necessary to estimate this value. If the base temperature of the heat sink is known, the relationship to junction temperature can be easily derived as follows:

$$T_j = T_H + \text{Power} \times \theta_{JH}$$

where: T_H = heat sink base temperature

The heat sink base temperature can be obtained by a simple thermocouple measurement.

If the actual module power dissipation is available, this value should be substituted for chip power. Otherwise, an estimate of the nominal and maximum junction temperature can be made by substituting the nominal and maximum device power dissipation values from Table 3.

1.5 PowerPC 601 Microprocessor Pinout Diagram

Figure 4 contains the pin assignments for the 601 and 601v.

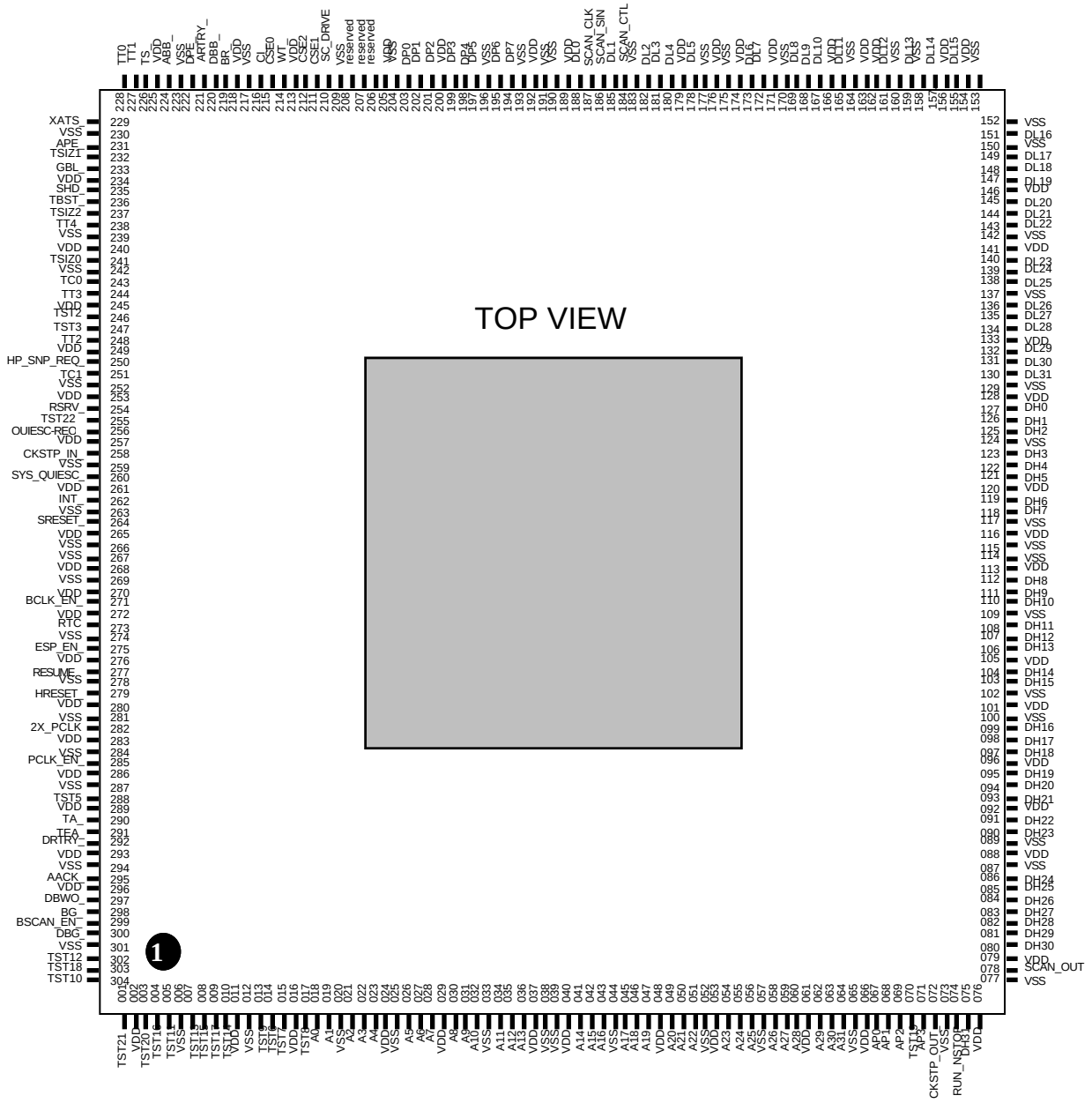


Figure 4. PowerPC 601 Microprocessor Pin Assignments

1.6 PowerPC 601 Microprocessor Pinout Listing

Table 9 provides the pinout listing for the 601 and 601v.

Table 9. PowerPC 601 Microprocessor Pinout Listing

Signal Name	Pin Number	Active	I/O
2X_PCLK	282	High	Input
A0–A31	18, 19, 21, 22, 23, 26, 27, 28, 30, 31, 32, 34, 35, 36, 41, 42, 43, 45, 46, 47, 49, 50, 51, 54, 55, 56, 58, 59, 60, 62, 63, 64	High	I/O
$\overline{\text{AACK}}$	295	Low	Input
$\overline{\text{ABB}}$	224	Low	Output
AP0–AP3	67, 68, 69, 71	High	I/O
$\overline{\text{APE}}$	231	Low	Output
$\overline{\text{ARTRY}}$	221	Low	I/O
$\overline{\text{BCLK\_EN}}$	271	Low	Input
$\overline{\text{BG}}$	298	Low	Input
$\overline{\text{BR}}$	219	Low	Output
$\overline{\text{BSCAN\_EN}}$	299	High	Input
$\overline{\text{CI}}$	216	Low	Output
$\overline{\text{CKSTP\_IN}}$	258	Low	Input
$\overline{\text{CKSTP\_OUT}}$	72	Low	Output
CSE0–CSE2	215, 211, 212	High	Output
$\overline{\text{DBB}}$	220	Low	I/O
$\overline{\text{DBG}}$	300	Low	Input
$\overline{\text{DBWO}}$	297	Low	Input
DH0–DH31	127, 126, 125, 123, 122, 121, 119, 118, 112, 111, 110, 108, 107, 106, 104, 103, 99, 98, 97, 95, 94, 93, 91, 90, 86, 85, 84, 83, 82, 81, 80, 75	High	I/O
DL0–DL31	188,185, 182, 181, 180, 178, 173, 172, 169, 168, 167, 165, 161, 159, 157, 155, 151, 149, 148, 147, 145, 144, 143, 140, 139, 138, 136, 135, 134, 132, 131, 130	High	I/O
DP0–DP7	203, 202, 201, 199, 198, 197, 195, 194	High	I/O
$\overline{\text{DPE}}$	222	Low	Output
$\overline{\text{DRTRY}}$	292	Low	Input
$\overline{\text{ESP\_EN}}$	275	Low	Input
$\overline{\text{GBL}}$	233	Low	I/O

Table 9. PowerPC 601 Microprocessor Pinout Listing (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{\text{HP\_SNP\_REQ}}$	250	Low	Input
$\overline{\text{HRESET}}$	279	Low	Input
$\overline{\text{INT}}$	262	Low	Input
$\overline{\text{PCLK\_EN}}$	285	Low	Input
QUIESC_REQ	256	High	Output
Reserved	206, 207	Tie high ($Vdd_{I/O}$)	—
Reserved	208	Tie low	—
RESUME	277	High	Input
$\overline{\text{RSRV}}$	254	Low	Output
RTC	273	High	Input
RUN_NSTOP	74	High	Output
SCAN_CLK	187	High	Input
SCAN_CTL	184	High	Input
SCAN_OUT	78	High	Output
SCAN_SIN	186	High	Input
SC_DRIVE	210	High	Input
$\overline{\text{SHD}}$	235	Low	I/O
$\overline{\text{SRESET}}$	264	Low	Input
$\overline{\text{SYS\_QUIESC}}$	260	Low	Input
$\overline{\text{TA}}$	290	Low	Input
$\overline{\text{TBST}}$	236	Low	I/O
TC0–TC1	243, 251	High	Output
$\overline{\text{TEA}}$	291	Low	Input
TSIZ0–TSIZ2	241, 232, 237	High	I/O
TST7, TST8, TST10–TST17, TST22	15, 17, 304, 5, 302, 7, 10, 8, 4, 9, 255	Tie high ($Vdd_{I/O}$)	Input
TST18, TST20, TST21, TST5, TST6, TST9	303, 3, 1, 288, 14, 13	Tie low	Input
TST19, TST2, TST3	70, 246, 247	Do not connect	Output
$\overline{\text{TS}}$	226	Low	I/O
TT0–TT4	228, 227, 248, 244, 238,	High	I/O

Table 9. PowerPC 601 Microprocessor Pinout Listing (Continued)

Signal Name	Pin Number	Active	I/O
Vdd_{INT}	2, 11, 16, 37, 53, 61, 76, 88, 92, 113, 128, 133, 162, 163, 171, 179, 189, 200, 205, 225, 240, 253, 257, 265, 268, 270, 280, 283, 293	High	Input
$Vdd_{I/O}$	24, 29, 40, 48, 66, 79, 96, 101, 105, 116, 120, 141, 146, 154, 156, 166, 174, 176, 192, 213, 218, 234, 245, 249, 261, 272, 276, 286, 289, 296	High	Input
Vss	6, 12, 20, 25, 33, 38, 39, 44, 52, 57, 65, 73, 77, 87, 89, 100, 102, 109, 114, 115, 117, 124, 129, 137, 142, 150, 152, 153, 158, 160, 164, 170, 175, 177, 183, 190, 191, 193, 196, 204, 209, 217, 223, 230, 239, 242, 252, 259, 263, 266, 267, 269, 274, 278, 281, 284, 287, 294, 301	Low	Input
$\overline{WT}$	214	Low	Output
$\overline{XATS}$	229	Low	I/O

Note: For the 50, 66, and 80 MHz versions of the 601, Vdd_{INT} and $Vdd_{I/O}$ are not implemented as separate supplies on the chip, and should be powered with the same potential.

1.7 PowerPC 601 Microprocessor Package Description

The following sections provide the package parameters and the mechanical dimensions for the 601 and 601v.

1.7.1 Package Parameters

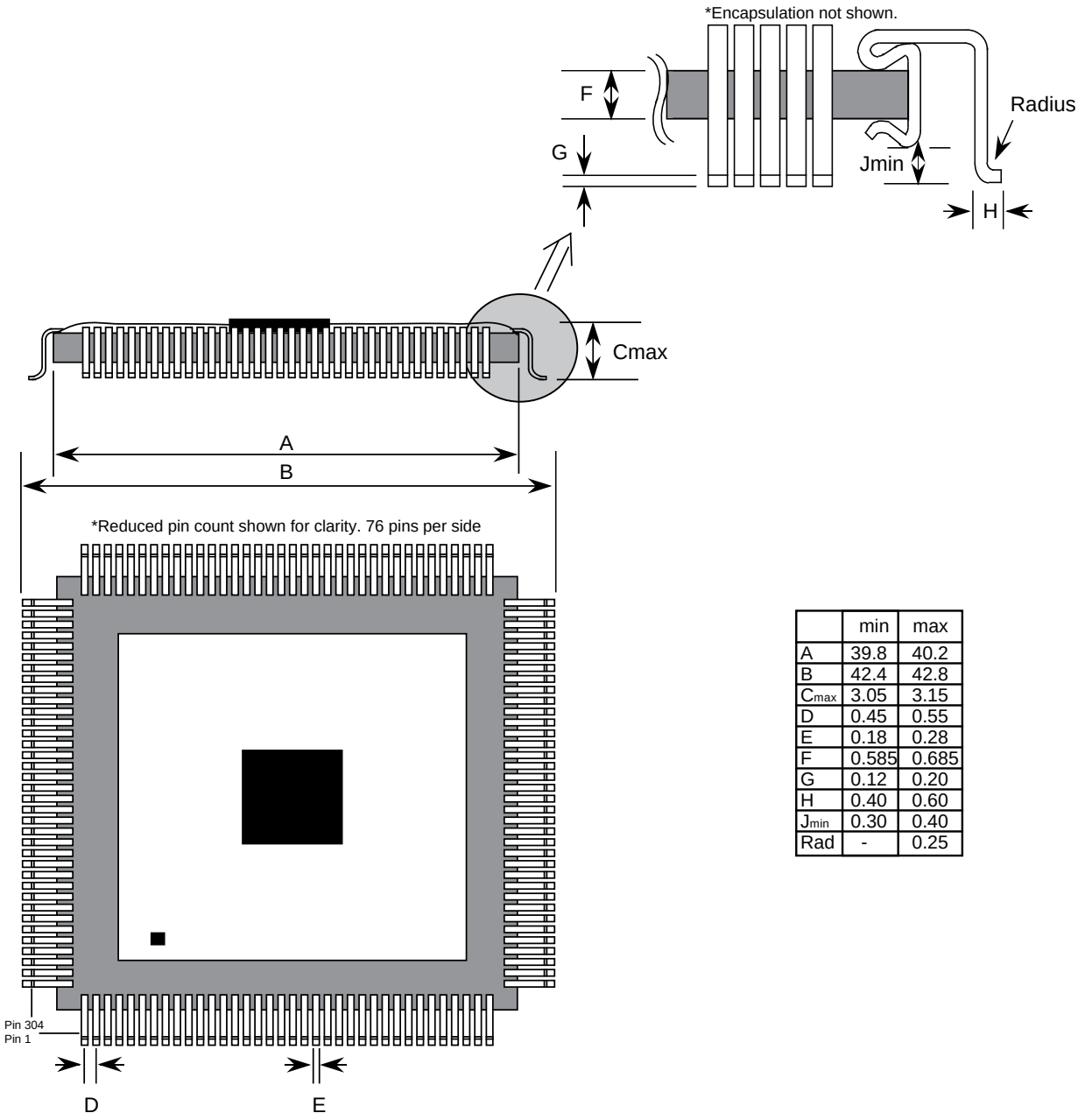
The package parameters are as provided in the following list. The package type is 40-mm, 304-pin ceramic quad flat pack.

Package outline	40 mm
Interconnects	304
Pitch	0.5 mm
Lead plating	Ni Au
Solder joint	Sn/PB (10/90)
Lead encapsulation	HYSOL 4323
C4 encapsulation	EPX 5341
Maximum module height	3.1 mm
Co-planarity specification	0.08 mm

Note: No solvent can be used with the C4FP.

1.7.2 PowerPC 601 Microprocessor Mechanical Dimensions

Figure 5 shows the mechanical dimensions for the 601 and 601v.



	min	max
A	39.8	40.2
B	42.4	42.8
C_{max}	3.05	3.15
D	0.45	0.55
E	0.18	0.28
F	0.585	0.685
G	0.12	0.20
H	0.40	0.60
J_{min}	0.30	0.40
Rad	-	0.25

*Not to scale All measurements in mm.

Figure 5. Mechanical Dimensions of the PowerPC 601 Microprocessor Package

Appendix A
General Handling Recommendations

The following list provides a few guidelines for package handling:

- Handle the electrostatic discharge sensitive (ESD) package with care before, during, and after processing.
- Do not apply any load to exceed 3 Kg after assembly.
- Components should not be hot dip tinned
- The package encapsulation is an acrylated urethane. Use adequate ventilation (local exhaust) for all elevated temperature processes.

The package parameters are as follows:

Heat sink adhesive	AIEG-7655
IBM reference drawing	99F4869
Test socket	Yamaichi IC51-3044-1543-REV C
Signal	187
Power/ground	117
Total	304

A.1 Package Environmental, Operation, Shipment, and Storage Requirements

The environmental, operation, shipment, and storage requirements are as follows:

- Make sure that the package is suitable for continuous operation under business office environments.
  - — Operating environment: 10 °C to 40 °C, 8% to 80% relative humidity
  - — Storage environment: 1 °C to 60 °C, 5% to 80% relative humidity
  - — Shipping environment: 40 °C to 60 °C, 5% to 100% relative humidity
- This component is qualified to meet JEDEC moisture Class 2
  - — After expiration of shelf life, packages may be baked at 120 °C (+10/–5 °C) for 4 hours minimum and packaged.

A.2 Card Assembly Recommendations

This section provides recommendations for card assembly process. Follow these guidelines for card assembly.

- This component is supported for aqueous, IR, convection reflow, and vapor phase card assembly processes.
- The temperature of packages should not exceed 220 °C for longer than 5 minutes.
- The package entering a cleaning cycle must not be exposed to temperature greater than that occurring during solder reflow or hot air exposure.
- It is not recommended to re-attach a package that is removed after card assembly.

A.2.1 Card Assembly Process

During the card assembly process, no solvent can be used with the C4FP, and no more than 3 Kg of force must be applied normal to the top of the package prior to, during, or after card assembly. Other details of the card assembly process follow:

Solder paste	Either water soluble (for example, Alpha 1208) or no clean
Solder stencil thickness	0.152 mm
Solder stencil aperature	Width reduced to 0.03 mm from the board pad width
Placement tool	Panasonic MPA3 or equivalent
Solder reflow	Infrared, convection, or vapor phase
Solder reflow profile	Infrared and/or convection •Average ramp-up—0.48 to 1.8 °C/second •Time above 183 °C—45 to 145 seconds •Minimum lead temperature—200 °C •Maximum lead temperature—240 °C •Maximum C4FP temperature—245 °C Vapor phase •Preheat (board)—60 °C to 150 °C •Time above 183 °C—60 to 145 seconds •Minimum lead temperature—200 °C •Maximum C4FP temperature—220 °C •Egress temperature—below 150 °C

Clean after reflow	De-ionized (D.I.) water if water-soluble paste is used •Cleaner requirements—conveyorized, in-line •Minimum of four washing chambers —Pre-clean chamber: top and bottom sprays, minimum top-side pressure of 25 psig, water temperature of 70 °C minimum, dwell time of 24 seconds minimum, water is not re-used, water flow rate of 30 liters/minute. —Wash chamber #1: top and bottom sprays, minimum top-side pressure of 48 psig, minimum bottom-side pressure of 44 psig, water temperature of 62.5 °C (±2.5 °C), dwell time of 48 seconds minimum, water flow rate of 350 liters/minute. —Wash chamber #2: top and bottom sprays, minimum top-side pressure of 32 psig, minimum bottom-side pressure of 28 psig, water temperature of 72.5 °C (±2.5 °C), dwell time of 48 seconds minimum, water flow rate of 325 liters/minute. —Final rinse chamber: top and bottom sprays, minimum top-side pressure of 25 psig, water temperature of 72.5 °C minimum, dwell time of 24 seconds minimum, water flow rate of 30 liters/minute. •No cleaning required if “no clean solder paste” is used
Touch-up and repair	Water soluble (for example, Kester 450) or No Clean Flux
C4FP removal	Hot air rework
C4FP replace	Hand solder

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