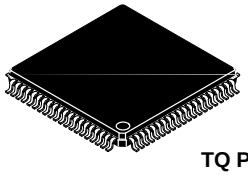
MPC27T416

Advance Information

16K x 16 Bit Cache Tag RAM for PowerPC™ Processors



TQ PACKAGE
TQFP
CASE 917A–02

The MPC27T416 is a 262,144 bit cache–tag static RAM designed to support PowerPC microprocessors at bus speeds up to 66 MHz. It is organized as 16K words of 16 bits each and is fabricated using Motorola's high performance, silicon gate BiCMOS technology. There are fourteen common I/O tag bits and two separate I/O status bits. A 14–bit comparator is on–chip to allow fast comparison of the 14 stored tag bits with the current tag input data. An active high MATCH output is generated when the valid bit is true and these two groups of data are the same for a given address.

This high–speed MATCH signal, with t_{AVMV} times as fast as 9 ns, provides the fastest possible enabling of secondary cache accesses.

The two separate I/O status bits (VALID, DIRTY) can be configured for either dedicated or generic functionality, depending on the SFUNC input pin. With SFUNC low, the status bits are defined and used internally by the device, allowing easier determination of the validity and use of the given tag data. SFUNC high releases the defined internal status bit usage and control, allowing users to configure the status bit information to fit their system needs. A synchronous RESET pin, when held low at a rising clock edge, will reset all status bits in the array for easy invalidation of all tag addresses.

The MPC27T416 also provides the option for transfer acknowledge ($\overline{TA}$) generation within the cache tag itself, based upon MATCH, VALID bit, and other external inputs provided by the user. This can significantly simplify cache controller logic and minimize cache decision time. Match and read operations are both asynchronous in order to provide the fastest access times possible, while write operations are synchronous for ease of system timing.

The MPC27T416 uses a 5 V power supply on V_{CC} and V_{SS}, with separate V_{CCQ} pins provided for the outputs to offer compliance with both 5 V TTL and 3.3 V LVTTL logic levels. The PWRDN pin offers a low–power standby mode, which provides significant system power savings.

The MPC27T416 is offered in a space saving 80–pin thin quad flat pack (TQFP) package.

- 16K x 16 Configuration:
  - 14 Tag Bits
  - Two Status Bits (Valid and Dirty)
- Valid Bit used to Qualify Match Output
- High–Speed Address–to–Match Comparison Times – 9/10/12 ns
- TA Circuitry Included Inside the Cache–Tag for the Highest Speed Operation
- Asynchronous Read/Match Operation and Synchronous Write and Reset Operation
- Separate Write Enable Pins for Tag Bits and Status Bits
- Separate Output Enable Pins for Tag Bits, Status Bits, and $\overline{TA}$
- Synchronous RESET Pin for Invalidation of all Tag Entries
- Dual Chip Selects for Easy Depth Expansion with No Performance Degradation
- I/O Pins Both 5 V TTL and 3.3 V LVTTL Compatible with V_{CCQ} Pins
- PWRDN Pin to Place Device in Low–Power Mode
- Compatible with PowerPC Platform (CHRP)
- Packaged in a 80–Pin Thin Quad Flat Pack (TQFP)

PowerPC is a trademark of IBM Corp.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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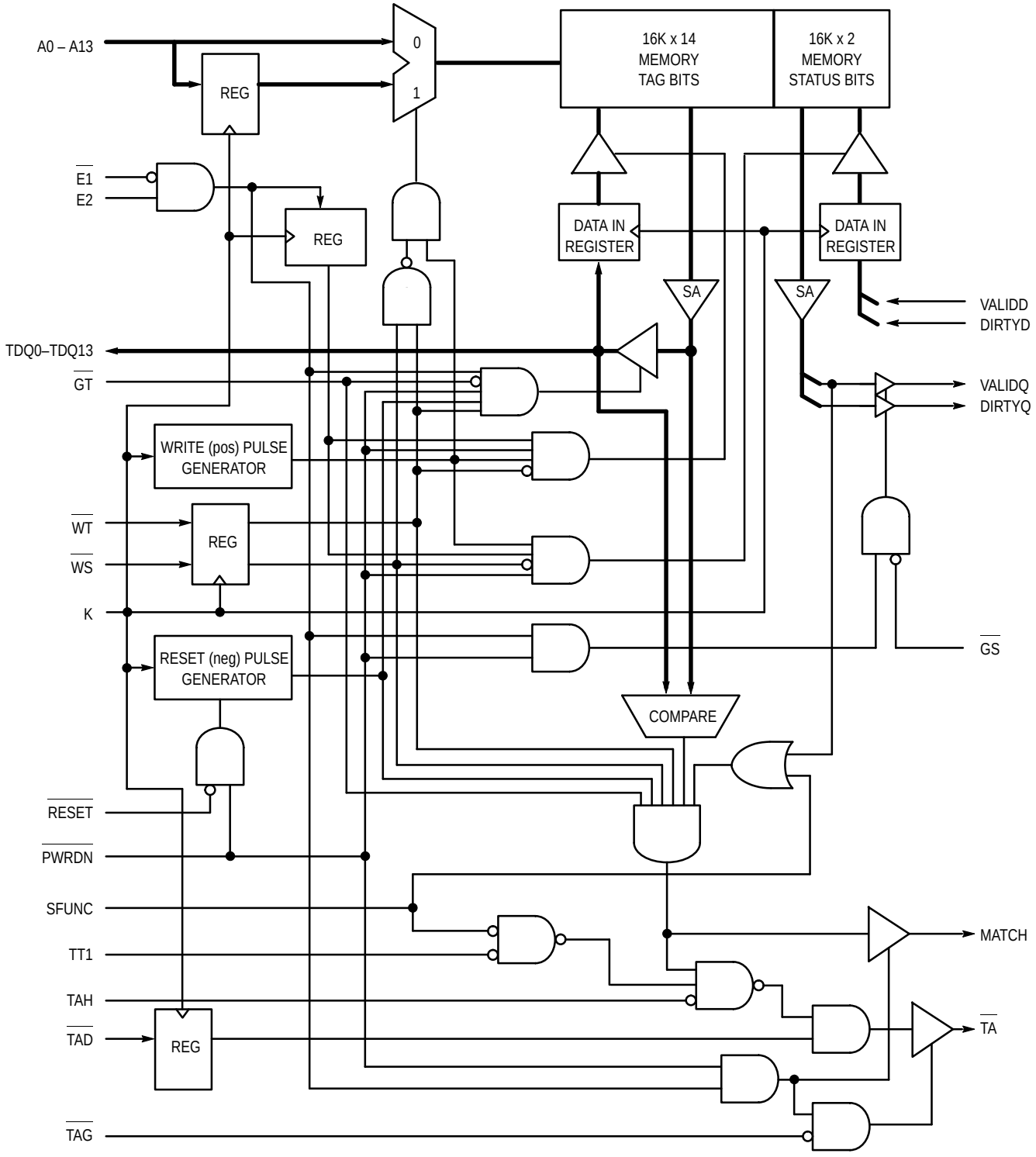
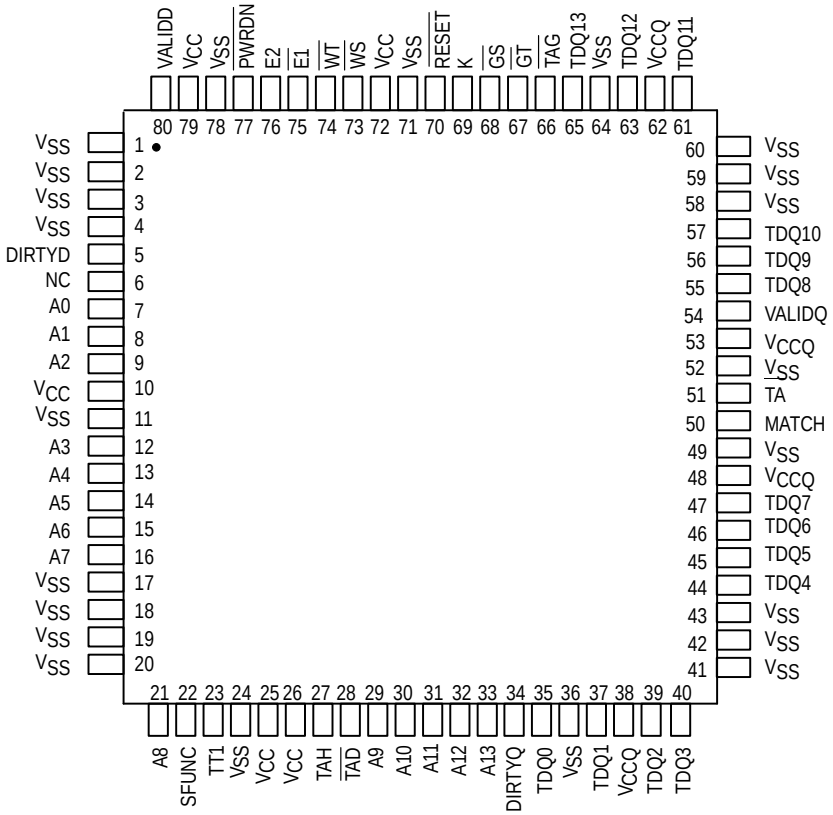
FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS



PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
7, 8, 9, 12, 13, 14, 15, 16, 21, 29, 30, 31, 32, 33,	A0 – A13	Input	Address Inputs: These inputs are registered and must meet setup and hold times for write cycles only. For all other cycles, addresses are asynchronous.
75, 76	$\overline{E1}$, E2	Input	Chip Selects: These inputs are registered and must meet setup and hold times for write cycles only. For all other cycles, E1 and E2 are asynchronous.
69	K	Input	Clock: This signal registers the address, data in, and all control signals except G, TAH, TT1, SFUNC, and PWRDN.
74	WT	Input	Write Enable–Tag Bits: This input is registered and must meet setup and hold times for all cycles this chip is selected.
73	WS	Input	Write Enable–Status Bits: This input is registered and must meet setup and hold times for all cycles this chip is selected.
67	$\overline{GT}$	Input	Output Enable–Tag Bits: Asynchronous, active low.
68	$\overline{GS}$	Input	Output Enable–Status Bits: Asynchronous, active low.
70	RESET	Input	Status Bit Reset: Reset cycle is initiated synchronously on a rising clock edge and will terminate within the Status Bit Reset Time. When RESET is returned high, the part will return to normal operation within the time specified in the RESET AC Cycle Timing table.
77	$\overline{PWRDN}$	Input	Powerdown Mode Control Pin: This signal is asynchronous and places the RAM in standby mode.
22	SFUNC	Input	Status Bit Function Control Pin
23	TT1	Input	Read/Write Input from Processor
80	VALIDD	Input	Valid Bit Input
5	DIRTYD	Input	Dirty Bit Input
6	NC	—	No Connection to the Chip
51	$\overline{TA}$	Output	Transfer Acknowledge: Typically used as “ready” signal to processor for cache reads. Can also be used as an active low MATCH pin.
27	TAH	Input	$\overline{TA}$ Force High: Active high signal places $\overline{TA}$ into high–Z mode.
66	$\overline{TAG}$	Input	$\overline{TA}$ Output Enable: Asynchronous, active low.
28	$\overline{TAD}$	Input	Additional $\overline{TA}$ Input
35, 37, 39, 40, 44, 45, 46, 47, 55, 56, 57, 61, 63, 65,	TDQ0–TDQ13	I/O	Tag Data Input/Outputs: Used as input port for compare cycles. Used as output port for tag read cycles.
54	VALIDQ	Output	Valid Bit Output
34	DIRTYQ	Output	Dirty Bit Output
50	MATCH	Output	Match: This pin is asserted high when the selected tag’s valid bit is true, and the stored tag in the RAM array matches the tag data presented on the TDQ pins.
10, 25, 26, 72, 79	V_{CC}	Supply	Power Supply: 5.0 V ± 5%
38, 48, 53, 62	V_{CCQ}	Supply	Output Buffer Power Supply: 5 V ± 5% or 3.3 V ± 0.3 V.
1, 2, 3, 4, 11, 17, 18, 19, 20, 24, 36, 41, 42, 43, 49, 52, 58, 59, 60, 64, 71, 78	V_{SS}	Supply	Ground

HIP SELECT FUNCTION TRUTH TABLE (See Notes 1 and 2)

Next Cycle	E1	E2	RESET	PWRDN	K	WT	WS	TAG	TDQ	VALIDQ	DIRTYQ	MATCH	TA	POWER
Deselect	H	X	X	H	X	X	X	X	High–Z	High–Z	High–Z	High–Z	High–Z	Active
Deselect	X	L	X	H	X	X	X	X	High–Z	High–Z	High–Z	High–Z	High–Z	Active
Select	L	H	X	H	X	X	X	X	—	—	—	—	—	Active

RESET FUNCTION TRUTH TABLE (See Notes 1 and 2)

Next Cycle	E1	E2	RESET	PWRDN	K	WT	WS	TAG	TDQ	VALIDQ	DIRTYQ	MATCH	TA	POWER
Reset Status	L	H	L	H	↑	H	H	L	High–Z	L(3)	L(3)	L	H(4)	Active
Reset Status	L	H	L	H	↑	H	H	H	High–Z	L(3)	L(3)	L	High–Z	Active
Reset Status	H	X	L	H	↑	H	H	X	High–Z	High–Z	High–Z	High–Z	High–Z	Active
Reset Status	X	L	L	H	↑	H	H	X	High–Z	High–Z	High–Z	High–Z	High–Z	Active
Not Allowed	X	X	L	H	↑	L	X	X	—	—	—	—	—	—
Not Allowed	X	X	L	H	↑	X	L	X	—	—	—	—	—	—

POWER–DOWN FUNCTION TRUTH TABLE (See Notes 1 and 2)

Next Cycle	E1	E2	RESET	PWRDN	K	WT	WS	TAG	TDQ	VALIDQ	DIRTYQ	MATCH	TA	POWER
Standby	X	X	X	L	X	H	H	X	High–Z	High–Z	High–Z	High–Z	High–Z	Power–down

NOTES: 1. X = Don't Care, H = V_{IH}, L = V_{IL}, "—" = Undefined.
2. GT, GS, TT1, TAH, and SFUNC are X for this table.
3. GS is low.
4. TA output is dependent on the previous registered value of $\overline{TAD}$.

READ FUNCTION TRUTH TABLE (See Notes 1 and 2)

Cycle Type	GT	GS	WT	WS	K	TT1	TDQ	VALIDD	DIRTYD	VALIDQ	DIRTYQ	MATCH
Read Tag I/O	L	X	H	X	X	X	D_{out}	—	—	—	—	L
Read Status Bits	X	L	X	X	X	X	—	—	—	D_{out}	D_{out}	—
Tag I/O Disable	H	X	X	X	X	X	High–Z	—	—	—	—	—
Status Disable	X	H	X	X	X	X	—	—	—	High–Z	High–Z	—

WRITE FUNCTION TRUTH TABLE (See Notes 1 and 2)

Cycle Type	GT	GS	WT	WS	K	TT1	TDQ	VALIDD	DIRTYD	VALIDQ	DIRTYQ	MATCH
Write Tag I/O	H	X	L	X	↑	X	D_{in}	—	—	—	—	L
Not Allowed	L	X	L	X	↑	X	—	—	—	—	—	—
Write Status Bits	X	L	X	L	↑	X	—	D_{in}	D_{in}	D_{out}(3)	D_{out}(3)	L
Write Status Bits	X	H	X	L	↑	X	—	D_{in}	D_{in}	High–Z	High–Z	L

NOTES: 1. X = Don't Care, H = V_{IH}, L = V_{IL}, "—" = Undefined.
2. This table applies when E1 is low, and E2, RESET, and $\overline{PWRDN}$ are high. $\overline{TAG}$, TAH, $\overline{TAD}$, and SFUNC are X for this table.
3. D_{out} in this case is the same as D_{in}; the input data is written through to the outputs during the write operation.

MATCH FUNCTION TRUTH TABLE (See Notes 1 and 3)

Next Cycle	E1	E2	SFUNC	GT	WT	WS	TDQ	VALIDQ(4)	DIRTYQ(4)	MATCH
Deselect	H	X	X	X	X	X	High–Z	—	—	High–Z
Deselect	X	L	X	X	X	X	High–Z	—	—	High–Z
Select	L	H	X	X	X	X	—	—	—	—
Read Tag I/O	L	H	X	L	H	X	D_{out}	—	—	L
Write Tag I/O	L	H	X	H	L	X	D_{in}	—	—	L
Write Status Bits	L	H	X	X	X	L	—	D_{in}	D_{in}	L
Invalid Data–Dedicated Status Bits	L	H	L	H	H	H	TDQ_{in}	L	—	L
Match–Dedicated Status Bits	L	H	L	H	H	H	TDQ_{in}	H	—	M(2)
Match–Generic Status Bits	L	H	H	H	H	H	TDQ_{in}	X	—	M(2)

NOTES: 1. X = don't care, H = V_{IH}, L = V_{IL}, "—" = Undefined.
2. M = high if TDQ_{in} equals the memory contents at that address; M = low if TDQ_{in} does not equal the memory contents at that address.
3. PWRDN and RESET are high for this table. TT1, TAH, TAG, TAD, GS, and K are X.
4. This column represents the stored memory cell data for the given status bit at the selected address.

TA FUNCTION TRUTH TABLE (See Notes 1, 2, 3, and 5)

Next Cycle	TAG	TAD(6)	GT	WT	WS	TAH	TT1	SFUNC	TDQ	VALIDQ(4)	DIRTYQ(4)	MATCH	$\overline{TA}$
TA Disabled	H	X	X	X	X	X	X	X	—	X	—	—	High–Z
External TA Input(7)	L	L	X	X	X	X	X	X	—	X	—	—	L
Read Tag	L	H	L	X	X	X	X	X	D_{out}	X	—	L	H
Write Tag	L	H	X	L	X	X	X	X	D_{in}	X	—	L	H
Write Status	L	H	X	X	L	X	X	X	—	D_{in}	D_{in}	L	H
Force TA High	L	H	X	X	X	H	X	X	—	X	—	—	H
Invalid Tag	L	H	X	X	X	X	X	L	—	L	—	L	H
Compare	L	H	H	H	H	L	H	L	TDQ_{in}	H	—	M(2)	M(2)
Compare	L	H	H	H	H	L	X	H	TDQ_{in}	X	—	M(2)	M(2)

NOTES: 1. X = don't care, H = V_{IH}, L = V_{IL}, "—" = Undefined.
2. M = high if TDQ_{in} equals the memory contents at that address; M = low if TDQ_{in} does not equal the memory contents at that address.
3. PWRDN and RESET are high for this table. GS and K are X.
4. This column represents the stored memory cell data for the given status bit at the selected address.
5. E1 is low, E2 is high for this table.
6. TAD, WT, and WS are synchronous inputs; thus the inputs noted in the table must be applied during a rising K edge.
7. TAD will be a factor in determining the TA output in all cases except when TAH is low, SFUNC and/or TT1 is high, and there is a valid MATCH. In that case, TA will be low (valid).

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}, V_{CCQ}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.7	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

TQFP PACKAGE THERMAL CHARACTERISTICS (See Note 1)

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	45 38	°C/W	2
Junction to Board (Leads)		$R_{\theta JB}$	27	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	12	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87. Single layer board is the normally quoted value per the specification. The result on the four layer board is an extension to that specification.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, V_{CCQ} = 5.0 V ± 5%, or 3.3 V ± 0.3 V, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
5 V Output Buffers	V_{CCQ}	4.75	5.0	5.25	V
3.3 V Output Buffers	V_{CCQ}	3.0	3.3	3.6	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V

* V_{IL} (min) = – 2.0 V for pulse width of less than 10 ns, once per cycle.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit	Notes
Input Leakage Current (V_{CC} = Max, V_{in} = 0 V to V_{CC})		$I_{lkg(I)}$	—	± 1	µA	
Output Leakage Current (E1 ≥ V_{IH} , E2 ≤ V_{IL}, G ≥ V_{IH}, V_{CC} = Max, V_{out} = 0 V to V_{CCQ}, V_{CCQ} = Max)		$I_{lkg(O)}$	—	± 1	µA	
AC Supply Current (PWRDN ≥ V_{IH}, Outputs Open, V_{CC} = Max, f = f_{MAX})	MPC27T416–9 MPC27T416–10 MPC27T416–12	I_{CCA}	—	300 290 280	mA	3
CMOS Standby Supply Current (PWRDN ≤ V_{IL}, V_{in} ≥ V_{IH} or ≤ V_{IL}, V_{CC} = Max, f = f_{MAX})	MPC27T416–9 MPC27T416–10 MPC27T416–12	I_{SB1}	—	30 30 30	mA	3
Clock Running Supply Current ($\overline{\text{PWRDN}}$ ≤ V_{IL}, V_{in} ≥ V_{HC} or ≤ V_{LC}, V_{CC} = Max, f = 0)	MPC27T416–9 MPC27T416–10 MPC27T416–12	I_{SB2}	—	25 25 25	mA	3, 4
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	0.4	V	
Output High Voltage (I_{OH} = –4 mA)		V_{OH}	2.4	—	V	

NOTES: 1. All values are maximum guaranteed values.
2. E1 ≤ V_{IL}, E2 ≥ V_{IH}.
3. f_{MAX} = 1/t_{CYC} (all address inputs are cycling at f_{MAX}). f = 0 means no address input lines are changing.
4. V_{HC} = V_{CC} – 0.2 V, V_{LC} = 0.2 V.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	6	pF
Tag Input/Output Capacitance	$C_{I/O}$	—	8	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, V_{CCQ} = 5.0 V ± 5% or 3.3 V ± 0.3 V, T_J = 20 to 110°C, Unless Otherwise Noted)

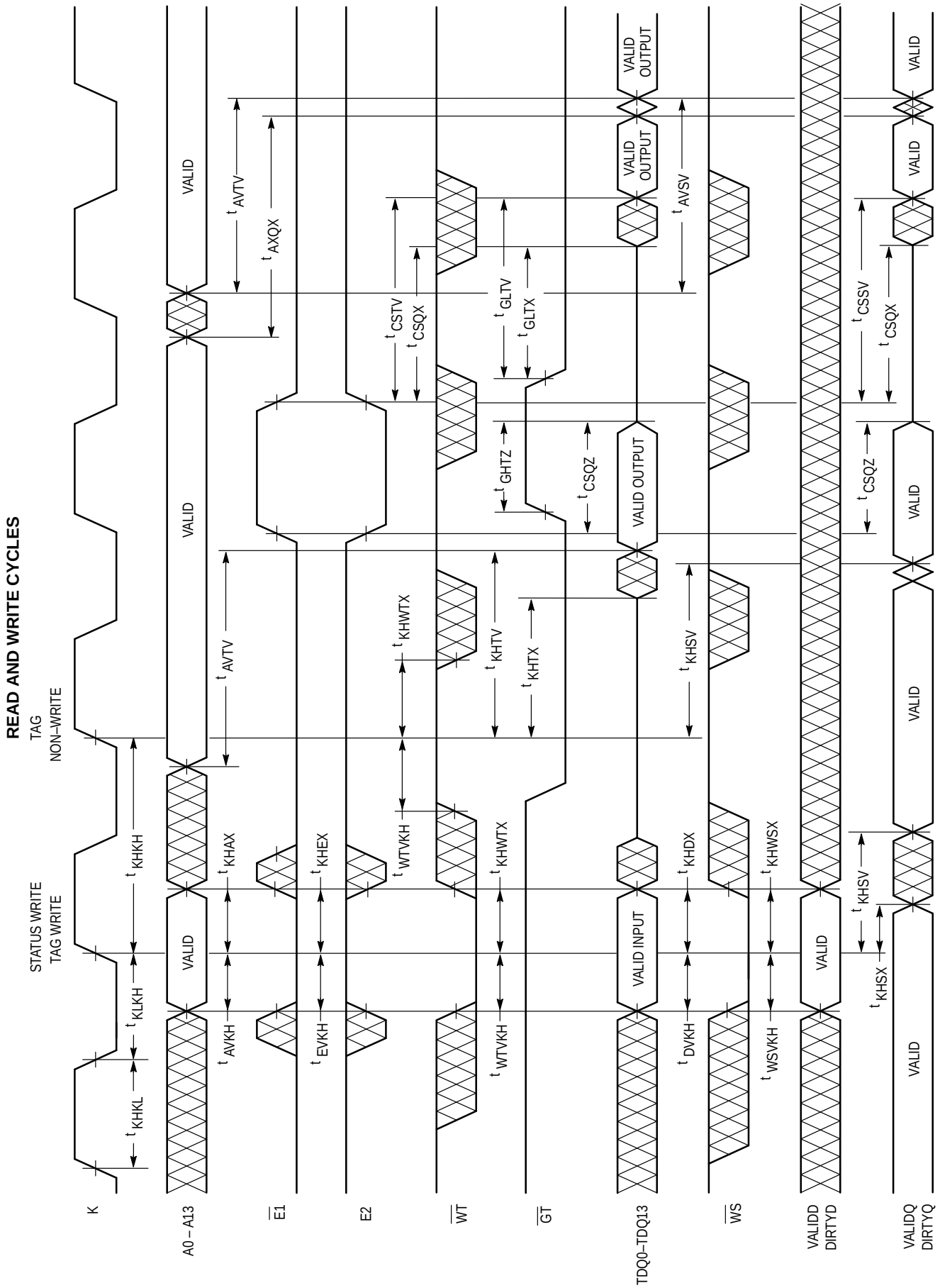
Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 2 ns

Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Note 1)

Parameter	Symbol	MPC27T416–9		MPC27T416–10		MPC27T416–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock Cycle Time	t_{KHKH}	15	—	15	—	16.6	—	ns	
Address Access Time Tag Bits	t_{AVTV}	—	11	—	12	—	14	ns	
Chip Select Access Time Tag Bits	t_{CSTV}	—	9	—	10	—	12	ns	
Chip Select to Tag and Status Bits in Low–Z	t_{CSQX}	1	—	1	—	1	—	ns	2
Chip Select to Tag and Status Bits in High–Z	t_{CSQZ}	1	6	1	6	1	7	ns	2
Output Enable to Tag Bits Valid	t_{GLTV}	—	6	—	6	—	7	ns	
Output Enable to Tag Bits Low–Z	t_{GLTX}	0	—	0	—	0	—	ns	2
Output Enable to Tag Bits High–Z	t_{GHTZ}	1	6	1	6	1	7	ns	2
Tag and Status Bit Hold from Address Change	t_{AXQX}	2	—	2	—	2	—	ns	
Address Access Time Status Bits	t_{AVSV}	—	9	—	10	—	12	ns	
Chip Select Access Time Status Bits	t_{CSSV}	—	7	—	8	—	10	ns	
Clock High Read to Outputs in Low–Z	t_{KHTX}	1.5	—	1.5	—	1.5	—	ns	2
Clock High Read to Tag Bits Valid	t_{KHTV}	—	10	—	10	—	12	ns	3
Clock High Write to Status Outputs Valid	t_{KHSV}	—	9	—	9	—	10	ns	3
Status Output Hold from Clock High Write	t_{KHSX}	0	—	0	—	0	—	ns	2
Output Enable to Status Bits Valid	t_{GLSV}	—	6	—	6	—	7	ns	
Output Enable to Status Bits High–Z	t_{GHSZ}	1	6	1	6	1	7	ns	
Output Enable to Status Bits Low–Z	t_{GLSX}	0	—	0	—	0	—	ns	
$\overline{WT}$ and $\overline{WS}$ High to $\overline{PWRDN}$ Low	t_{WHPL}	5	—	5	—	5	—	ns	
$\overline{PWRDN}$ High to $\overline{WT}$ and $\overline{WS}$ Active	t_{PHWL}	50	—	50	—	50	—	ns	
Clock Pulse High	t_{KHKL}	4.5	—	4.5	—	5	—	ns	
Clock Pulse Low	t_{KLKH}	4.5	—	4.5	—	5	—	ns	
Setup Times: Address Tag Write Enable Status Write Enable Data In Chip Enable	t_{AVKH} t_{WTVKH} t_{WSVKH} t_{DVKH} t_{EVKH}	3	—	3	—	3	—	ns	
Hold Times: Address Tag Write Enable Status Write Enable Data In Chip Enable	t_{KHAX} t_{KHWTX} t_{KHWSX} t_{KHDX} t_{KHEX}	1.0	—	1.0	—	1.0	—	ns	

NOTES:
1. All Write cycles are synchronous and referenced from rising K.
2. This parameter is sampled and not 100% tested.
3. Addresses are stable prior to K transition high.


READ AND WRITE CYCLES
STATUS WRITE
TAG WRITE
TAG
NON–WRITE
K
A0 – A13
Ei
E2
WT
GT
TDQ0–TDQ13
WS
VALIDD
DIRTYD
VALIDQ
DIRTYQ
VALID
VALID INPUT
VALID OUTPUT
tKHKH
tKHKL
tKLKH
tAVTV
tAXQX
tKHAX
tAVKH
tKHEX
tEVKH
tKHWTX
tWTVKH
tKHTV
tKHTX
tWTVKH
tKHWTX
tKHSV
tKHDX
tDVKH
tKHWSX
tWSVKH
tKHSV
tKHSX
tCSTV
tCSQX
tGLTV
tGLTX
tGHTZ
tCSQZ
tAVSV
tCSSV
tCSQX
tCSQZ

MATCH AND $\overline{TA}$ CYCLE TIMING

Parameter	Symbol	MPC27T416–9		MPC27T416–10		MPC27T416–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Address to MATCH Valid	t_{AVMV}	—	9	—	10	—	12	ns	
Data Input to MATCH Valid	t_{TVMV}	—	9	—	10	—	12	ns	
Chip Select to MATCH Valid	t_{CSMV}	—	9	—	10	—	12	ns	
Chip Select to MATCH in Low–Z	t_{CSMX}	1	—	1	—	1	—	ns	1
Chip Select to MATCH in High–Z	t_{CSMZ}	1	6	1	6	1	7	ns	1
MATCH Valid Hold from Address	t_{AVMX}	2	—	2	—	2	—	ns	
MATCH Valid Hold from Data	t_{TVMX}	2	—	2	—	2	—	ns	
TA Valid Hold from Address	t_{AVTAX}	2	—	2	—	2	—	ns	
TA Valid Hold from Data	t_{TVTAX}	2	—	2	—	2	—	ns	
Address to TA Valid	t_{AVTAV}	—	10	—	11	—	13	ns	
Data Input to TA Valid	t_{TVTAV}	—	10	—	11	—	13	ns	
Chip Select Low to TA Valid	t_{CSTAV}	—	10	—	11	—	13	ns	
TAG Low to TA Valid	t_{TAGTAV}	—	6	—	7	—	8	ns	
TAG Low to TA in Low–Z	t_{TAGTAX}	0	—	0	—	0	—	ns	1
TAG High to TA in High–Z	t_{TAGTAZ}	1	6	1	6	1	7	ns	1
TAH High to Force TA High	t_{TAFTAH}	—	5	—	5	—	6	ns	
TAH Low to TA Valid	t_{TAFTAV}	—	5	—	5	—	6	ns	
TAD Set–up Time	t_{TADVKH}	4	—	4	—	4	—	ns	
TAD Hold Time	t_{KHTADX}	1.5	—	1.5	—	1.5	—	ns	
Clock High TAD Low to TA Low	t_{TADTAL}	—	6	—	7	—	8	ns	
Clock High TAD High to TA Valid	t_{TADTAV}	—	6	—	7	—	8	ns	
GT Low to MATCH and TA Invalid	t_{GTML}	—	7	—	7	—	8	ns	
GT High to MATCH and TA Valid	t_{GTMV}	—	8	—	8	—	10	ns	
TT1 Low to TA High	t_{TTLTAH}	—	7	—	7	—	8	ns	2
TT1 High to TA Valid	t_{TTHTAV}	—	7	—	7	—	8	ns	2
Clock High Write to MATCH and TA Invalid	t_{KHMI}	—	7	—	7	—	8	ns	
Clock High Read to MATCH and TA Valid	t_{KHMV}	—	9	—	10	—	12	ns	3
Setup Times: Tag Write Enable Status Write Enable	t_{WTVKH} t_{WSVKH}	3	—	3	—	3	—	ns	
Hold Times: Tag Write Enable Status Write Enable	t_{KHWTX} t_{KHWSK}	1.0	—	1.0	—	1.0	—	ns	

NOTES:
1. This parameter is sampled and not 100% tested.
2. These parameters only apply when SFUNC is low.
3. t_{AVMV}, t_{TVMV}, t_{CSMV}, t_{ADB}, t_{DAB}, t_{CSB} must also be satisfied.

AC TEST LOADS

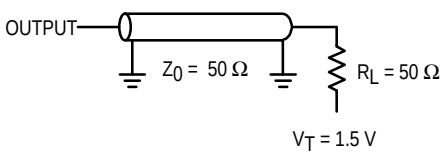


Figure 1A. AC Test Load

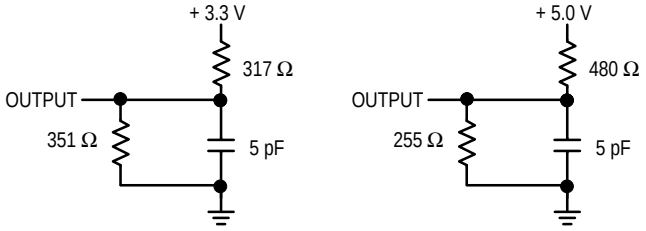
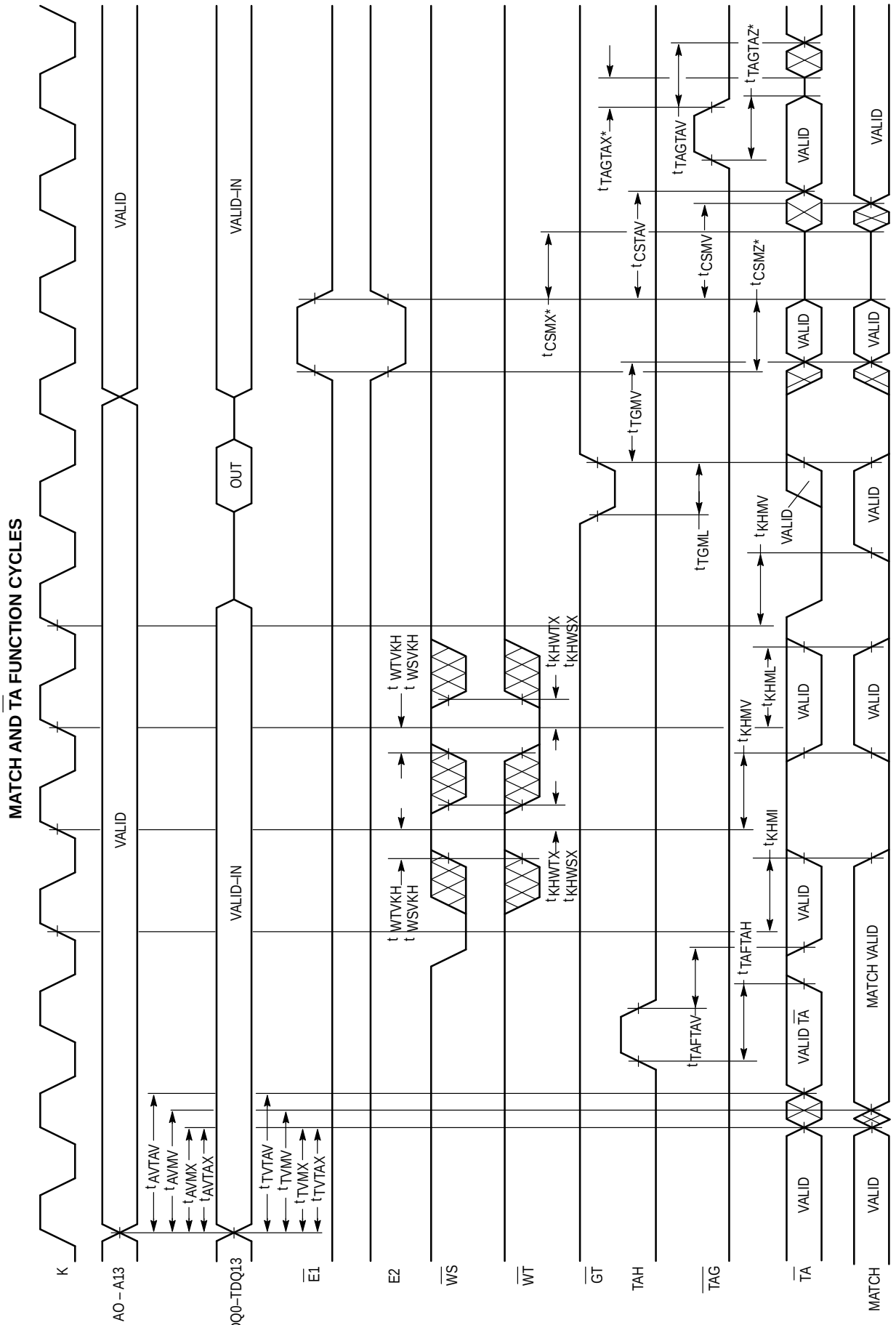


Figure 1B. High–Z Test Load



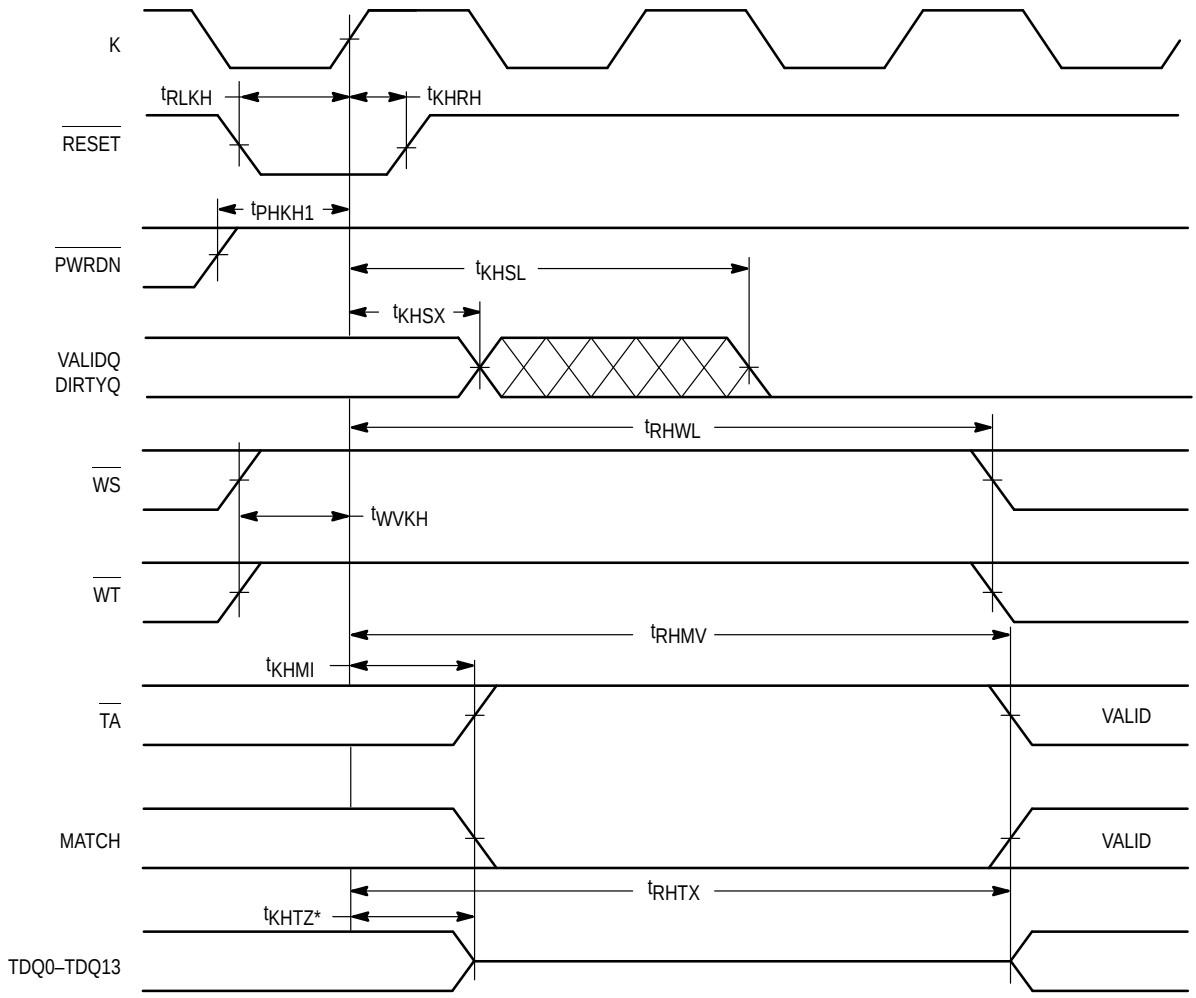
* Transition is measured plus or minus 200 mV from steady state.

RESET AND PWRDN CYCLE TIMING (See Note 2)

Parameter	Symbol	MPC27T416–9		MPC27T416–10		MPC27T416–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
RESET Set–up Time	t_{RLKH}	4	—	4	—	4	—	ns	
RESET Hold Time	t_{KHRH}	1	—	1	—	1	—	ns	
Status Bit Reset Time	t_{KHSL}	—	60	—	60	—	70	ns	
Status Bit Hold from RESET Low	t_{KHSX}	2	—	2	—	2	—	ns	
RESET Low to MATCH and TA Invalid	t_{KHMI}	—	10	—	10	—	12	ns	
RESET High to MATCH and TA Valid	t_{RHMV}	—	120	—	120	—	130	ns	
RESET Low to Tag Bits High–Z	t_{KHTZ}	—	10	—	10	—	12	ns	1
RESET High to Tag Bits Low–Z	t_{RHTX}	—	100	—	100	—	110	ns	1
PWRDN Set–up Time (when RESET low)	t_{PHKH1}	30	—	30	—	30	—	ns	
RESET High to WT and WS Low	t_{RHWL}	95	—	95	—	105	—	ns	
PWRDN Low to Low Power Mode	t_{PLIL}	—	50	—	50	—	50	ns	1
PWRDN High to Active Power Mode	t_{PHIH}	0	—	0	—	0	—	ns	1
PWRDN Low to Outputs in High–Z	t_{PLQZ}	—	10	—	10	—	12	ns	1
PWRDN High to Outputs in Low–Z	t_{PHQX}	0	—	0	—	0	—	ns	1
PWRDN High to Outputs Valid	t_{PHQV}	—	50	—	50	—	50	ns	
WT and WS High to PWRDN Low	t_{KHPL}	5	—	5	—	5	—	ns	1
WT and WS Set–up Time	t_{WVKH}	3	—	3	—	3	—	ns	
PWRDN Set–up Time (first write following PWRDN cycle)	t_{PHKH2}	50	—	50	—	50	—	ns	

NOTES:
1. This parameter is sampled and not 100% tested.
2. PWRDN mode is intended to be used during extended time periods of device inactivity.

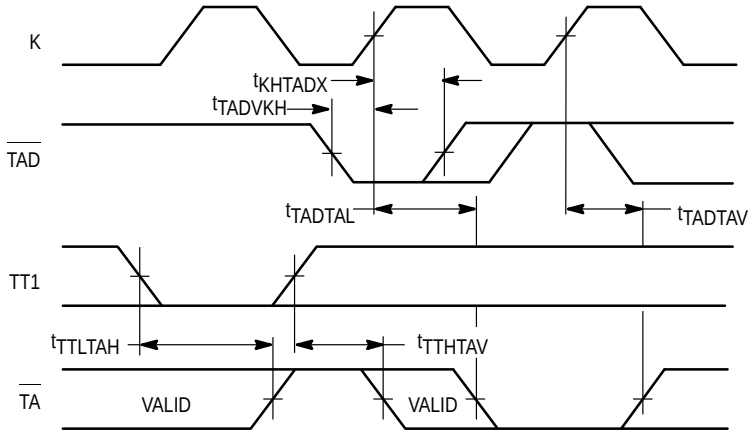
$\overline{\text{RESET}}$ FUNCTION



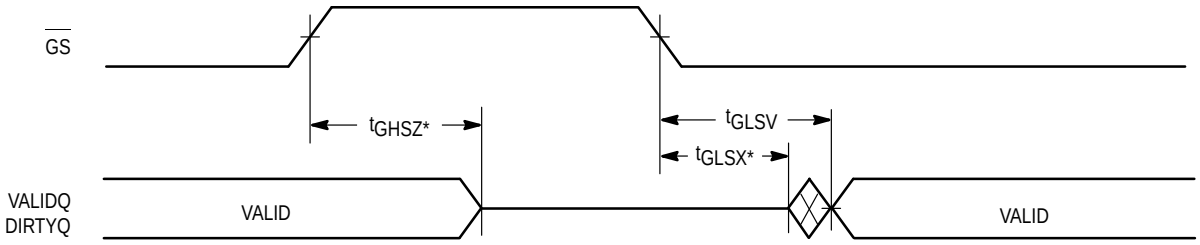
* Transition is measured plus or minus 200 mV from steady state.

$\overline{\text{TA}}$ AND TT1 SIGNAL

(SFUNC = low)

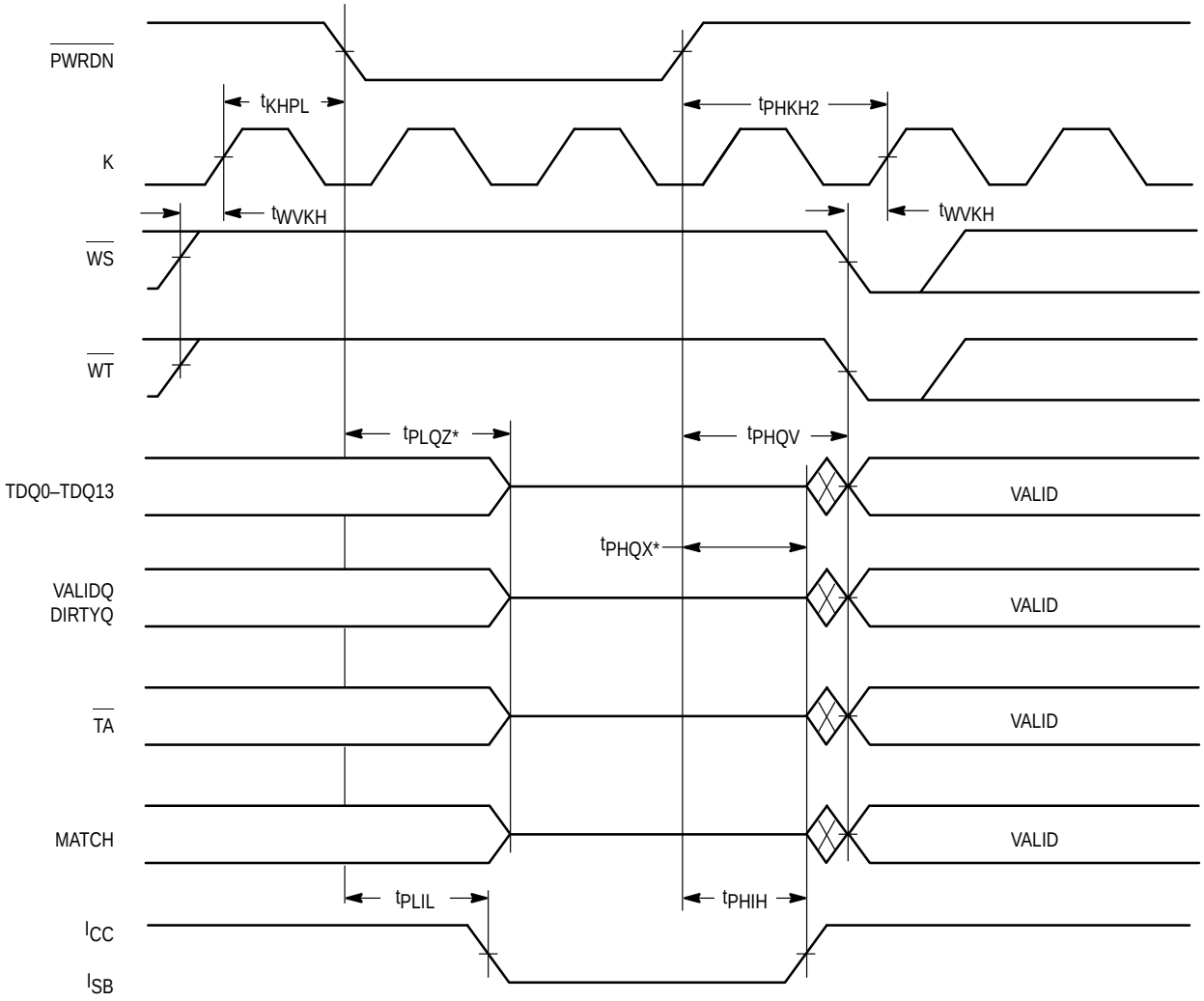


$\overline{GS}$ FUNCTION



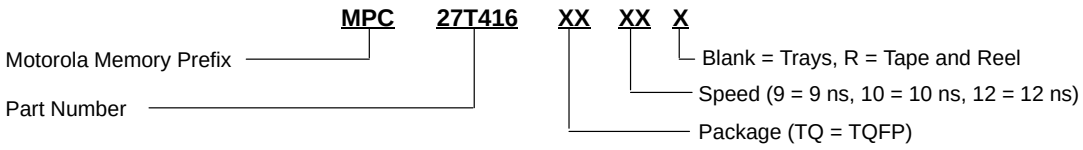
* Transition is measured plus or minus 200 mV from steady state.

POWER DOWN FUNCTION



* Transition is measured plus or minus 200 mV from steady state.

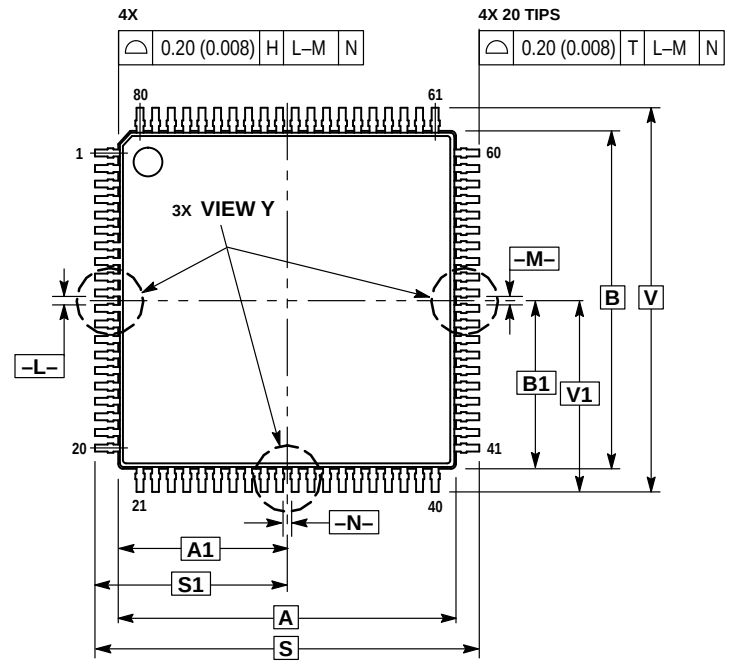
ORDERING INFORMATION
(Order by Full Part Number)

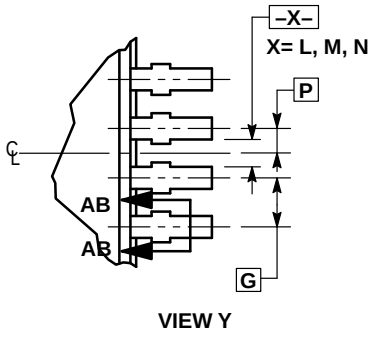


Full Part Numbers — MPC27T416TQ9 MPC27T416TQ10 MPC27T416TQ12
MPC27T416TQ9R MPC27T416TQ10R MPC27T416TQ12R

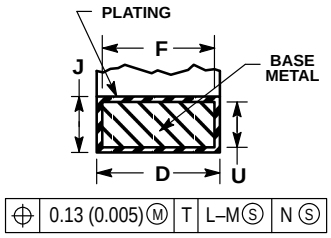
PACKAGE DIMENSIONS

TQ PACKAGE
TQFP
CASE 917A–02

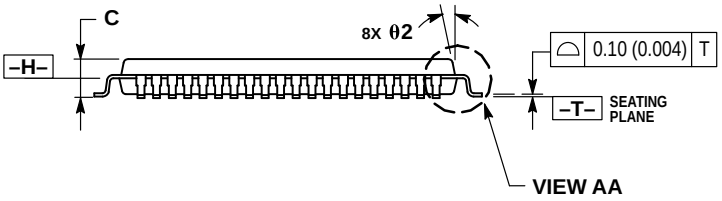




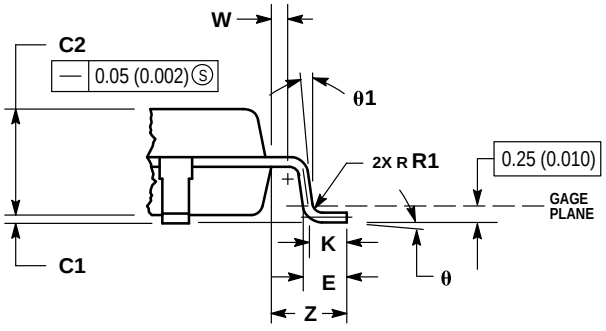
VIEW Y



SECTION AB–AB
ROTATED 90° CLOCKWISE



VIEW AA



VIEW AA

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.460 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.00 BSC		0.551 BSC	
A1	7.00 BSC		0.276 BSC	
B	14.00 BSC		0.551 BSC	
B1	7.00 BSC		0.276 BSC	
C	—	1.74	—	0.069
C1	0.04	0.24	0.002	0.009
C2	1.30	1.50	0.051	0.059
D	0.22	0.38	0.009	0.015
E	0.40	0.75	0.016	0.030
F	0.17	0.33	0.007	0.013
G	0.65 BSC		0.026 BSC	
J	0.09	0.27	0.004	0.011
K	0.50 REF		0.020 REF	
P	0.325 BSC		0.013 REF	
R1	0.09	0.20	0.004	0.008
S	16.00 BSC		0.630 BSC	
S1	8.00 BSC		0.315 BSC	
U	0.09	0.16	0.004	0.006
V	16.00 BSC		0.630 BSC	
V1	8.00 BSC		0.315 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	10°	0°	10°
θ1	0°	—	0°	—
θ2	9°	14°	9°	14°

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