# MP8840

8-Channel, Voltage Output, 2 MHz, 4 Quadrant Multiplying, 8-Bit DAC with Serial Digital Data Port

## FEATURES

- **8 Independent 4-Quadrant Multiplying 8-Bit DACs**
- **High Speed:**
  - **Settling Time: 3.5 μs to ±1 LSB**
  - **Slew Rate: 4 V/μs**
  - **Voltage Reference Input Bandwidth: 2.5 MHz ($V_{IN}$ = 100 mV p-p)**
- **Low Power: 80 mW (typ)**
- **DACs Matched to ±0.5% (typ)**
- **Midscale Preset, All DAC Outputs are Zero Volts**
- **Latch-Up Free**
- **Greater than 2000 V ESD Protection**
- **5 MHz Version: MP7670**

## APPLICATIONS

- **Analog Multiplier Replacement**
- **High-Frequency Gain Control using DACs**
- **Convergence Adjustment for Displays and Monitors**
- **Potentiometer Adjustment Replacement**

## GENERAL DESCRIPTION

The MP8840 is an 8-channel, 4 quadrant multiplying, 8-bit accurate digital-to-analog converter with a 2.5 MHz input bandwidth. It includes an output drive amplifier per channel capable of driving a ±5 mA minimum to a load. DNL of ±1/4 LSB (typ) is achieved with a channel-to-channel matching of better than 0.5% (typ). Stability, matching, and precision of the DACs are achieved by using EXAR's thin film technology.

The MP8840 is ideal for direct gain control of high frequency analog signals. The bipolar output amplifier has low noise which produces a very sharp signal output particularly in display and monitor applications.

A proprietary subranging architecture provides wide signal bandwidth from $V_{IN}$ to output up to 2.5 MHz (typ), fast output settling time, and $V_{IN}$ feedthrough isolation of –60dB (typ).

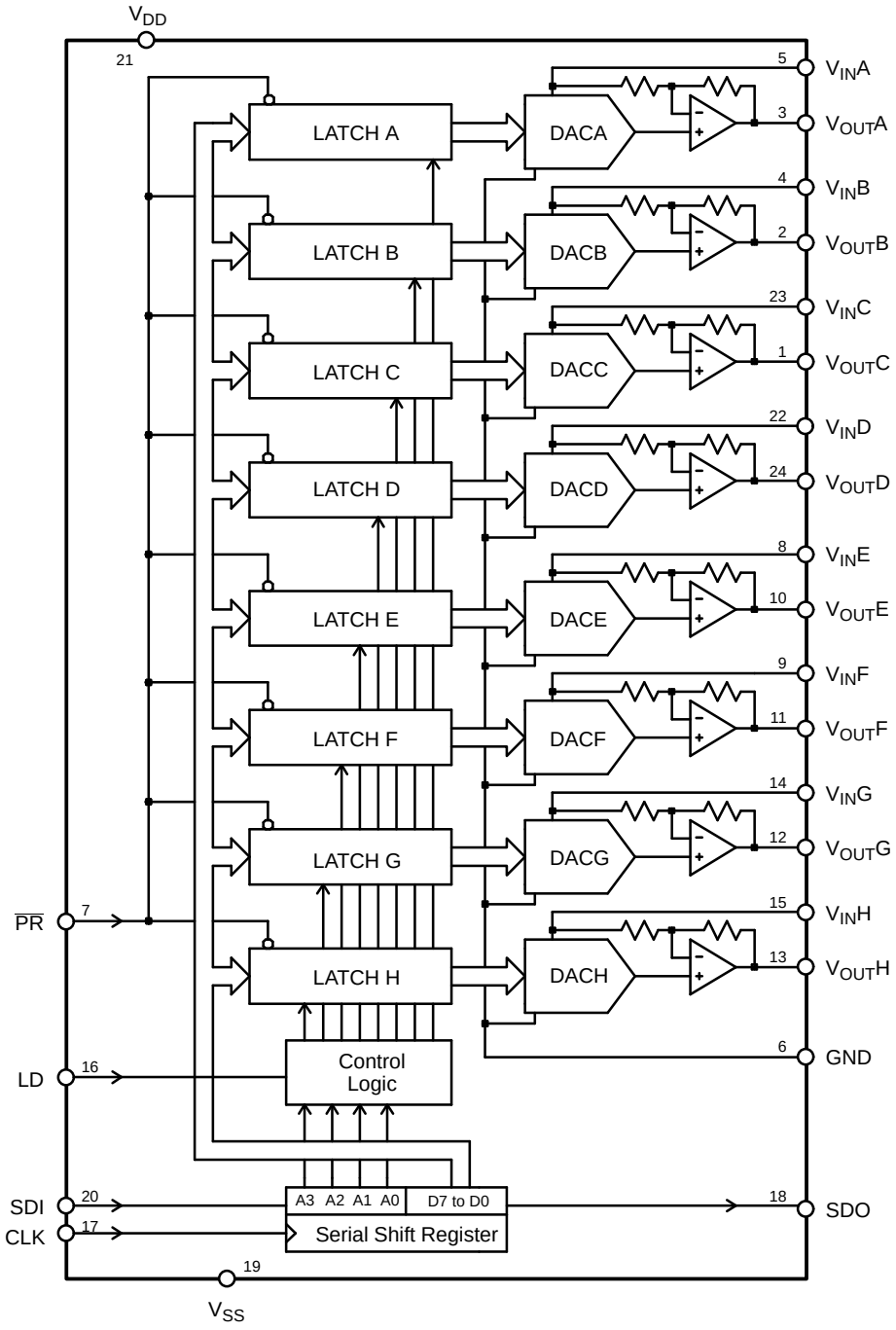
The MP8840 has a serial data 3-wire standard μ-processor logic interface to reduce pin count, package size, and board wire (space).

The MP8840 is fabricated on a junction isolated, high speed BiCMOS1™ process with thin film resistors.

## ORDERING INFORMATION

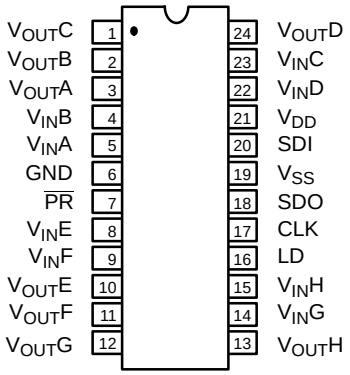
| Package Type | Temperature Range | Part No. |
|---|---|---|
| Plastic Dip | –40 to +85°C | MP8840AN |
| SOIC | –40 to +85°C | MP8840AS |

## SIMPLIFIED BLOCK DIAGRAM

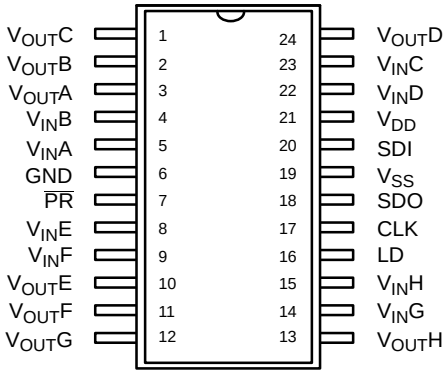


## PIN CONFIGURATIONS

*See Packaging Section for Package Dimensions*




**24 Pin PDIP (0.300")**
**NN24**




**24 Pin SOIC (Jedec, 0.300")**
**S24**

## PIN OUT DEFINITIONS

| PIN NO. | NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_{OUT}C$ | DAC C Output |
| 2 | $V_{OUT}B$ | DAC B Output |
| 3 | $V_{OUT}A$ | DAC A Output |
| 4 | $V_{IN}B$ | DAC B Reference Input |
| 5 | $V_{IN}A$ | DAC A Reference Input |
| 6 | GND | Ground |
| 7 | $\overline{PR}$ | Preset Input, Active Low |
| 8 | $V_{IN}E$ | DAC E Reference Input |
| 9 | $V_{IN}F$ | DAC F Reference Input |
| 10 | $V_{OUT}E$ | DAC E Output |
| 11 | $V_{OUT}F$ | DAC F Output |
| 12 | $V_{OUT}G$ | DAC G Output |

| PIN NO. | NAME | DESCRIPTION |
|---|---|---|
| 13 | $V_{OUT}H$ | DAC H Output |
| 14 | $V_{IN}G$ | DAC G Reference Input |
| 15 | $V_{IN}H$ | DAC H Reference Input |
| 16 | LD | Load DAC Register Strobe, Active High Input |
| 17 | CLK | Serial Clock Input |
| 18 | SDO | Serial Data Output |
| 19 | $V_{SS}$ | Negative Power Supply |
| 20 | SDI | Serial Data Input |
| 21 | $V_{DD}$ | Positive Power Supply |
| 22 | $V_{IN}D$ | DAC D Reference Input |
| 23 | $V_{IN}C$ | DAC C Reference Input |
| 24 | $V_{OUT}D$ | DAC D Output |

## ELECTRICAL CHARACTERISTICS TABLE FOR DUAL SUPPLIES

**Unless Otherwise Noted: $V_{DD}$ = 5 V, $V_{SS}$ = –5 V, GND = 0 V, $V_{IN}X$ =3 V**

| Parameter | Symbol | 25°C Min | 25°C Typ | 25°C Max | Tmin to Tmax Min | Tmin to Tmax Max | Units | Test Conditions/Comments |
|---|---|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | | | |
| Resolution (All Grades) | N | 8 | | | 8 | | Bits | |
| Differential Non-Linearity | DNL | | ±1/4 | ±1 | | ±1 | LSB | |
| Integral Non-Linearity | INL | | | ±1 | | ±1 | LSB | |
| Monotonicity | | | Guaranteed | | | | | |
| **DAC OUTPUT** | | | | | | | | |
| Output Offset | $V_{BZE}$ | | 3 | 25 | | | mV | $\overline{PR}$ = 0, Sets Code = $80_H$ |
| Voltage Range | OVR | –3 | | 3 | –3 | 3 | V | |
| Output Current | $I_{OUT}$ | ±5 | ±10 | | ±5 | | mA | $\Delta V_{OUT}$ <1 LSB |
| Capacitive Load | CL | | | 200 | | 200 | pF | No oscillations |
| **REFERENCE INPUTS** | | | | | | | | |
| Input Resistance of one DAC | $R_{IN}$ | 5 | | | 5 | | KΩ | $R_{IN}$ (typ) = 15KΩ//Rx<br>Rx = 20KΩ/(1-Code/256) |
| Input Capacitance[2] | $C_{IN}$ | | 19 | 30 | | | pF | |
| Voltage Range[1] | IVR | –3 | | 3 | –3 | 3 | V | |
| **DYNAMIC CHARACTERISTICS[2]** | | | | | | | | |
| Input to Output Bandwidth | BW | 1 | 2.5 | | | | MHz | Code = FS, $V_{IN}X$ = 100 mV p-p |
| Slew Rate | SR | 1.3 | 4.0 | | | | V/µs | Measured 10% to 90%, $\Delta V_{OUT}X$ = ±6 V |
| $V_{IN}$ Feedthrough | $F_{DT}$ | | –60 | | | | dB | Code = HS, up to f = 100 kHz |
| Total Harmonic Distortion | $T_{HD}$ | | 0.02 | | | | % | $V_{IN}X$ = 4 V p-p, Code = FS<br>f = 1 kHz, $f_{LP}$ = 80 kHz |
| Spot Noise Voltage | $e_N$ | | 0.17 | | | | µV/√Hz | f = 1 kHz |
| Output Settling Time | $t_S$ | | 3.5 | 6.0 | | | µs | ±1 LSB, Code = 0 to FS |
| Channel-to-Channel Crosstalk | $C_T$ | 60 | | | | | dB | Measured between adjacent channels, f = 100 kHz |
| Digital Feedthrough | Q | | 6 | | | | nVs | $V_{IN}X$ = 0 V, Code = 0 to FS |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic High[3] | $V_{IH}$ | 2.4 | | | 2.4 | | V | |
| Logic Low[3] | $V_{IL}$ | | | 0.8 | | 0.8 | V | |
| Input Current | $I_L$ | | | ±1 | | ±1 | µA | |
| Input Capacitance[2] | $C_L$ | | | 8 | | 8 | pF | |
| **DIGITAL OUTPUTS** | | | | | | | | |
| Logic High | $V_{OH}$ | 3.5 | | | 3.5 | | | $I_{OH}$ = –0.4 mA |
| Logic Low | $V_{OL}$ | | | 0.4 | | 0.4 | | $I_{OL}$ = 1.6 mA |
| **POWER SUPPLIES** | | | | | | | | |
| Power Supply Range | $V_{DD}$ | 4.5 | | 5.5 | 4.5 | 5.5 | V | |
| | $V_{SS}$ | –5.5 | | –4.5 | –5.5 | –4.5 | V | |
| Power Supply Rejection Ratio | | | | | | | | |
| Positive | PSRR+ | | 0.0002 | 0.01 | | | %/% | $\overline{PR}$ = 0 V, $\Delta V_{DD}$ = ±5% |
| Negative | PSRR– | | 0.0002 | 0.01 | | | %/% | $\overline{PR}$ = 0 V, $\Delta V_{SS}$ = ±5% |

## ELECTRICAL CHARACTERISTICS TABLE

| Description | Symbol | 25°C Min | 25°C Typ | 25°C Max | Tmin to Tmax Min | Tmin to Tmax Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| **POWER SUPPLIES (CONT'D)** | | | | | | | | |
| Power Dissipation | $P_{DISS}$ | | 80 | 150 | | | mW | $\overline{PR}$ = 0 V |
| Power Supply Current | $I_{DD}$ | | 8 | 15 | | | mA | $\overline{PR}$ = 0 V |
| Negative Supply Current | $I_{SS}$ | | 8 | 15 | | | mA | $\overline{PR}$ = 0 V |
| **DIGITAL TIMING SPECIFICATIONS[2, 4]** | | | | | | | | |
| Input Clock Pulse Width | $t_{CH}$, $t_{CL}$ | 80 | | | | | ns | |
| Data Setup Time | $t_{DS}$ | 40 | | | | | ns | |
| Data Hold Time | $t_{DH}$ | 20 | | | | | ns | |
| CLK to SDO Propagation Delay | $t_{PD}$ | | | 120 | | | ns | |
| Load Pulse Width | $t_{LD}$ | 70 | | | | | ns | |
| Preset Pulse Width | $t_{PR}$ | 50 | | | | | ns | |
| Clock Edge to Load | $t_{CKLD}$ | 30 | | | | | ns | |
| Load Edge to Next Clk Edge | $t_{LDCK}$ | 60 | | | | | ns | |

**NOTES**

1 Maximum input voltage is 2 V less than $V_{DD}$.

2 Guaranteed but not production tested.

3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.

4 See timing diagram.

**Specifications are subject to change without notice**

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## ABSOLUTE MAXIMUM RATINGS ($T_A$ = +25°C unless otherwise noted)[1, 2]

$V_{DD}$ to GND ..... +6.5 V
$V_{SS}$ to GND ..... –6.5 V
$V_{INA-H}$ to GND ..... $V_{DD}$ to $V_{SS}$
$V_{OUTA-H}$ to GND ..... $V_{DD}$ to $V_{SS}$
Digital Input & Output Voltage to GND . –0.5 to $V_{DD}$ +0.5 V
Operating Temperature Range
Extended Industrial ..... –40°C to +85°C

Maximum Junction Temperature ..... –65°C to +150°C
Storage Temperature ..... 150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating @ 75°C
PDIP, SOIC ..... 1000mW
Derates above 75°C ..... 14mW/°C

**NOTES:**

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

## THEORY OF OPERATION

The MP8840 contains 8 independent 4-quadrant multiplying D/A converters with output amplifiers. The design has incorporated a novel approach that provides fast, accurate, low noise, low distortion, small size, and low power in the same device. This device is particularly useful in applications where multipliers are used to perform the gain adjustment function for high frequency analog signal conditioning. Also note that typical multipliers tend to increase noise particularly for low gain settings and have high offsets. The MP8840 design delivers a very low, constant noise, and low offset with digital control through the entire gain range of the D/A converter.

### Linearity Characteristics

Each D/A converter in the MP8840 achieves DNL $\leq \pm 0.25$ LSB (typ), and gain error $\leq \pm 0.5\%$ (typ). Since all 8 channels of MP8840 are fabricated in the same IC, the linearity, gain, and input-output characteristics of all 8 channels match extremely well.

### The Logic Interface and Serial Port

The MP8840 is equipped with a serial data 3-wire standard µ-processor logic interface to reduce pin count, package size, and board wire. This interface consists of LD which controls the transfer of data to the selected DAC channels that are fed through the SDI (serial digital data and address bits) with the CLK (digital input shift register clock ). Please refer to the following timing diagrams and truth tables for logic details.

A SDO (serial digital data output driver) is connected to the other side of the input shift register and would save SDI bus space by allowing the daisy chaining of several MP8840s (connecting SDI of device 2 to SDO of device 1).

When the LD signal is low, CLK signal loads the digital input bits (SDI) into the 12-bit shift register. The LD signal going high loads this data into the selected DACs. Also, when the $\overline{PR}$ signal is low, the output of all DACs would be reset to 0 volts.

### Power Supplies and Input Voltage Ranges

The output and input DC ranges are limited to within $\pm 2$ V from each positive and negative supplies. For example, with supplies at $\pm 5$V, the recommended output range is $\pm 3$V.

The MP8840 design eliminates any code dependent current change into its GND, hence easing the board level design by eliminating the stringent need for other types of DACs for low GND impedance wiring considerations at board level.

Each output of the MP8840 DAC has an output amplifier driver delivering less than 0.05Ω of output impedance through a push-pull linear output stage. Each output and input characteristics parameter match extremely well, given that all channels are fabricated in the same IC.

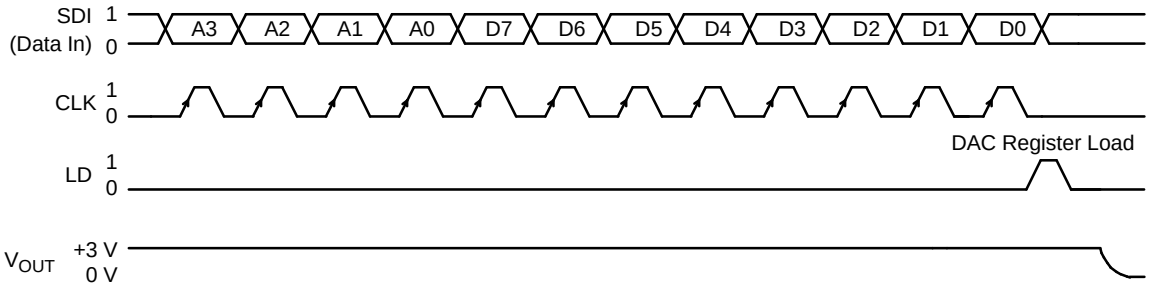



**Figure 1. Serial Data Timing and Loading**

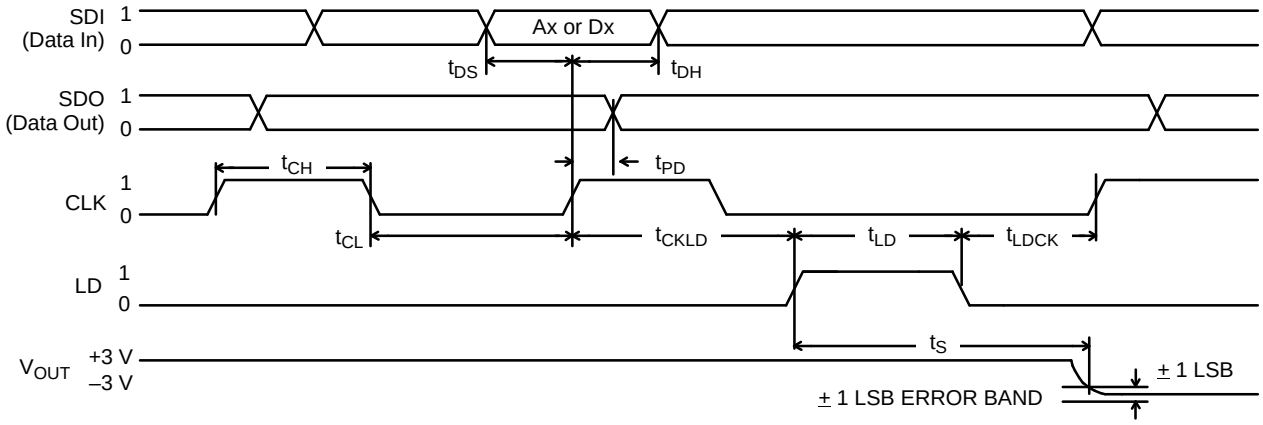



**Figure 2. Detail Serial Data Input Timing ($\overline{PR}$ = "1")**

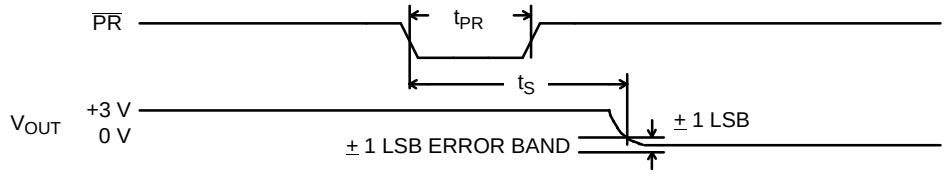



**Figure 3. PRESET Operation**

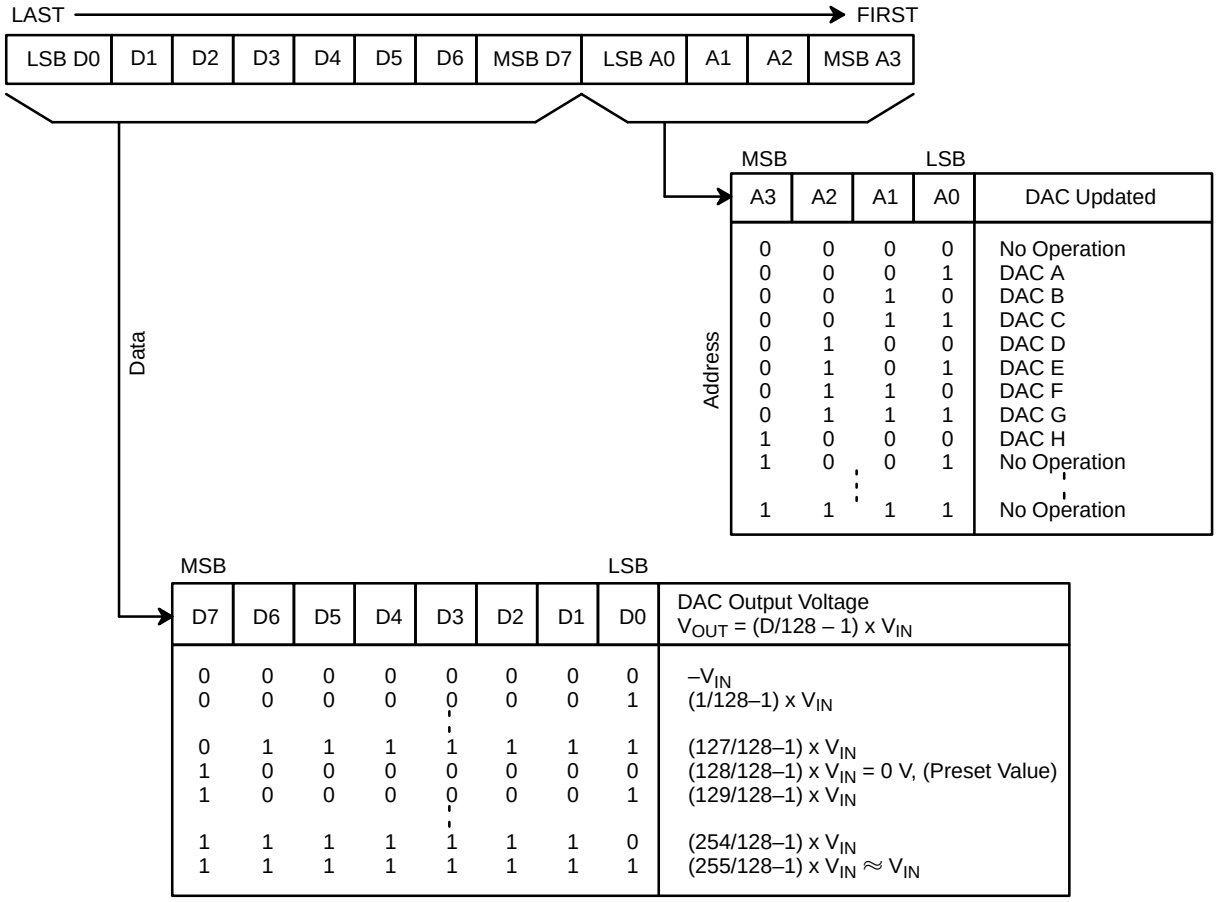



**Table 1. Serial Input Format**

| SDI | CLK | LD | $\overline{PR}$ | Input Shift Register Operation |
|---|---|---|---|---|
| X | L | L | H | No Operation |
| X | ↑ | L | H | Shift One Bit In from SDI (Pin 20), Shift One Bit* Out from SDO (Pin 18) |
| X | X | L | L | All DAC Registers = $80_H$ |
| X | L | H | H | Load Serial Register Data into DAC(X) Register |

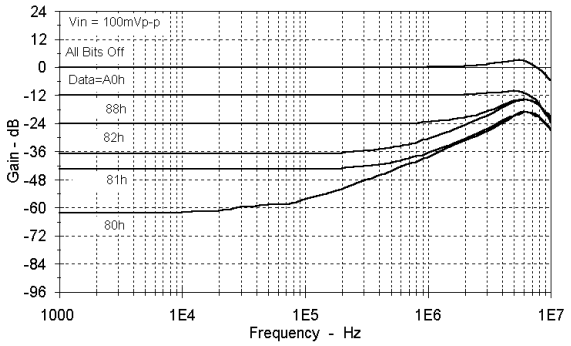
*Data shifted into the SDI pin appears twelve clocks later at the SDO pin.

**Table 2. Control Logic Truth Table**

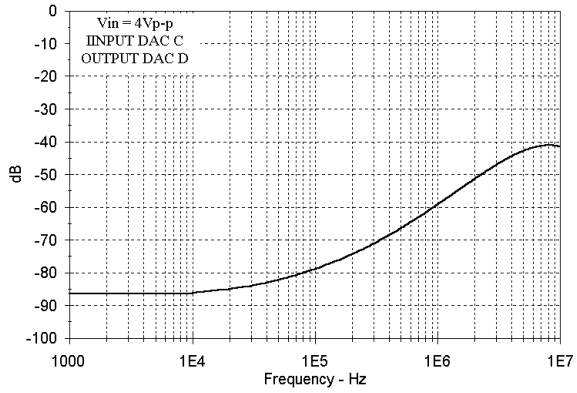
| Decimal Input (D) | $V_{OUT}$ (D) | Comments ($V_{IN}$ = 3 V) |
|---|---|---|
| 0 | –3.00 V | Inverted FS |
| 1 | –2.98 | |
| 127 | –0.02 | |
| 128 | 0.00 | Zero Output |
| 129 | 0.02 | |
| 254 | 2.95 | |
| 255 | 2.98 | Full Scale (FS) |

**Table 3. DAC Transfer Function**

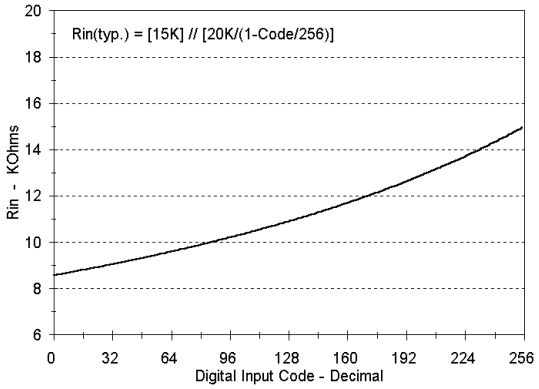
## PERFORMANCE CHARACTERISTICS



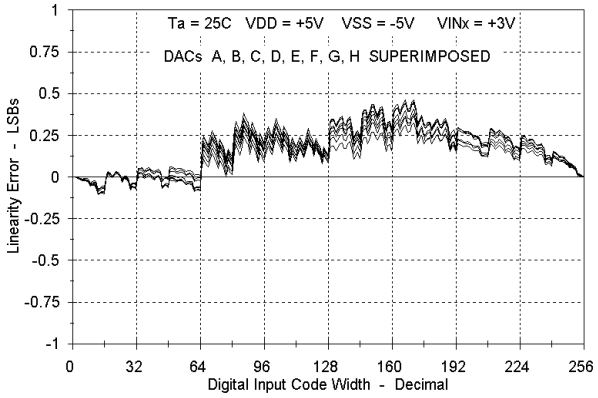

**Graph 1. Gain ($V_{OUT}/V_{IN}$) and Feedthrough vs. Frequency**



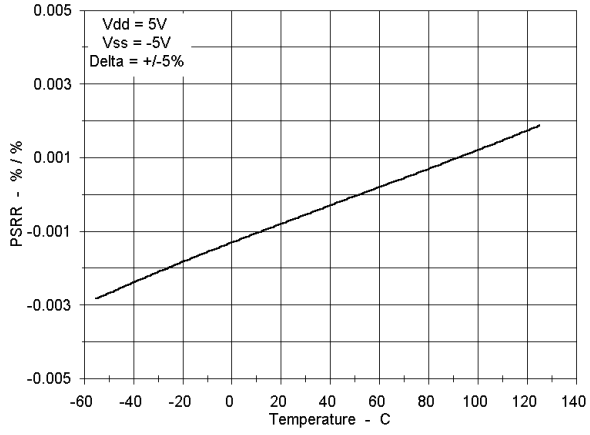

**Graph 2. DAC Crosstalk vs. Frequency**



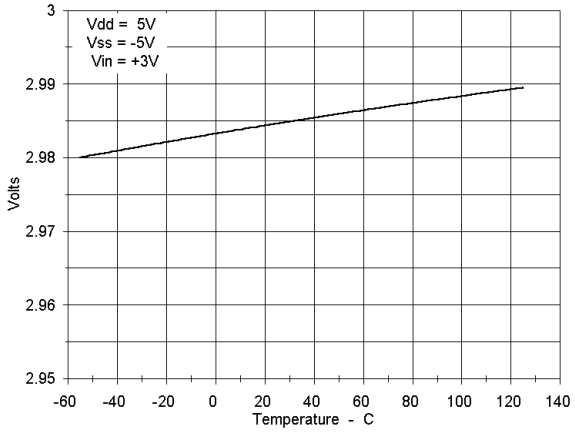

**Graph 3. DAC Input Resistance vs. Digital Input Code**



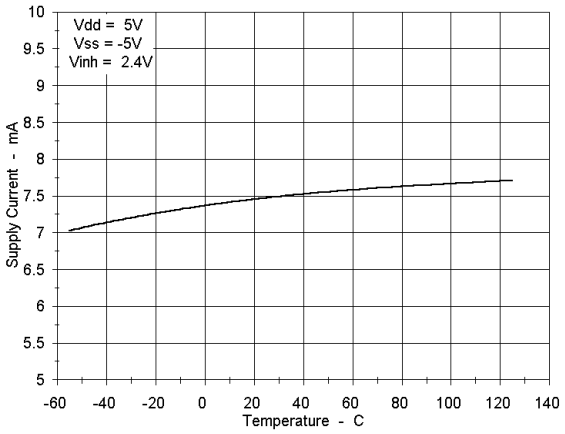

**Graph 4. Linearity Error vs. Digital Input Code**



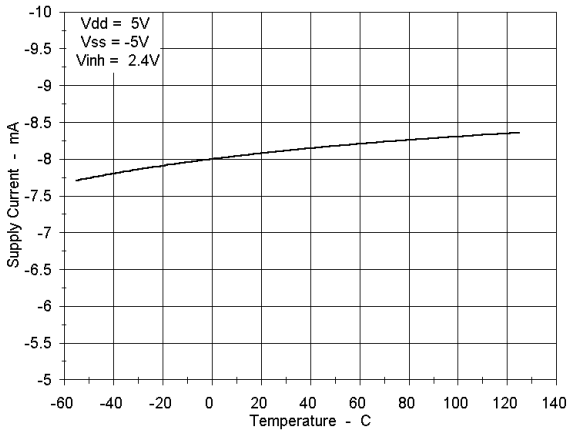

**Graph 5. PSRR (DC) vs. Temperature**



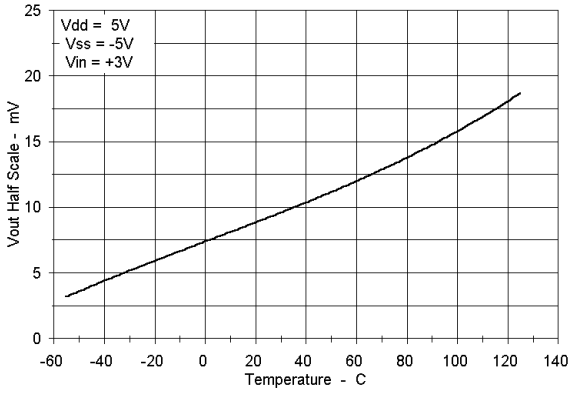

**Graph 6. $V_{OUT}$ Full Scale vs. Temperature**



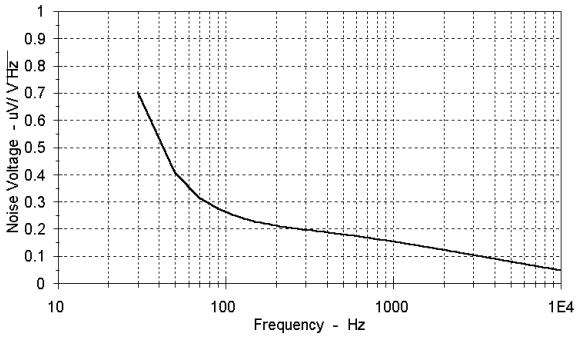

**Graph 7. Supply Current ($I_{DD}$) vs. Temperature**



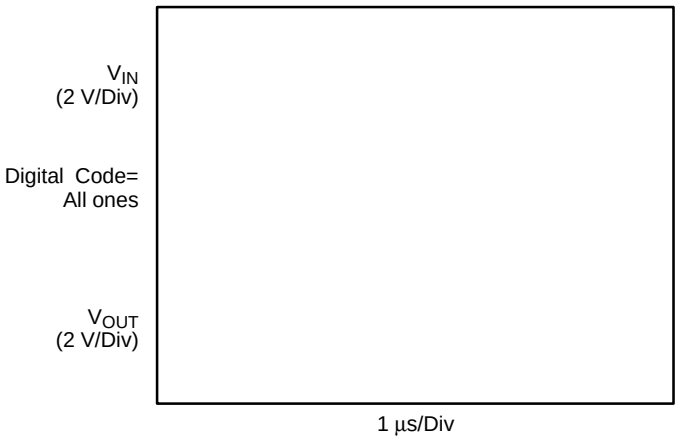

**Graph 8. Supply Current ($I_{SS}$) vs. Temperature**



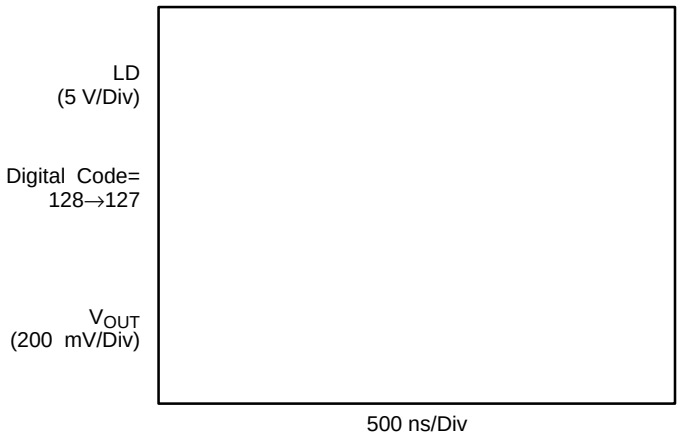

**Graph 9. $V_{OUT}$ Offset Error vs. Temperature**



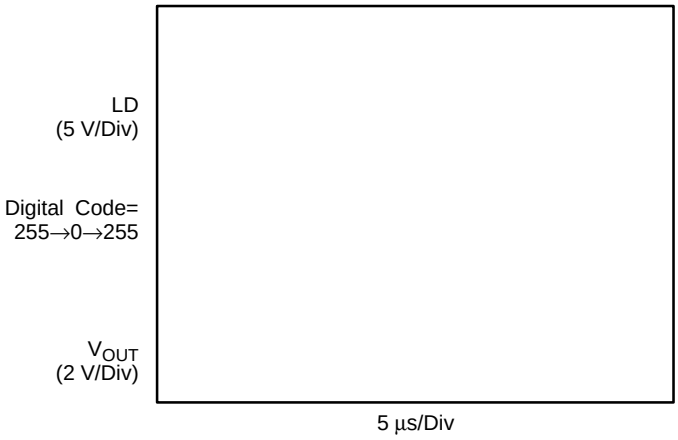

**Graph 10. Voltage Noise Density vs. Frequency**



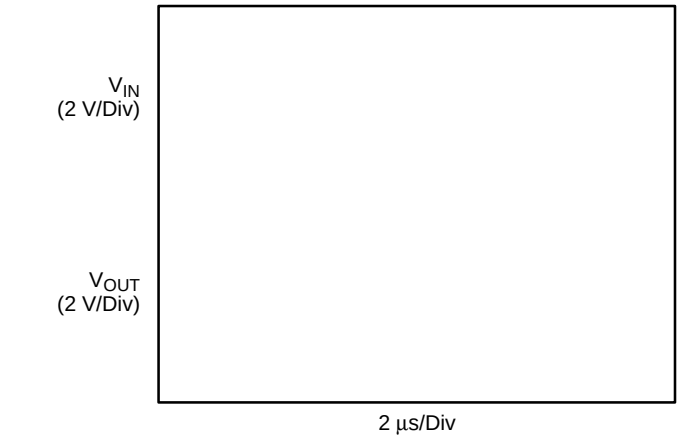

**Graph 11. Pulse Response**



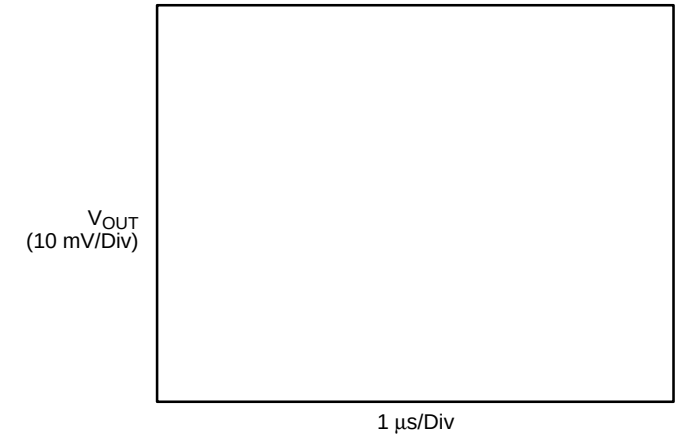

**Graph 12. 1 LSB Digital Step Change**



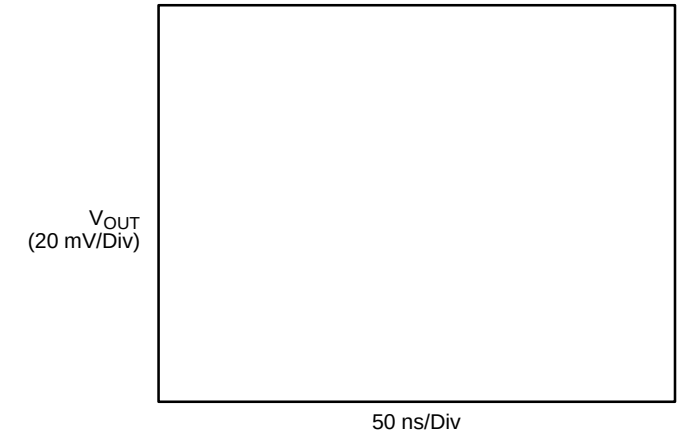

**Graph 13. Settling Time**



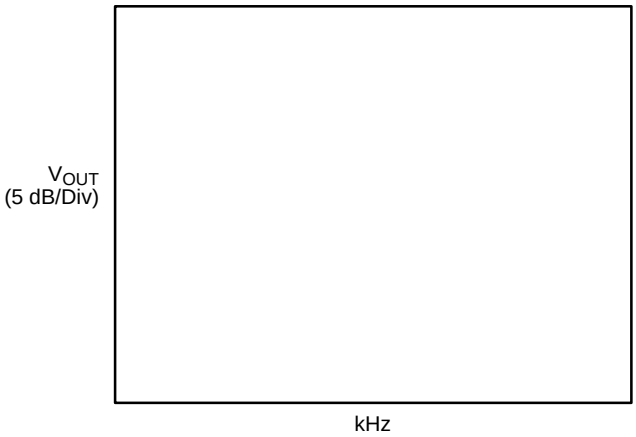

**Graph 14. 128kHz Sawtooth Waveform Response**



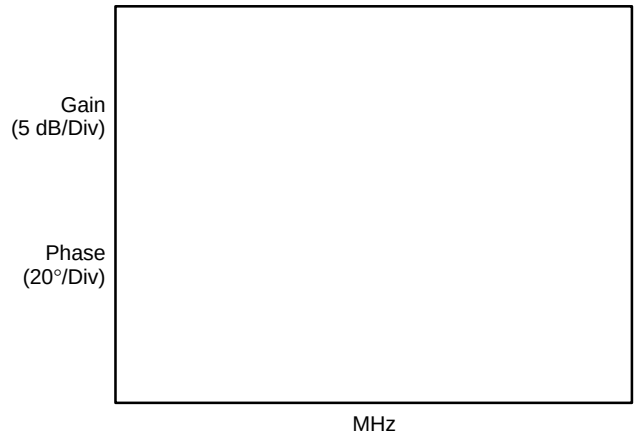

**Graph 15. Clock Feedthrough**



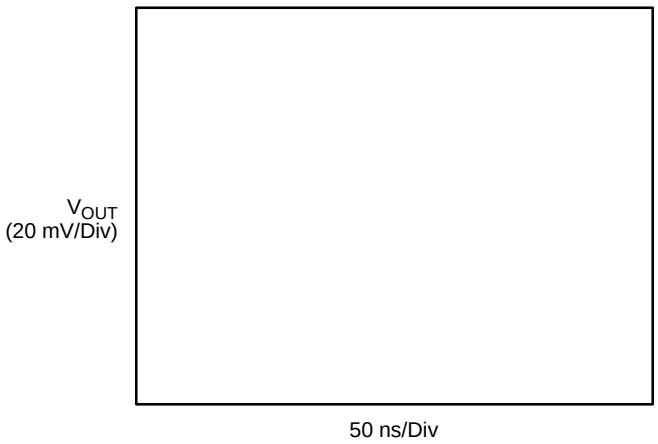

**Graph 16. Digital Crosstalk**




**Graph 17. PSRR vs. Frequency**

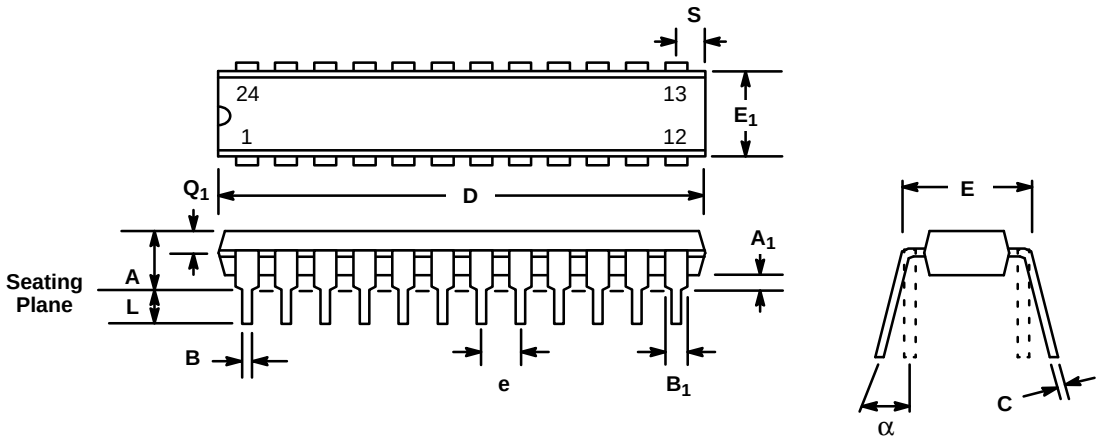



**Graph 18. Gain and Phase vs. Frequency**




**Graph 19. Digital Feedthrough**

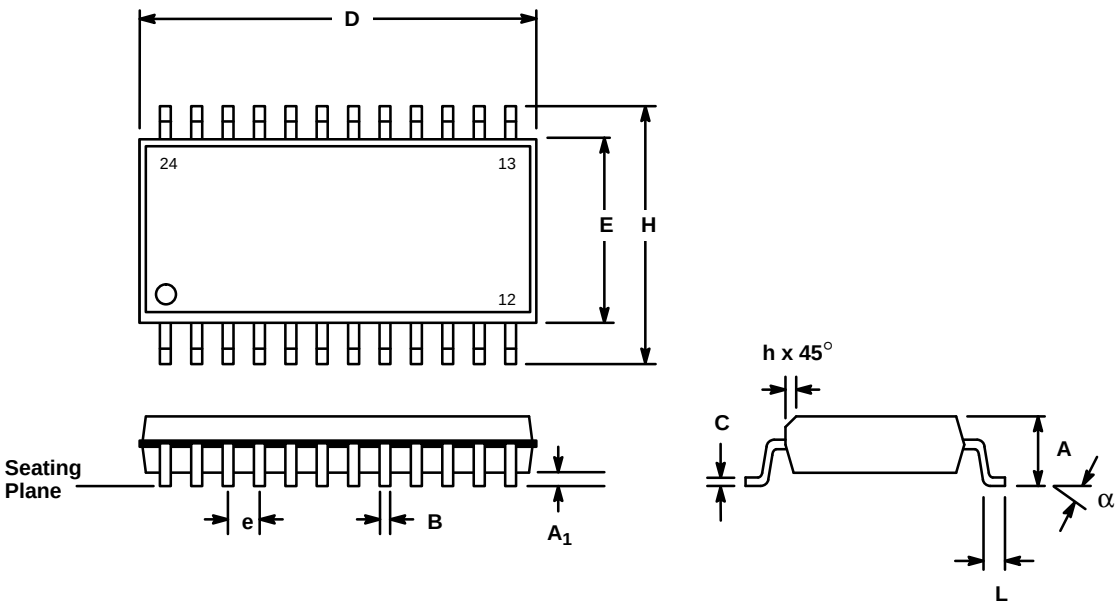
## 24 LEAD PLASTIC DUAL-IN-LINE
## (300 MIL PDIP)
## NN24




| SYMBOL | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | — | 0.200 | — | 5.08 |
| $A_1$ | 0.015 | — | 0.38 | — |
| B | 0.014 | 0.023 | 0.356 | 0.584 |
| $B_1$ (1) | 0.038 | 0.065 | 0.965 | 1.65 |
| C | 0.008 | 0.015 | 0.203 | 0.381 |
| D | 1.16 | 1.280 | 29.46 | 32.51 |
| E | 0.295 | 0.325 | 7.49 | 8.26 |
| $E_1$ | 0.220 | 0.310 | 5.59 | 7.87 |
| e | 0.100 BSC | | 2.54 BSC | |
| L | 0.115 | 0.150 | 2.92 | 3.81 |
| α | 0° | 15° | 0° | 15° |
| $Q_1$ | 0.055 | 0.070 | 1.40 | 1.78 |
| S | 0.028 | 0.098 | 0.711 | 2.49 |

Note: (1) The minimum limit for dimensions B1 may be 0.023” (0.58 mm) for all four corner leads only.

## 24 LEAD SMALL OUTLINE
## (300 MIL JEDEC SOIC)
## S24




| SYMBOL | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.097 | 0.104 | 2.464 | 2.642 |
| A1 | 0.0050 | 0.0115 | 0.127 | 0.292 |
| B | 0.014 | 0.019 | 0.356 | 0.483 |
| C | 0.0091 | 0.0125 | 0.231 | 0.318 |
| D | 0.602 | 0.612 | 15.29 | 15.54 |
| E | 0.292 | 0.299 | 7.42 | 7.59 |
| e | 0.050 BSC | | 1.27 BSC | |
| H | 0.400 | 0.410 | 10.16 | 10.41 |
| h | 0.010 | 0.016 | 0.254 | 0.406 |
| L | 0.016 | 0.035 | 0.406 | 0.889 |
| α | 0° | 8° | 0° | 8° |

# Notes

NOTICE

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