MP87L95

Low Voltage CMOS
Very Low Power 10-Bit
Analog-to-Digital Converter

FEATURES

- **3.3 V Operation**
- **10-Bit Resolution**
- **Sampling Rates from <1 kHz to 500 kHz**
- **DNL better than 1/2 LSB (typ) up to 250 kHz**
- **Very Low Power CMOS - 5 mW (typ)**
- **Power Down; Lower Consumption – 1 mW (typ)**
- **Interface to any Input Range between GND and V_{DD}**
- **No S/H Required for CCD Signals less than 250 kHz**
- **Latch-Up Free**
- **ESD Protection: 4000 Volts Minimum**

BENEFITS

- **Reliable Operation**
- **Reduced Board Space (Small Package)**
- **Reduced External Parts, No Sample/Hold Needed**
- **Suitable for Battery & Power Critical Applications**
- **Designer Can Adapt Input Range & Scaling**

APPLICATIONS

- **µP/DSP Interface and Control Applications**
- **High Resolution Imaging – Scanners, Copiers, Facsimile**
- **Multiplexed Data Acquisition**
- **Radar Pulse Analysis**
- **Low Power A/D Applications**

GENERAL DESCRIPTION

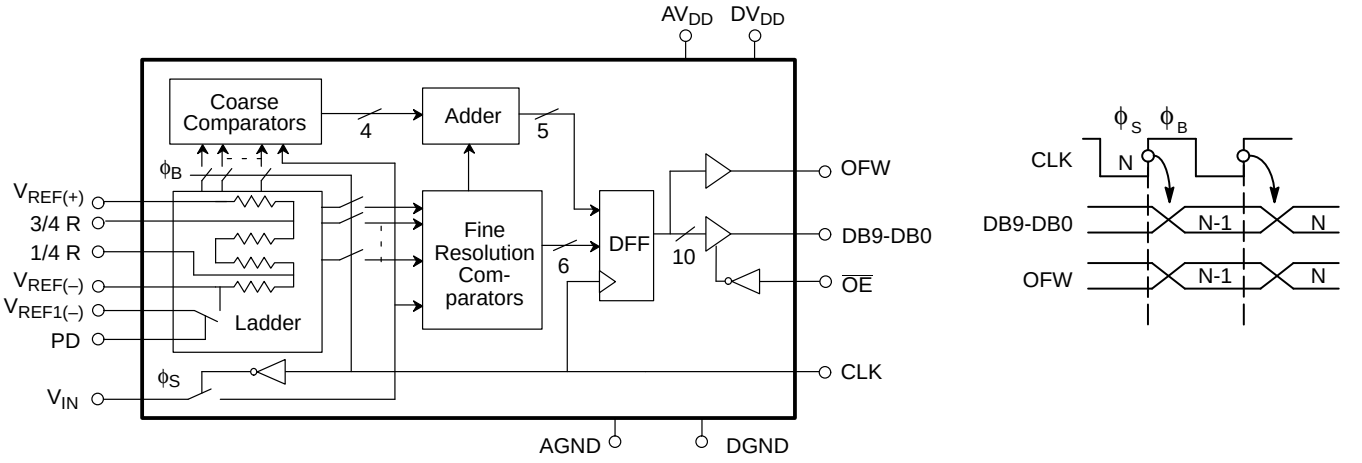
The MP87L95 is a flexible, easy to use, precision 10-bit Analog-to-Digital Converter that operates over a wide range of input and sampling conditions. The MP87L95 can operate with pulsed "on demand" conversion operation or continuous "pipeline" operation for sampling rates up to 250 kHz. The elimination of the S/H and small package size offer the designer a low cost solution. No sample and hold is required for charge couple device applications, up to 250 kHz, or multiplexed input applications when the signal source bandwidth is limited to 20 kHz. The input architecture of the MP87L95 allows direct interface to any analog input range between AGND and AV_{DD} (0 to 2 V, 3 V). The user simply sets $V_{REF(+)}$ and $V_{REF(–)}$ to encompass the desired input range.

Scaled reference resistor taps 1/4 R and 3/4 R allow for customizing the transfer curve. Digital outputs offer 3-state operation.

The MP87L95 uses a two-step flash technique. The first segment converts the 4 MSBs and consists of 15 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

When the power down input is "high", the data outputs DB9 to DB0 hold the current values and $V_{REF(–)}$ is disconnected from $V_{REF1(–)}$. The power consumption during the power down mode is approximately 1mW.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

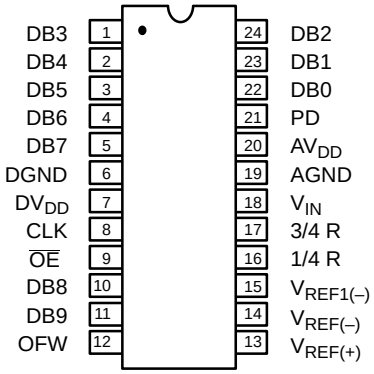


ORDERING INFORMATION

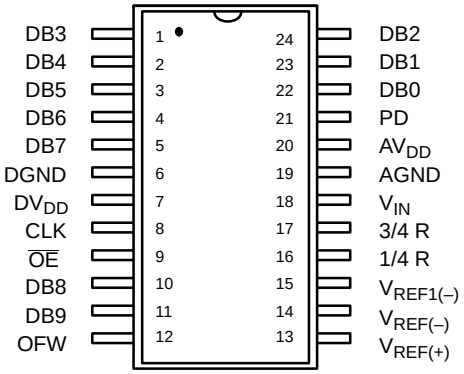
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP87L95AN	1	2
SOIC	–40 to +85°C	MP87L95AS	1	2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin PDIP (0.300")
NN24



24 Pin SOIC (Jedec, 0.300")
S24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB3	Data Output Bit 3
2	DB4	Data Output Bit 4
3	DB5	Data Output Bit 5
4	DB6	Data Output Bit 6
5	DB7	Data Output Bit 7
6	DGND	Digital Ground
7	DV_{DD}	Digital V_{DD}
8	CLK	Clock Input
9	$\overline{OE}$	Output Enable (Active Low)
10	DB8	Data Output Bit 8
11	DB9	Data Output Bit 9 (MSB)
12	OFW	Overflow Output

PIN NO.	NAME	DESCRIPTION
13	$V_{REF(+)}$	Upper Reference Voltage
14	$V_{REF(–)}$	Lower Reference Voltage
15	$V_{REF1(–)}$	Lower Reference Voltage
16	1/4 R	Reference Ladder Tap @ 1/4 FS
17	3/4 R	Reference Ladder Tap @ 3/4 FS
18	V_{IN}	Analog Signal Input
19	AGND	Analog Ground
20	AV_{DD}	Analog V_{DD}
21	PD	Power Down
22	DB0	Data Output Bit 0 (LSB)
23	DB1	Data Output Bit 1
24	DB2	Data Output Bit 2

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 3$ V, F_S = 250 KHz (50% Duty Cycle), $V_{REF(+)} = 2.6$, $V_{REF(-)}$ = AGND, $T_A = 25°C$

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		10			Bits	
Sampling Rate	F_S			0.25	MHz	For Rated Performance
ACCURACY[2]						
Differential Non-Linearity	DNL			±1	LSB	Best Fit Line (Max INL – Min INL)/2
Integral Non-Linearity	INL			±2	LSB	
Zero Scale Error	EZS		+1.00		LSB	Reference from $V_{REF(+)}$ to $V_{REF(-)}$
Full Scale Error	EFS		–2.5		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	$V_{REF(+)}$			AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			V	
Differential Ref. Voltage[5]	V_{REF}	0.5		AV_{DD}	V	
Ladder Resistance	R_L	525	675	900	Ω	
Ladder Temp. Coefficient[1]	R_{TCO}		2000		ppm/°C	
Ladder Switch Resistance[1]			12		Ω	
Ladder Switch Off Leakage	$I_{ILKG-SW}$		50		nA	
ANALOG INPUT[1]						
Input Voltage Range[7]	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V	
Input Capacitance[3]	C_{IN}		60		pF	
Aperture Delay	t_{AP}		60	70	ns	
DIGITAL INPUTS						
Logical “1” Voltage	V_{IH}	2.5			V	
Logical “0” Voltage	V_{IL}			0.5	V	
Leakage Currents	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK				±100	µA	
PD, $\overline{OE}$ (Internal Res to DGND)		–5		30	µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1.*)[1]						
Clock Period	T_S	4			µs	
Rise & Fall Time[4]	t_R, t_F			10	ns	
“High” Time[6]	t_B	2		1000	µs	
“Low” Time[6]	t_S	2		1000	µs	Functional
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical “1” Voltage	V_{OH}	V_{DD}-0.5			V	I_{LOAD} = 1 mA
Logical “0” Voltage	V_{OL}			0.5	V	I_{LOAD} = 1 mA
3-state Leakage	I_{OZ}			±5	µA	V_{OUT} = DGND to DV_{DD}
Data Hold Time (*See Figure 1.*)[1]	t_{HLD}		50	60	ns	
Data Valid Delay[1]	t_{DL}		60	70	ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS (CONT'D)						C_{OUT}=15 pF
Data Enable Delay[1]	t_{DEN}		35	40	ns	
Data 3-state Delay[1]	t_{DHZ}		30	40	ns	
Clock to PD Set-up Time	t_{CLKS1}			400	ns	
Clock to PD Hold Time	t_{CLKH1}			600	ns	
Power Down Delay	t_{PD}			300	ns	
Power Up Delay	t_{PU}			200	ns	
POWER SUPPLIES[8]						
Power Down (I_{DD})	I_{DDOWN}		0.3	1.2	mA	
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	3	3.3	3.6	V	
Current (AV_{DD} + DV_{DD})	I_{DD}			3	mA	V_{IN} = 2 V

NOTES:
1. Guaranteed. Not tested.
2. Tester measures code transition voltages by dithering the voltage of the analog input (V_{IN}). The difference between the measured code width and the ideal value (V_{REF}/1024) is the DNL error (*see Figure 5.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*See Figure 7.*).
3. See V_{IN} input equivalent circuit (*see Figure 9.*).
4. Clock specification to meet aperture specification (t_{AP}). Actual rise/fall time can be less stringent with no loss of accuracy.
5. Specified values guarantee functional device. Refer to other parameters for accuracy.
6. System can clock MP87L95 with any duty cycle as long as all timing conditions are met.
7. Input range where input is converted correctly into binary code. Input voltage outside specified range converts to zero or full scale output.
8. DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} (to GND) ..... +5.5 V
$V_{REF(+)}$ & $V_{REF(–)}$ ..... GND –0.5 to V_{DD} +0.5 V
V_{IN} ..... GND –0.5 to V_{DD} +0.5 V
All Inputs ..... GND –0.5 to V_{DD} +0.5 V
All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
PDIP, SOIC 1000mW
Derates above 75°C ..... 14mW/°C

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3. V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

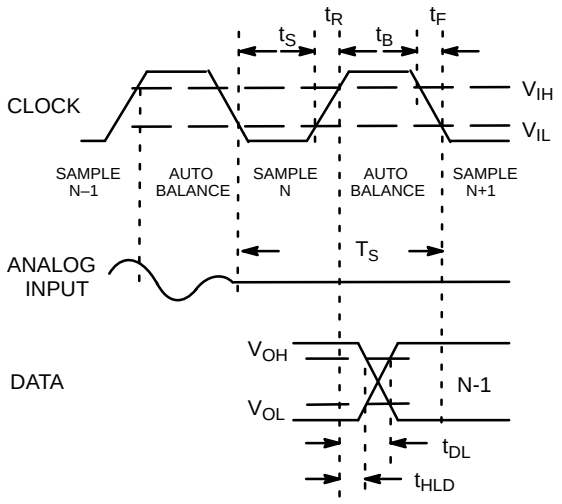


Figure 1. MP87L95 Timing Diagram

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP87L95 converts analog voltages into 1024 digital codes by encoding the outputs of 15 coarse and 67 fine comparators. Digital logic is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 2 clock periods.

The reference resistance ladder is a series of 1025 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 1024 * R \quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 1024 * LSB$

The clock signal generates the two internal phases, ϕ_B (CLK high) and ϕ_S (CLK low = sample) (*See Figure 2.*). The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The coarse comparators make the first pass conversion and select a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next ϕ_B phase.

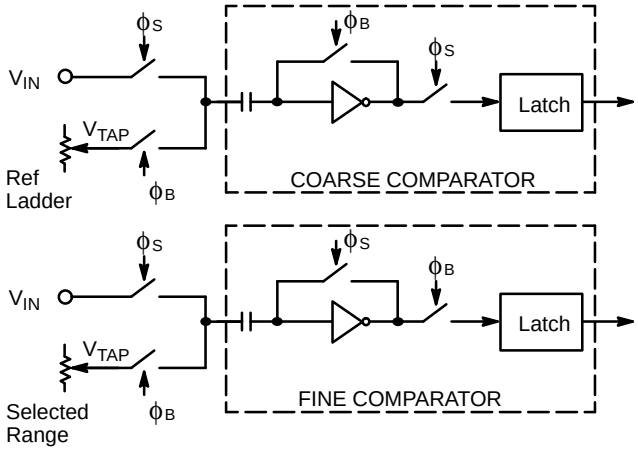


Figure 2. MP87L95 Comparators

A_{IN} Sampling, Ladder Sampling, and Conversion Timing

Figure 3. shows this relationship as a timing chart. A_{IN} sampling, ladder sampling and output data relationships are shown for the general case where the levels which drive the ladder need to change for each sampled A_{IN} time point. The ladder is referenced for both last A_{IN} sample and next A_{IN} sample at the same time. If the ladder's levels change by more than 1 LSB, one of the samples must be discarded. Also note that the clock low period for the discarded A_{IN} can be reduced to the minimum t_S time of 150 ns.

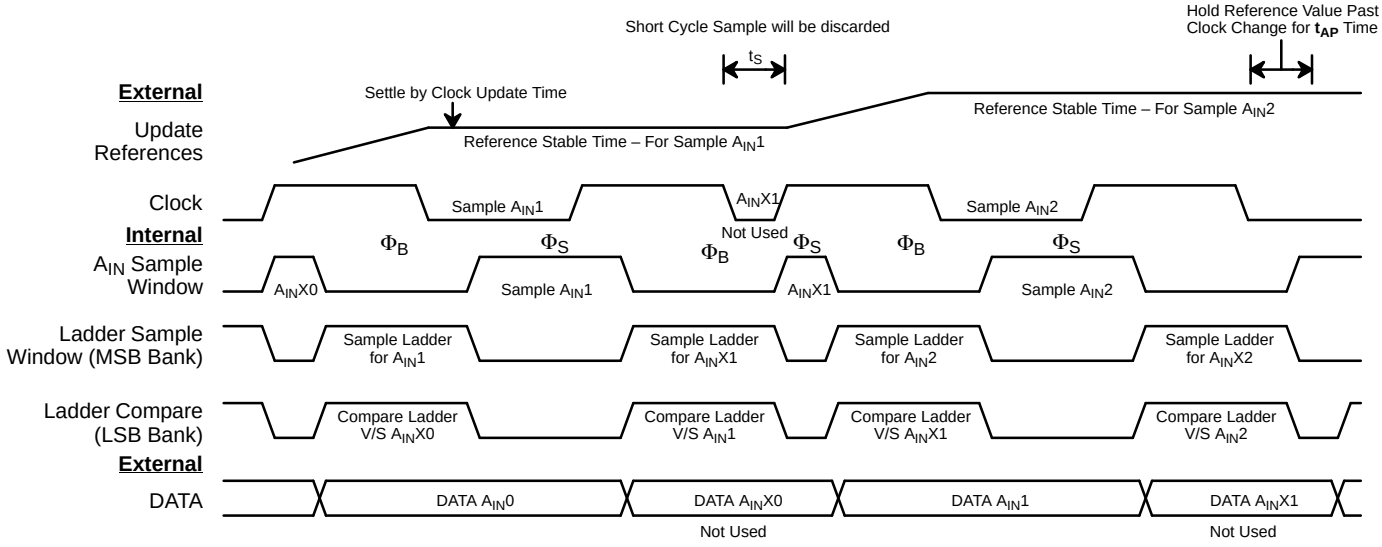


Figure 3. A_{IN} Sampling, Ladder Sampling & Conversion Timing

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 4.*

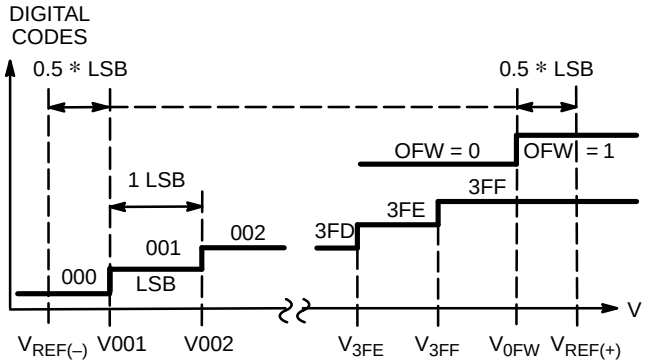


Figure 4. Ideal A/D Transfer Function

The overflow transition (V_{OFW}) takes place at:

$V_{IN} = V_{OFW} = V_{REF(+)} – 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V001 = V_{REF(–)} + 0.5 * LSB$

$V_{IN} = V_{3FF} = V_{REF(–)} – 1.5 * LSB$

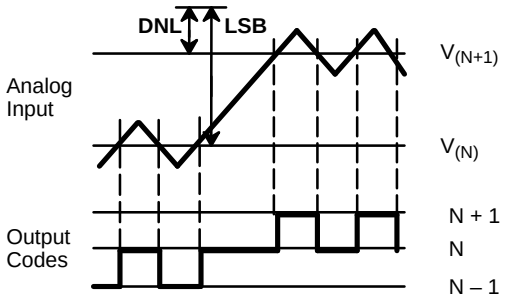
$LSB = V_{REF} / 1024 = (V_{3FF} – V001) / 1022$

Note that the overflow transition is a flag and has no impact on the data bits.

In a “real” converter the code-to-code transitions don’t fall exactly every V_{REF}/1024 volts.

A positive DNL (Differential Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSB’s.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = $\pm$ 0.5 LSB means that all code widths are within 0.5 and 1.5 LSB. If V_{REF} = 4.608 V then 1 LSB = 4.5 mV and every code width is within 2.25 and 6.75 mV.



(N+1) Code Width = $V_{(N+1)} – V_{(N)}$
LSB = [$V_{REF(+)} – V_{REF(–)}$] / 1024

$DNL_{(N)} = [V_{(N+1)} – V_{(N)}] – LSB$

Figure 5. DNL Measurement On Production Tester

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (E_{ZS}, E_{FS}) are:

DNL (001) = V002 – V001 – LSB

: : :

DNL (3FE) = $V_{3FF} – V_{3FE}$ – LSB

E_{FS} (full scale error) = $V_{3FF} – [V_{REF(+)} –1.5 * LSB]$

E_{ZS} (zero scale error) = $V_{001} – [V_{REF(–)} + 0.5 * LSB]$

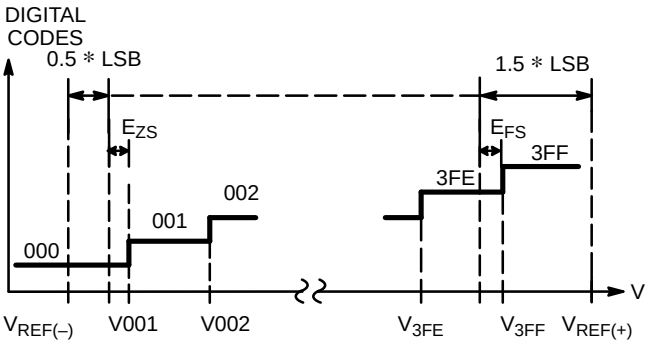


Figure 6. Real A/D Transfer Curve

Figure 6. shows the zero scale and full scale error terms.

Figure 7. gives a visual definition of the INL error. The chart shows a 3-bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, the computer draws a line parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and the negative INL errors. For example, an INL error of –1 to +2 LSBs relative to the Ideal Line would be ±1.5 LSB's relative to the best fit line.

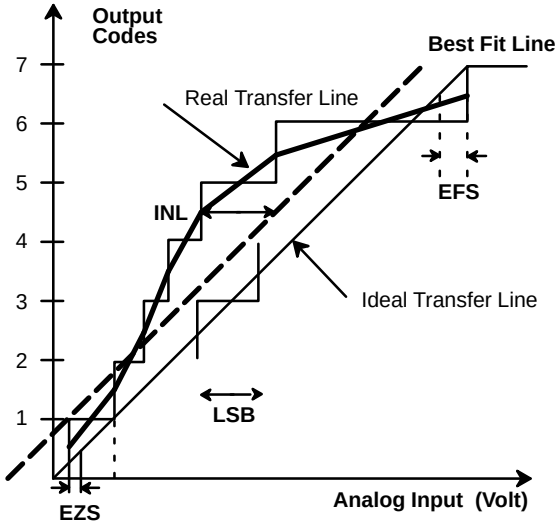


Figure 7. INL Error Calculation

Clock and Conversion Timing

A system will clock the MP87L95 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 8a* shows normal operation, while the timing of *Figure 8b* keeps the MP87L95 in balance and ready to sample the analog input.

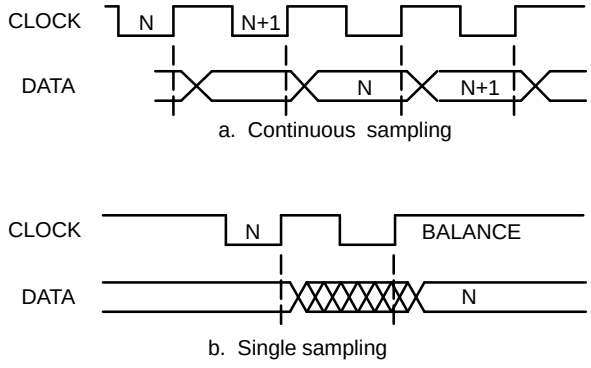


Figure 8. Relationship of Data to Clock

Analog Input

Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP87L95's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. These have an impact above 5 MHz and they are very important above 10 MHz. Use of Current Feedback Amplifiers is an easy and cost effective way to maximize performance.

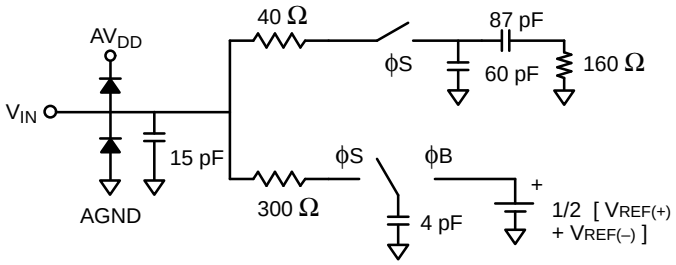


Figure 9. Analog Input Equivalent Circuit

Reference Voltages

The input/output relationship is a function of V_{REF}:

$$A_{IN} = V_{IN} - V_{REF(-)}$$
$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$
$$DATA = 1023 * (A_{IN}/V_{REF})$$

A system can increase total gain by reducing V_{REF}.

Digital Interfaces

The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output. The input $\overline{OE}$ controls the output buffers in an asynchronous mode.

$\overline{OE}$	OFW	DB9 – DB0
1	Valid	High Z
0	Valid	Valid

Table 1. Output Enable Logic

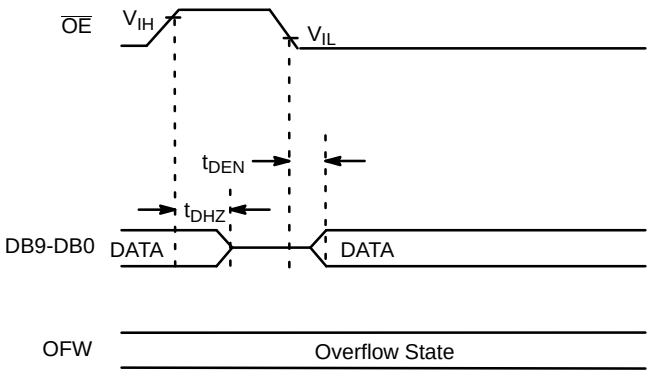


Figure 10. Output Enable/Disable Timing Diagram

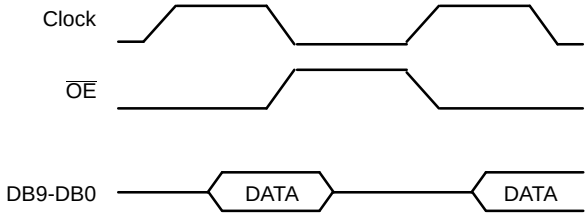


Figure 11. Preferred Output Control

Figure 11. shows the preferred output control where $\overline{OE}$ and clock are opposite phase. This provides a quiet time at the end of the A_{IN} sample phase.

The functional equivalent of the MP87L95 (*Figure 12.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An ideal analog switch which samples V_{IN}.
3) An ideal A/D which tracks and converts V_{IN} with no delay.
4) A series of two DFF's with specified hold (t_{HLD}) and delay (t_{DL}) times.

t_{AP}, t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

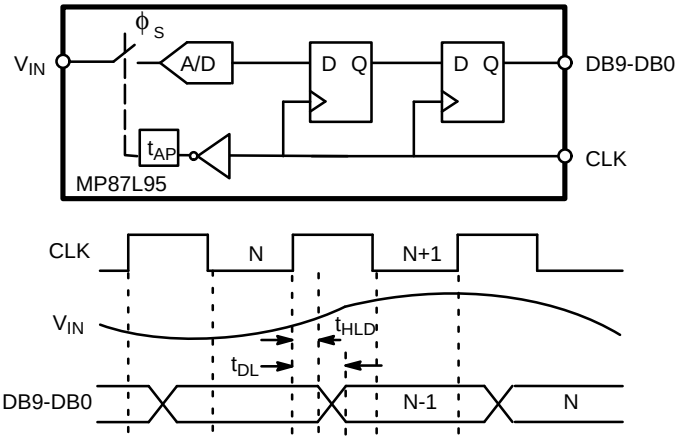


Figure 12. MP87L95 Functional Equivalent Circuit and Interface Timing

Power Down

Figure 13. shows the relationship between the clock, sampled A_{IN} to output data relationship and the effect of power down.

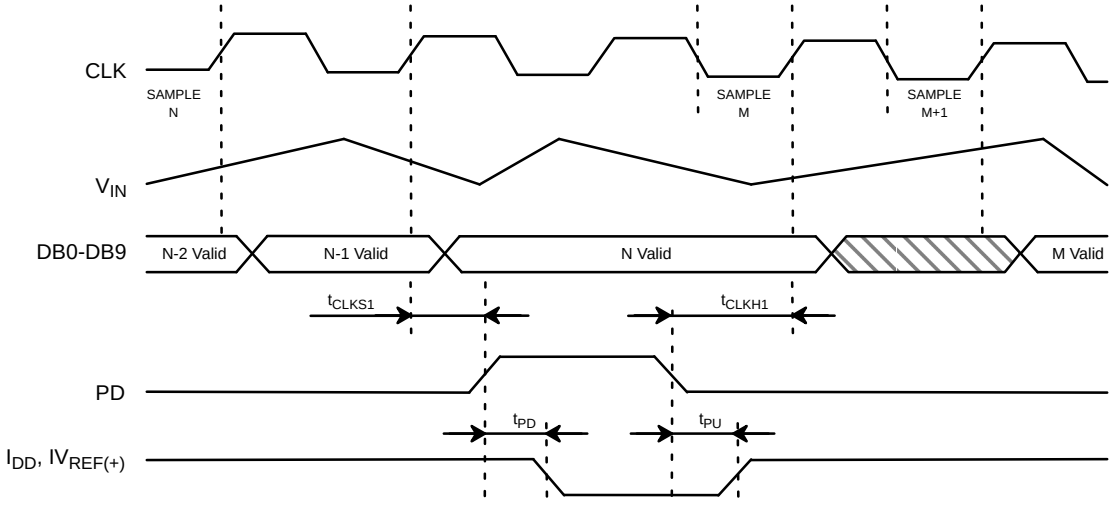


Figure 13. Power Down Timing Diagram

APPLICATION NOTES

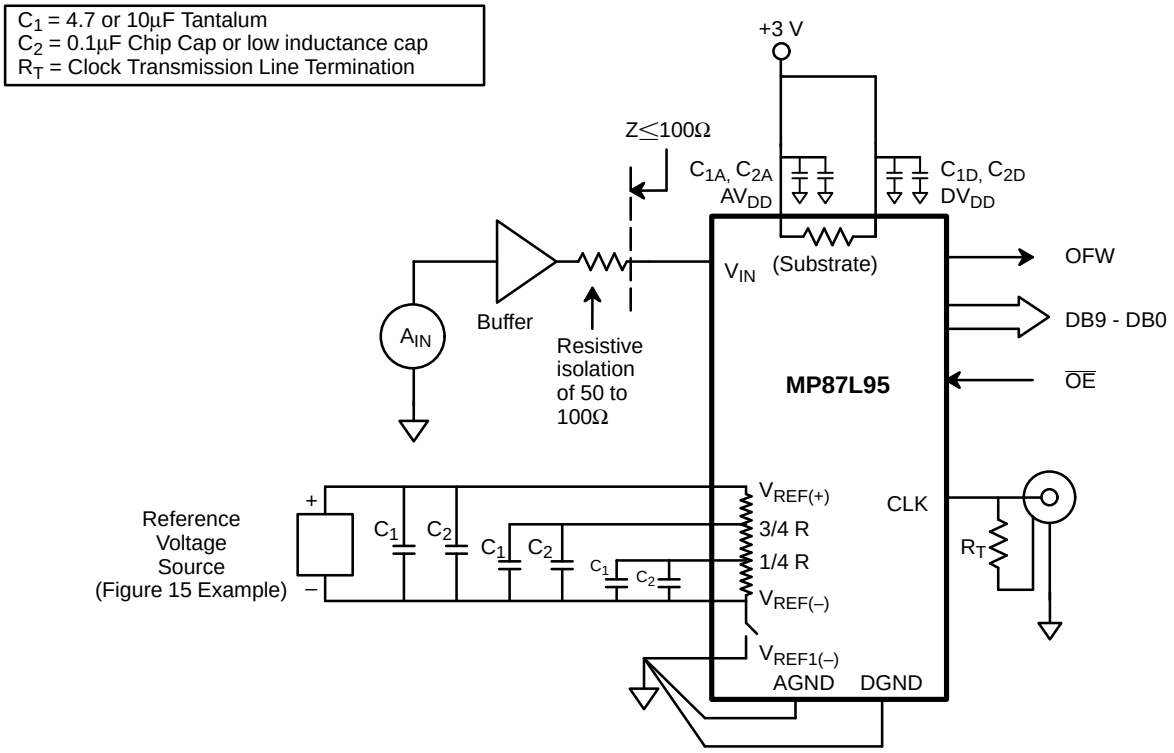


Figure 14. Typical Circuit Connections

The following information will be useful in maximizing the performance of the MP87L95.

1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V or DGND –0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP87L95 inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP87L95. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths. *DGND should not be shared with other digital circuitry.* If separate low impedance paths cannot be provided, DGND should be connected to AGND next to the MP87L95.
7. *DV_{DD} should not be shared with other digital circuitry* to avoid conversion errors caused by digital supply transients. DV_{DD} for the MP87L95 should be connected to AV_{DD} next to the MP87L95.
8. DV_{DD} and AV_{DD} are connected inside the MP87L95 through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used. 100Ω resistors in series with the digital outputs in some applications reduces the digital output disruption of A_{IN}.

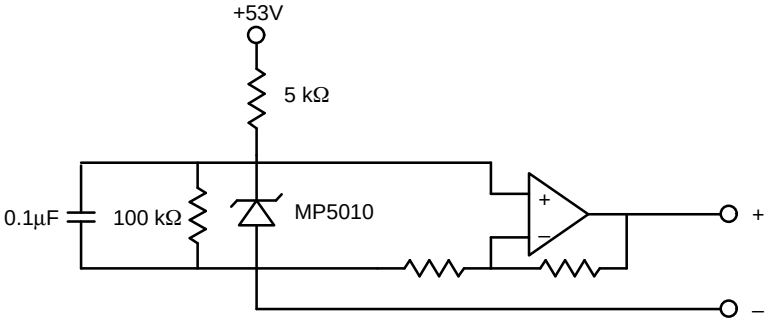
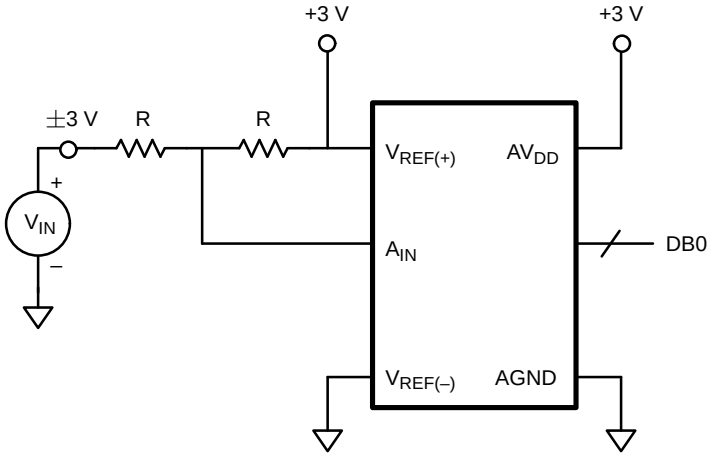


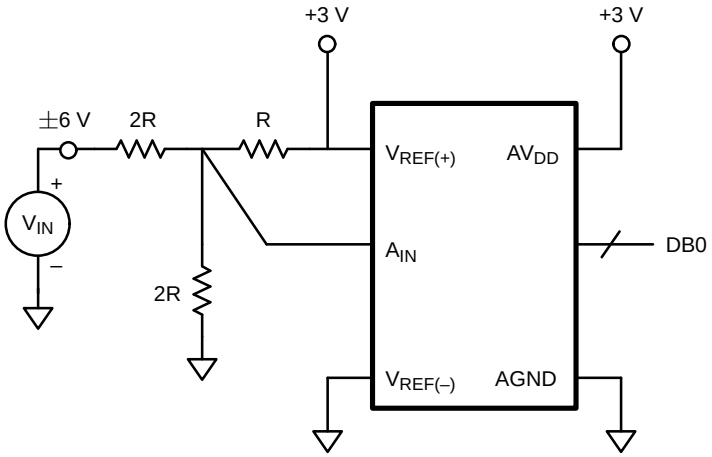
Figure 15. Example of a Reference Voltage Source



For R = 5k use Beckman Instructions #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the (R ∗ C_{IN} of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

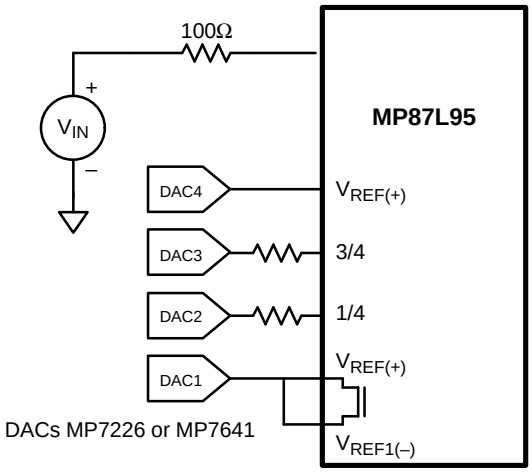
Figure 16. ±3 V Analog Input



For R = 5k use Beckman Instructions #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the (R ∗ C_{IN} of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

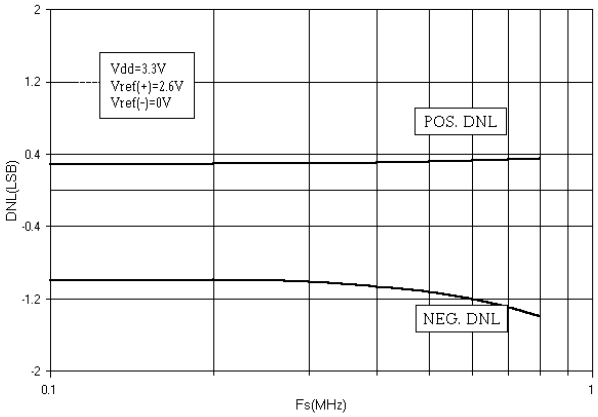
Figure 17. ±6 V Analog Input



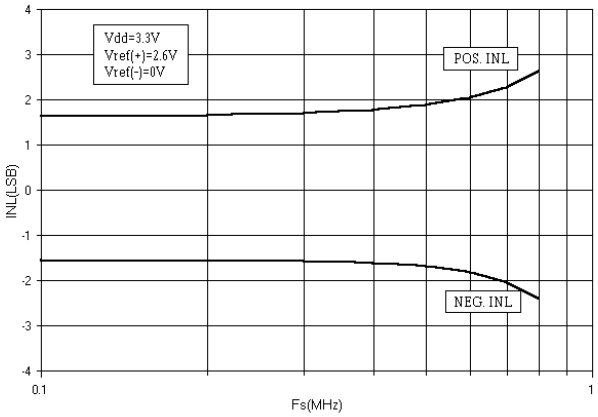
@ Power Down write values to DAC 3, 2, 1 = DAC 4 to minimize power consumption.
Only A_{IN} and Ladder detail shown.

Figure 18. A/D Ladder with Programmed Control (of $V_{REF(+)}$, $V_{REF(–)}$, 1/4 and 3/4 TAP.)

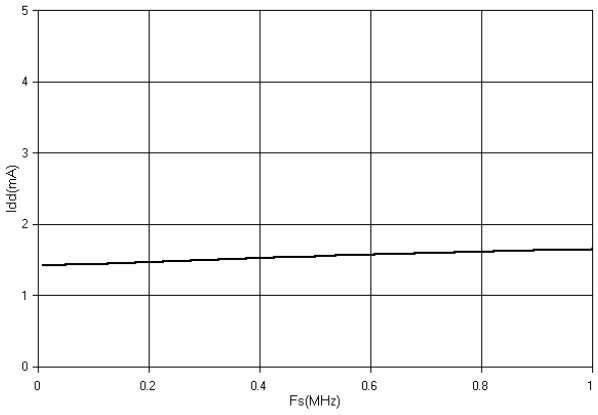
PERFORMANCE CHARACTERISTICS



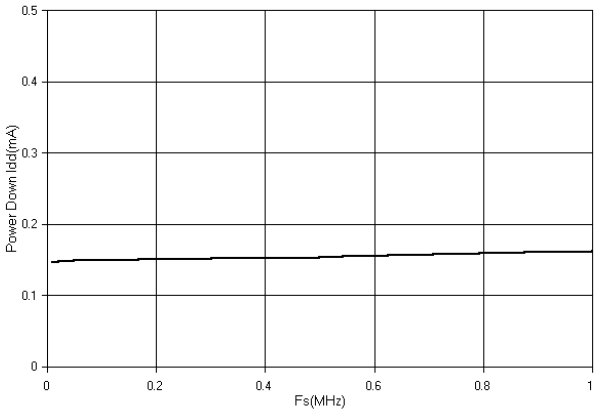
Graph 1. DNL vs. Sampling Frequency



Graph 2. INL vs. Sampling Frequency

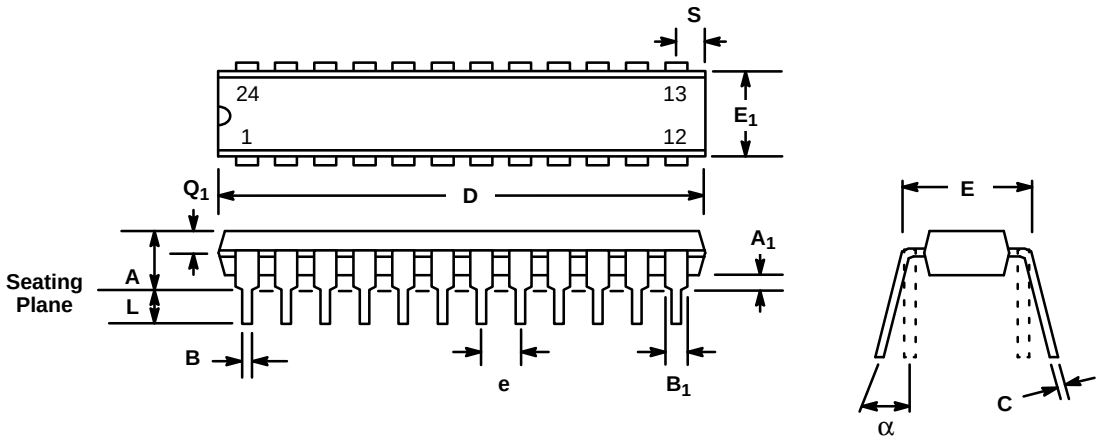


Graph 3. Supply Current vs. Sampling Frequency



Graph 4. Power Down Current vs. Sampling Frequency

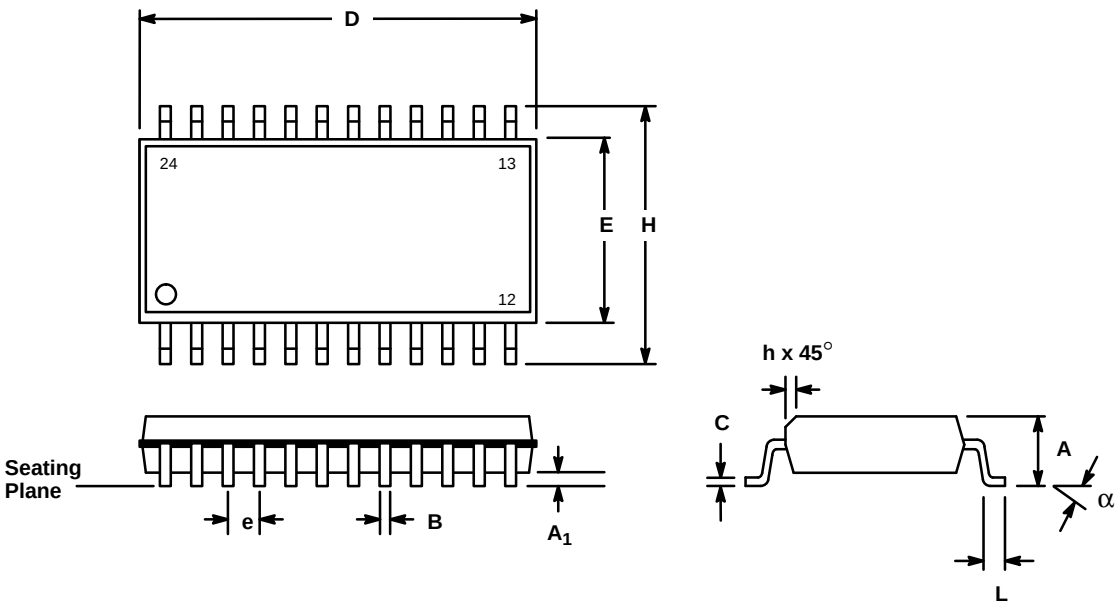
24 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
NN24



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.16	1.280	29.46	32.51
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.028	0.098	0.711	2.49

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

24 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S24



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.642
A1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.602	0.612	15.29	15.54
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

Notes

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