



MP87L91

Low Voltage CMOS 12-Bit
High Speed Analog-to-Digital Converter
with Parallel Logic Interface Port

FEATURES

- 3.3 V Operation
- 12-Bit ADC with DNL = ± 1 LSB, INL = ± 2 LSB
- Sampling Frequency 1 MHz (typ)
- Rail-to-Rail Input Range
- V_{REF} Range: 1.5 V to V_{DD}
- CMOS Low Power: 25 mW (typ)
- 1/4, 1/2 and 3/4 Scale Reference Resistor Taps
- Three-State Outputs
- Binary and Two's Complement Digital Output Mode

APPLICATIONS

- Instrumentation
- Medical Imaging
- Ultrasound
- Magnetic Resonance Signal Acquisition
- Digital Oscilloscopes
- Spectrum Analysis

GENERAL DESCRIPTION

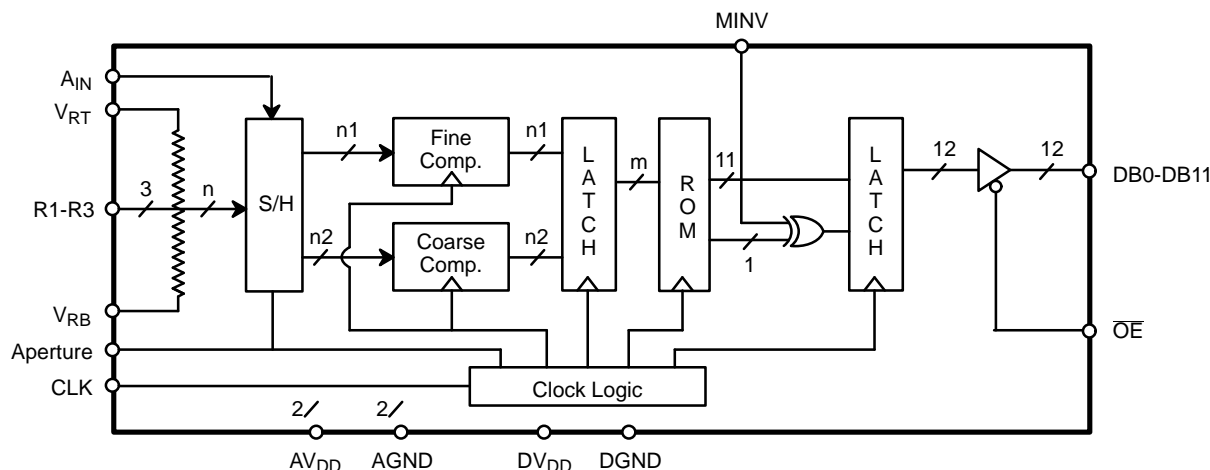
The MP87L91 is a monolithic 1 MSPS 12-bit 2-step flash Analog-to-Digital Converter with DNL = ± 1 LSB and INL = ± 2 LSB. The MP87L91 contains an internal track and hold.

The MP87L91 operates with a single 3.3 V supply while consuming less than 25 mW of power (typical). Separate pins for reference ladder terminals and power supplies allow

flexibility for various A_{IN} , ΔV_{REF} , and power supply ranges.

Data is presented at the parallel output port every clock cycle after a 2.5 cycle pipeline delay from sample edge. Also, the digital output port is equipped with a 3-state function. MINV enables binary and 2's complement data formatting. Through pins R1-R3, transfer function adjustment, linearity, and speed enhancement can be accommodated.

SIMPLIFIED BLOCK DIAGRAM

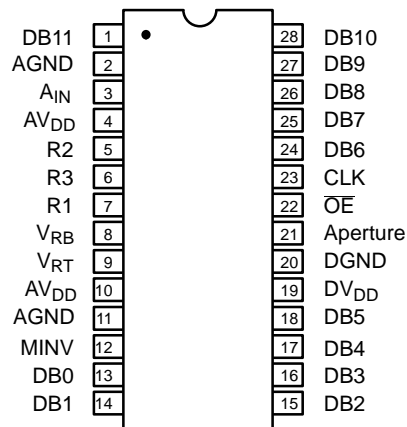


ORDERING INFORMATION

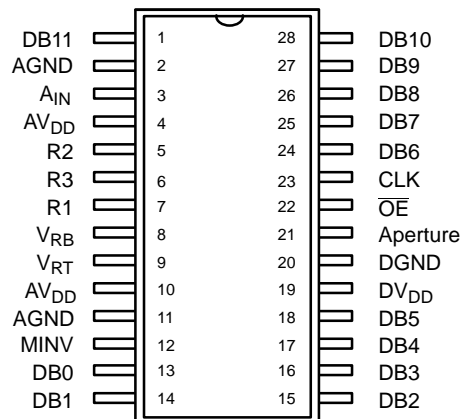
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PDIP	-40 to +85°C	MP87L91AN	±1	2 1/2
SOIC	-40 to +85°C	MP87L91AS	±1	2 1/2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP (0.600")
N28



28 Pin SOIC (EIAJ, 0.335")
R28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB11	Data Output Bit 11 (MSB)
2	AGND	Analog Negative Supply
3	A _{IN}	Analog Input
4	AV _{DD}	Analog Positive Supply
5	R2	Ref. Resistor Ladder Tap (1/2 V _{REF})
6	R3	Ref. Resistor Ladder Tap (3/4 V _{REF})
7	R1	Ref. Resistor Ladder Tap (1/4 V _{REF})
8	V _{RB}	Negative Reference
9	V _{RT}	Positive Reference
10	AV _{DD}	Analog Positive Supply
11	AGND	Analog Negative Supply
12	MINV	Invert MSB (Active High)
13	DB0	Data Output Bit 0 (LSB)
14	DB1	Data Output Bit 1

PIN NO.	NAME	DESCRIPTION
15	DB2	Data Output Bit 2
16	DB3	Data Output Bit 3
17	DB4	Data Output Bit 4
18	DB5	Data Output Bit 5
19	DV _{DD}	Digital Positive Supply
20	DGND	Digital Negative Supply
21	Aperture	Delayed Clock, indicates sample point
22	OE	Output Enable (Active Low)
23	CLK	Clock
24	DB6	Data Output Bit 6
25	DB7	Data Output Bit 7
26	DB8	Data Output Bit 8
27	DB9	Data Output Bit 9
28	DB10	Data Output Bit 10

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 3\text{ V}$, $FS = 1\text{ MHz}$ (50% Duty Cycle),
 $V_{RT} = 3.0\text{ V}$, $V_{RB} = AGND$, $TA = 25^{\circ}\text{C}$

Parameter	Symbol	Min	25°C Typ	Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		12			Bits	
Sampling Rate	FS			1	MHz	
ACCURACY ¹						
Differential Non-Linearity	DNL			±1	LSB	Best Fit Line (Max INL – Min INL)/2
Integral Non-Linearity	INL			2 1/2	LSB	
Zero Scale Error	EZS		+20		LSB	
Full Scale Error	EFS		–20		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	V _{REF(+)}	0.5		A _{VDD}	V	
Negative Ref. Voltage	V _{REF(–)}	AGND			V	
Differential Ref. Voltage ³	V _{REF}	1.5		V _{DD}	V	
Ladder Resistance	R _L		550		Ω	
ANALOG INPUT						
Input Voltage Range	V _{IN}	V _{REF(–)}		V _{REF(+)}	V p-p	Aperture pin load 5 pF. Measured at 50% point.
Input Capacitance Sample ⁵	C _{IN}		50		pF	
Input Capacitance Convert ⁵			8		pF	
Aperture Delay from Clock	t _{AP}		55	60	ns	
Aperture Delay from Aperture Signal	t _{AP}		0		ns	
DIGITAL INPUTS						
Logical “1” Voltage	V _{IH}	2.5			V	V _{IN} =DGND to DV _{DD}
Logical “0” Voltage	V _{IL}			0.5	V	
Leakage Currents ⁶	I _{IN}				μA	
CLK, \overline{OE} , MINV			10		μA	
Input Capacitance			5		pF	
Clock Timing						
Clock Period	t _S		1		μs	
Rise & Fall Time ⁷	t _R , t _F		15		ns	
“High” Time	t _{PWH}		500		ns	
“Low” Time	t _{PWL}		500		ns	
Duty Cycle			50		%	
DIGITAL OUTPUTS						
Logical “1” Voltage	V _{OH}	DV _{DD} -0.5			V	C _{OUT} =15 pF I _{LOAD} = 1 mA I _{LOAD} = 1 mA V _{OUT} =DGND to DV _{DD}
Logical “0” Voltage	V _{OL}			0.5	V	
3-state Leakage	I _{OZ}		1		μA	
Data Valid Delay ²	t _{DL}		65	75	ns	
Data Enable Delay	t _{DEN}		60	75	ns	
Data 3-state Delay	t _{DHZ}		60		ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	Min	25°C Typ	Max	Units	Test Conditions/Comments
POWER SUPPLIES⁸ (T _{min} to T _{max})						
Operating Voltage (AV _{DD} , DV _{DD})	V _{DD}	3	3.3	3.6	V	
Current (AV _{DD} + DV _{DD})	I _{DD}			12	mA	
AC PARAMETERS						
Signal Noise Ratio	SNR		66		dB	

NOTES

- ¹ Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/4096) is the DNL error. The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage. Accuracy is a function of the sampling rate (FS).
- ² Guaranteed. Not tested.
- ³ Specified values guarantee functionality. Refer to other parameters for accuracy.
- ⁴ -3 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.
- ⁵ Switched capacitor analog input requires driver with low output resistance.
- ⁶ All inputs have diodes to DV_{DD} and DGND. Input(s) OE and MINV have internal pull down(s). Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.
- ⁷ Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.
- ⁸ AGND & DGND pins are connected through the silicon substrate.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)^{1, 2, 3}

V _{DD} to GND	5.5 V	Storage Temperature	-65 to +150°C
V _{REF} (+) & V _{REF} (-)	V _{DD} +0.5 to GND -0.5 V	Lead Temperature (Soldering 10 seconds)	+300°C
V _{IN}	V _{DD} +0.5 to GND -0.5 V	Package Power Dissipation Rating @ 75°C	
All Inputs	V _{DD} +0.5 to GND -0.5 V	PDIP, SOIC	1050mW
All Outputs	V _{DD} +0.5 to GND -0.5 V	Derates above 75°C	14mW/°C

NOTES:

- ¹ Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- ² Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
- ³ V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

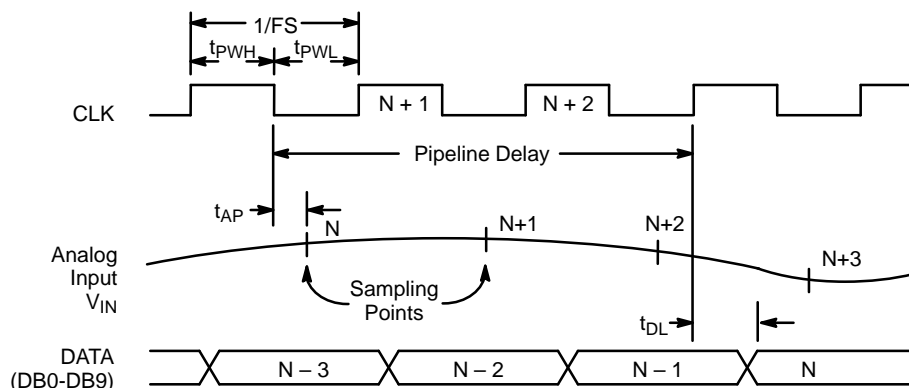


Figure 1. Timing Diagram

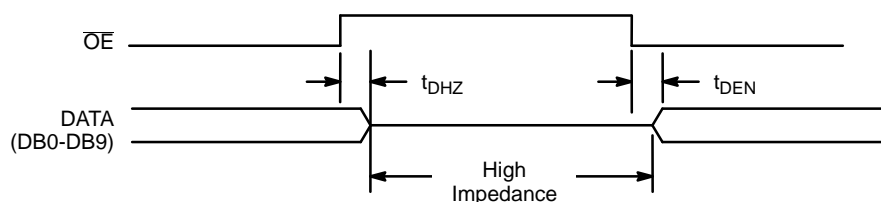


Figure 2. 3-State Timing Diagram

OVERVIEW OF THE MP87L91 PINS & OPERATION NOTES

\overline{OE} : Output Enable (Input)

This signal controls the 3-state drivers on the digital outputs DB0 - DB11. During normal operation \overline{OE} should be held low so that all outputs are enabled (NOTE: an internal resistor will pull \overline{OE} to this level if it is not connected). When \overline{OE} is driven high DB0 - DB11 goes into high impedance mode. This control operates asynchronously to the clock and only controls the output drivers. The internal output register will get updated if the clock is running while the outputs are in 3-state mode. If possible, \overline{OE} should be in 3-state during Clock = 1 to reduce digital noise coupling into A_{IN} during the sample time. Aperature provides a convenient control for this purpose since it guarantees that the A_{IN} sample period is complete when the outputs are enabled.

APERTURE: Aperture Delay Sync (Output)

This signal is high when the internal sample/hold function is sampling V_{IN} , and goes low when it is in the hold mode (when the ADC is comparing the stored input value to the reference ladder). The value of V_{IN} at the high to low transition of APERTURE is the value that will be digitized. A system can monitor this signal and adjust the CLK to accurately synchronize the sampling point to an external event. The Aperature pin may also be used

to control the \overline{OE} (outputs between 3-state and active mode). This will reduce the errors introduced by digital output coupling during the A_{IN} sample time.

MINV: Digital Output Format (Input)

This signal controls the format of the digital output data bits DB0 - DB11. Normally it is held low so the data is in straight binary format (all 0's when $V_{IN} = V_{RB}$; all 1's when $V_{IN} = V_{RT}$). If MINV is pulled high then the MSB (DB11) will be inverted.

MINV is meant to be a static digital signal. If it is to change during operation it should only change when the CLK is low. Changing MINV on the wrong phase of the CLK will not hurt anything, but the effects on the digital outputs will not be seen until the output latch of the output register is enabled. MINV has an internal pull down device. This function is not available in the engineering sidebrase samples. For these samples, this pin must be tied to GND.

V_{IN} : Analog Input

This part has a switched capacitor type input circuit. This means that the input impedance changes with the phase of the input clock.

R1, R2, R3: Reference Ladder Taps

These taps connect to every 1/4 point along the reference ladder; R1 is 1/4th up from V_{RB} , R3 is 3/4ths up from V_{RB} (or 1/4th down from V_{RT}). Normally these pins should have 0.1 microfarad capacitors to V_{SS} , this helps reduce the INL errors by stabilizing the reference ladder voltages.

These taps can also be used to alter the transfer curve of the ADC. A 4 segment, piecewise linear, custom transfer curve can be designed by connecting voltage sources to these pins.

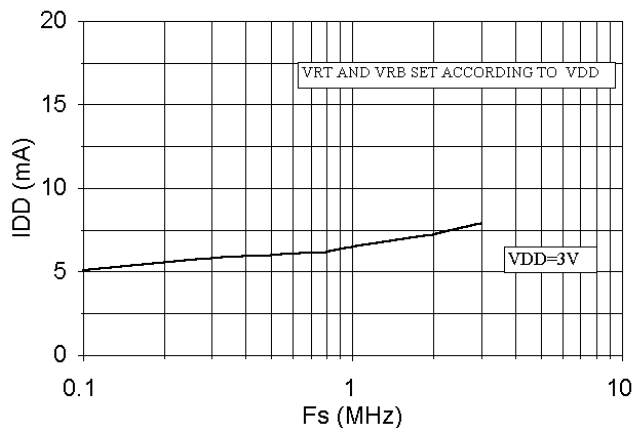
This may be desirable to make the probability of codes for a certain range of V_{IN} be enhanced or minimized.

Sometimes this is referred to as probability density function shaping, or histogram shaping.

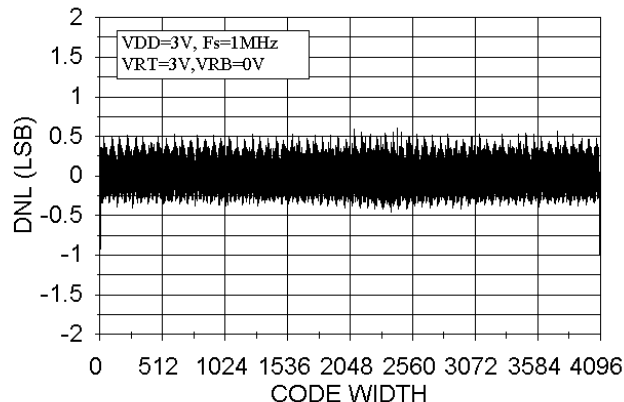
The internal interconnect resistance from each of the t_{AP} pins to the ladder is less than 3Ω .

1.6V maximum per tap is recommended for applications above 85°C . For operation less than 85°C up to 3.2 V per tap can be utilized.

PERFORMANCE CHARACTERISTICS

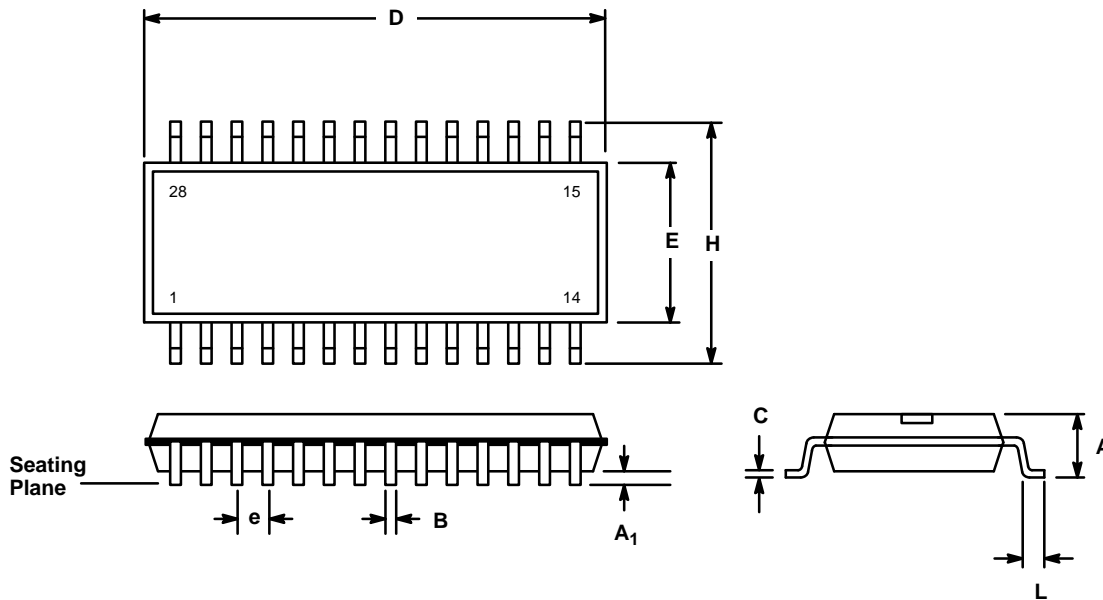


Graph 1. I_{DD} vs. FS



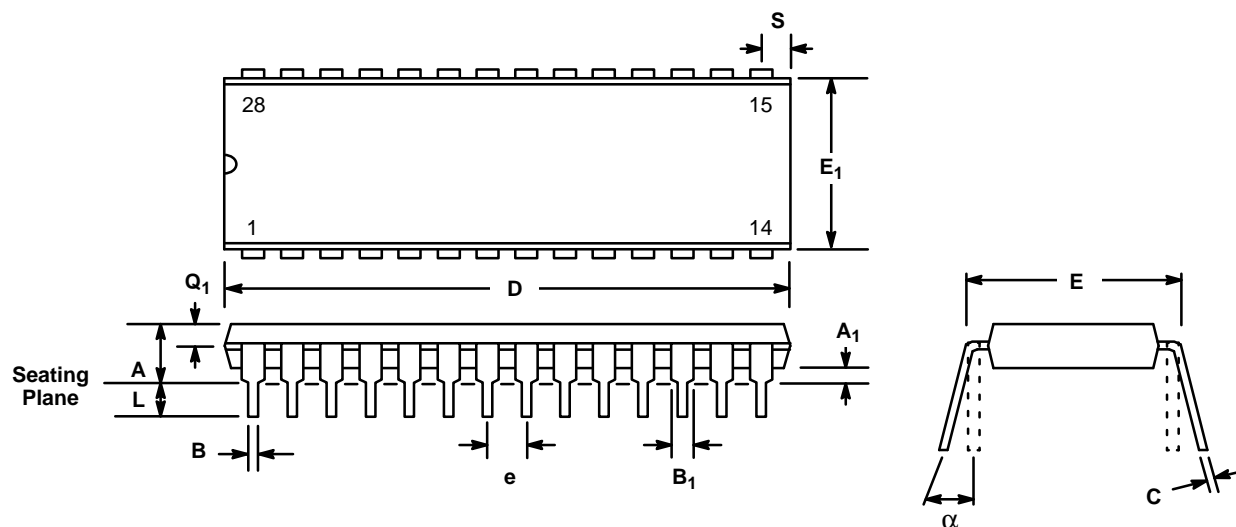
Graph 2. DNL Error Plot

**28 LEAD SMALL OUTLINE
(335 MIL EIAJ SOIC)
R28**



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.60	2.80	0.102	0.110
A ₁	0.2 (typ.)		0.008 (typ.)	
B	0.3	0.5	0.012	0.020
C	0.10	0.20	0.004	0.008
D	17.6	18.0	0.693	0.709
E	8.3	8.5	0.327	0.335
e	1.27 (typ.)		0.050 (typ.)	
H	11.5	12.1	0.453	0.477
L	0.8	1.2	0.031	0.047

28 LEAD PLASTIC DUAL-IN-LINE (600 MIL PDIP) N28



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.232	—	5.893
A ₁	0.015	—	0.381	—
B	0.014	0.023	0.356	0.584
B ₁ (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.380	1.490	35.05	37.85
E	0.585	0.625	14.86	15.88
E ₁	0.500	0.610	12.70	15.49
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q ₁	0.055	0.070	1.40	1.78
S	0.020	0.100	1.508	2.54

Note: (1) The minimum limit for dimensions B₁ may be 0.023" (0.58 mm) for all four corner leads only.

Notes

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