MP87L75

Low Voltage CMOS
8-Bit High Speed
Analog-to-Digital Converter

FEATURES

- **3.3 Volt Operation**
- **8-Bit Resolution**
- **Small 20 Pin SOIC, PDIP & SSOP Packages**
- **DNL = ±1/2 LSB, INL = ±1 LSB (typ)**
- **Internal S/H Function**
- **V_{IN} DC Range: 0 V to V_{DD}**
- **V_{REF} DC Range: 1 V to V_{DD}**
- **Low Power: 20 mW typ. (excluding reference)**
- **Latch-Up Free**

APPLICATIONS

- **Digital Radio**
- **Cellular Telephones**
- **CCD's and Scanners**
- **Hand Held and Battery Powered Data Acquisition**

GENERAL DESCRIPTION

The MP87L75 is an 8-bit Analog-to-Digital Converter in a small 20 pin SOIC package that operates at 3.3 V. Designed using an advanced CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

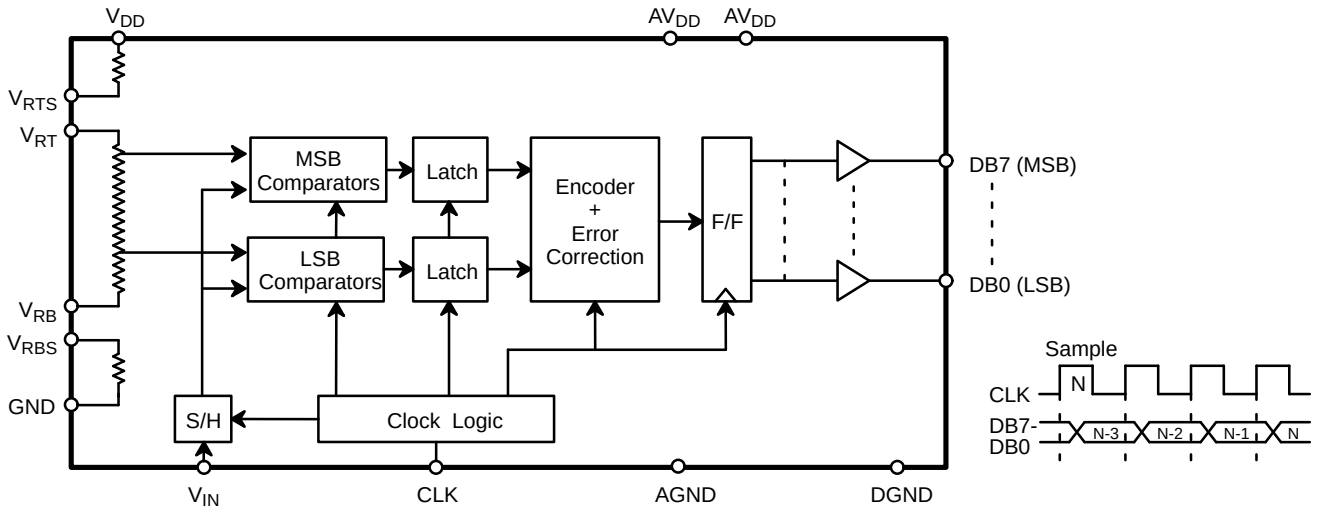
This device uses a two-step flash architecture to maintain low power consumption at high conversion rates. The input circuitry of the MP87L75 includes an on-chip S/H function and allows the user to digitize analog input signals between GND and V_{DD}. Careful design and chip layout have achieved a low analog input capacitance. This reduces "kickback" and eases the requirements of the buffer/amplifier used to drive the MP87L75.

The designer can choose the internally generated reference voltages by connecting V_{RB} to V_{RBS} and V_{RT} to V_{RTS}, or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 0.4 V at V_{RB} and 1.72 V at V_{RT}. Providing external reference voltages allows easy interface to any input signal range between GND and V_{DD}. This also allows the system to adjust these voltages to cancel zero scale and full scale errors, or to change the input range as needed.

The device operates from a single +3.3 V supply ±10%. Power consumption is 20 mW at FS = 10 MHz.

Specified for operation over the commercial / industrial (–40 to +85°C) temperature range, the MP87L75 is available in Plastic dual-in-line (PDIP), Surface Mount (SOIC), and Shrunk small outline (SSOP) packages.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

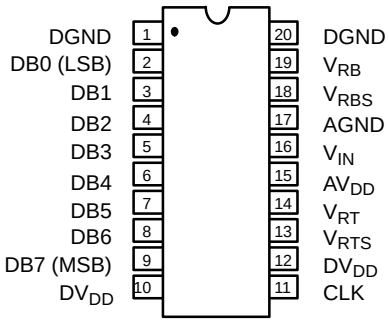


ORDERING INFORMATION

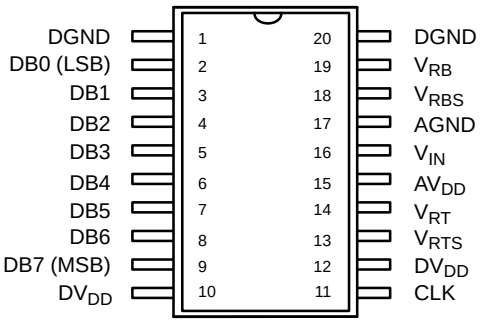
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
SOIC	–40 to +85°C	MP87L75AS	±1/2	1 1/2
SSOP	–40 to +85°C	MP87L75AQ	±1/2	1 1/2
PDIP	–40 to +85°C	MP87L75AN	±1/2	1 1/2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



20 Pin PDIP (0.300")
N20



20 Pin SOIC (Jedec, 0.300") – S20
20 Pin SSOP – A20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DGND	Digital Ground
2	DB0	Data Output Bit 0 (LSB)
3	DB1	Data Output Bit 1
4	DB2	Data Output Bit 2
5	DB3	Data Output Bit 3
6	DB4	Data Output Bit 4
7	DB5	Data Output Bit 5
8	DB6	Data Output Bit 6
9	DB7	Data Output Bit 7 (MSB)
10	DV_{DD}	Digital Power Supply

PIN NO.	NAME	DESCRIPTION
11	CLK	Sample Clock
12	DV_{DD}	Digital Power Supply
13	V_{RTS}	Internal Top Ladder Bias
14	V_{RT}	Top Reference
15	AV_{DD}	Analog Power Supply
16	V_{IN}	Analog Input
17	AGND	Analog Ground
18	V_{RBS}	Internal Bottom Ladder Bias
19	V_{RB}	Bottom Reference
20	DGND	Digital Ground

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 3.3 V, FS = 6 MHz (50% Duty Cycle), V_{RT} = 2.5 V, V_{RB} = 0.5 V, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		8			Bits	
Sampling Rate	FS			10	MHz	
ACCURACY (A Grade)[1]						
Differential Non-Linearity	DNL			±1/2	LSB	
Integral Non-Linearity	INL			1 1/2	LSB	Best Fit Line (Min INL – Max INL)/2
REFERENCE VOLTAGES						
Differential Ref. Voltage[3]	V_{REF}	1.0		AV_{DD}	V	$V_{REF} = V_{RT} – V_{RB}$
Ladder Resistance	R_L		350		Ω	
Ladder Temp. Coefficient	R_{TCO}		2000		ppm/°C	
Self Bias 1						
Short V_{RB} and V_{RBS}	V_{RB}		0.4		V	
Short V_{RT} and V_{RTS}	V_{RT}-V_{RB}		1.32		V	
Self Bias 2						
V_{RB} = AGND, Short V_{RT} and V_{RTS}	V_{RT}		1.52		V	
ANALOG INPUT						
Input Bandwidth (–1 dB)[4]	BW		5		MHz	
Input Voltage Range	V_{IN}	V_{RB}		V_{RT}	V	
Input Capacitance[5]	C_{IN}		16		pF	
Aperture Delay	t_{AP}		30		ns	
DIGITAL INPUTS						
Logical “1” Voltage	V_{IH}	2.5			V	
Logical “0” Voltage	V_{IL}			0.5	V	
DC Leakage Currents[6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK			5		µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1.*)[7]						
Clock Period	1/FS		100		ns	
High Pulse Width	t_{PWH}		50		ns	
Low Pulse Width	t_{PWL}		50		ns	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical “1” Voltage	V_{OH}	2.5			V	I_{LOAD} = 1 mA
Logical “0” Voltage	V_{OL}			0.5	V	I_{LOAD} = 1 mA
Data Valid Delay	t_{DL}		30		ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Description	Symbol	25°C Min	25°C Typ	25°C Max	Units	Conditions
POWER SUPPLIES						
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	3	3.3	3.6	V	
Current	I_{DD}		6	12	mA	Does not include ref. current

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (*Figure 2.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 3.*). Accuracy is a function of the sampling rate (FS).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 –1 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.

5 See V_{IN} input equivalent circuit (*Figure 4.*). Switched capacitor analog input requires driver with low output resistance.

6 All inputs have diodes to V_{DD} and GND. Input DC currents will not exceed specified limits for any input voltage between GND and V_{DD}.

7 t_R, t_F should be limited to >5 ns for best results.

8 AGND & DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 5.5 V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating @ 75°C
SOIC, SSOP, PDIP ..... 700 mW
Derates above 75°C ..... 9mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

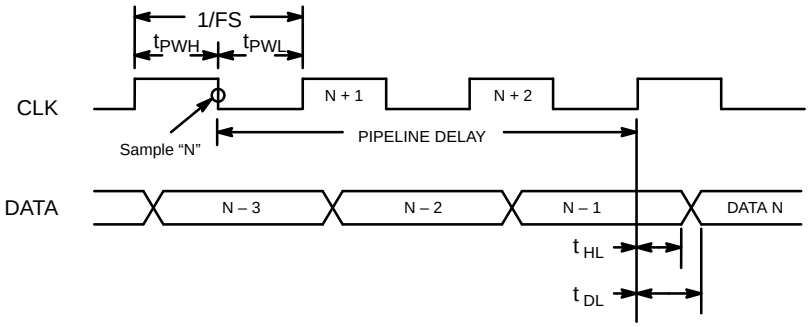
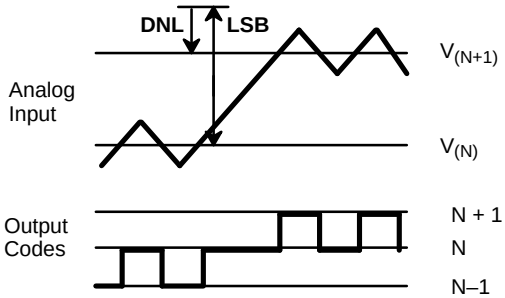


Figure 1. MP87L75 Timing Diagram



Code Width (N) = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{RT} - V_{RB}$] / 256

$DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - LSB$

Figure 2. DNL Measurement

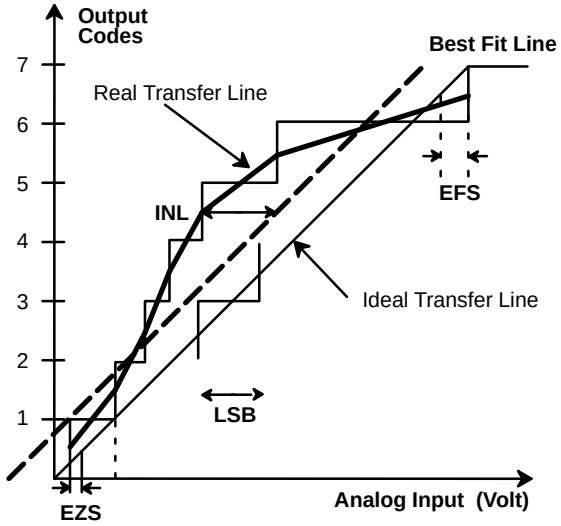


Figure 3. INL Error Calculation

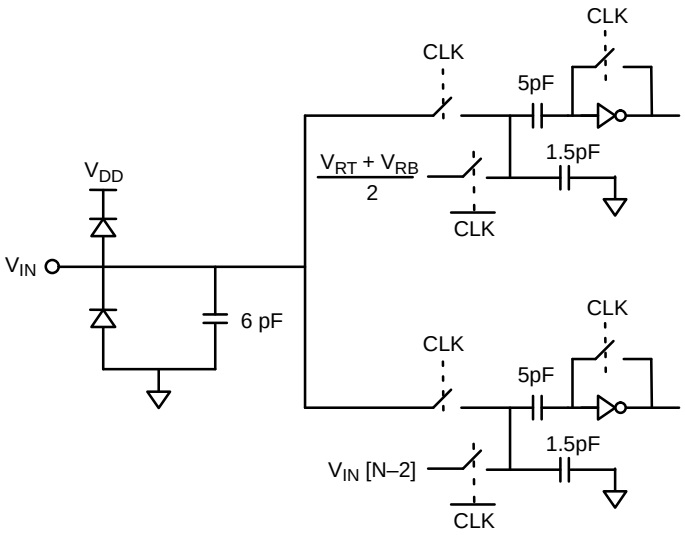


Figure 4. Equivalent Input Circuit

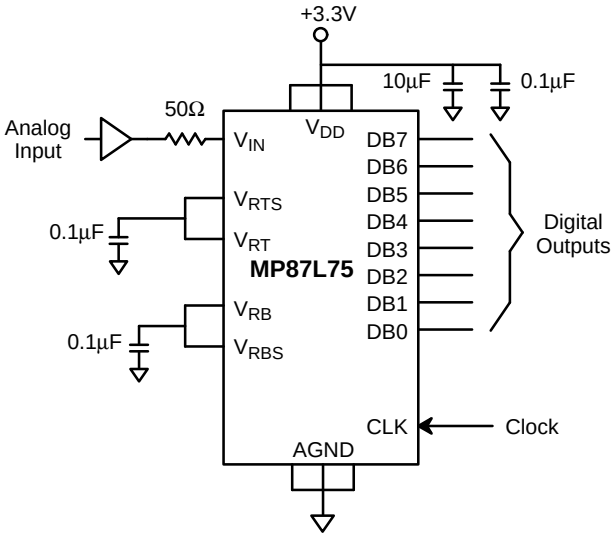


Figure 5. Typical Circuit Connections

APPLICATION NOTES

Signals should not exceed AV_{DD} or DV_{DD} +0.5V or go below AV_{DD} or DV_{DD} –0.5V. All pins have internal protection diodes that will protect them from short transients (<100µs) outside the supply range.

AGND and DGND pins are connected internally through the P–substrate. DC voltage differences between these pins will cause undesirable internal substrate currents.

The power supply (AV_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to AGND, placed as close to the chip as possible.

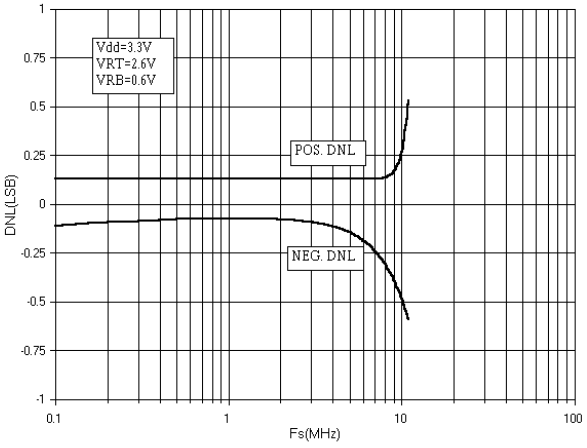
The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

It is possible for the data valid delay (t_{DL}) to be equal to or greater than the high pulse width of the sampling clock (t_{PWH}), See *Figure 1.* This can cause timing related errors. For sample rates above 8 MSPS use only the rising edge of the sample clock (CLK) to latch data from the MP87L75 to other parts of the system.

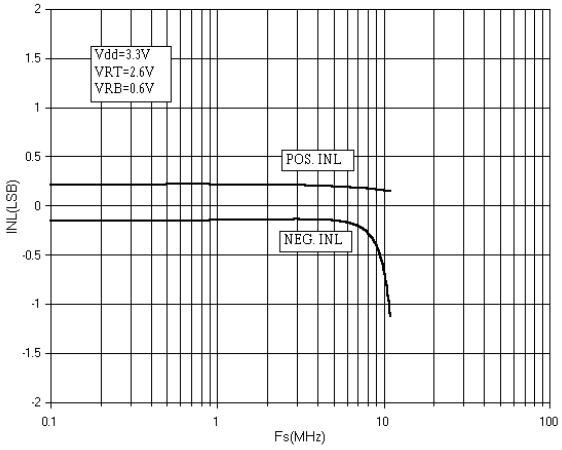
The reference can be biased internally by shorting V_{RT} to V_{RTS} and V_{RB} to V_{RBS}. This will generate 0.36 V at V_{RB} and 1.56 V at V_{RT} (see *Figure 5.).*

If the internal reference pins V_{RTS} and/or V_{RBS} are not used they should be left unconnected.

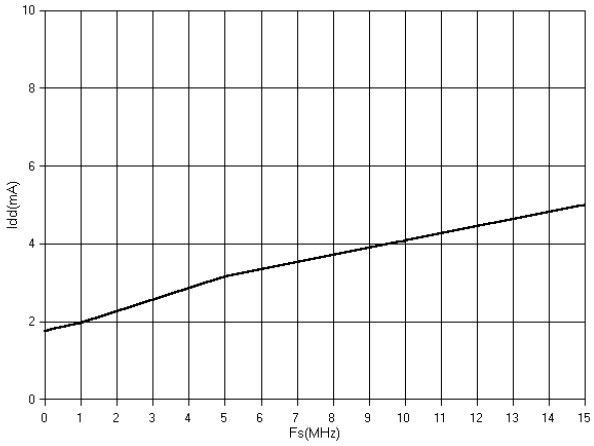
PERFORMANCE CHARACTERISTICS



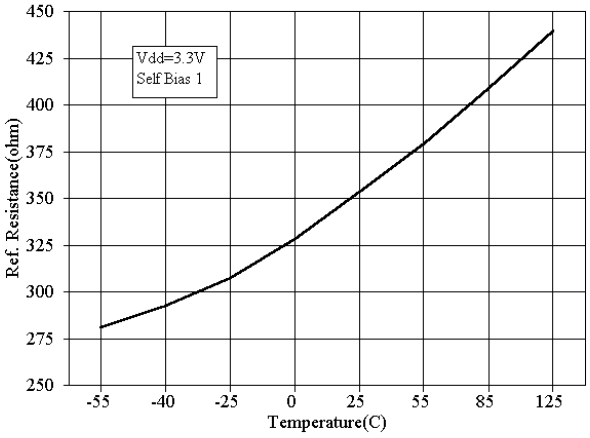
Graph 1. DNL vs. Sampling Frequency



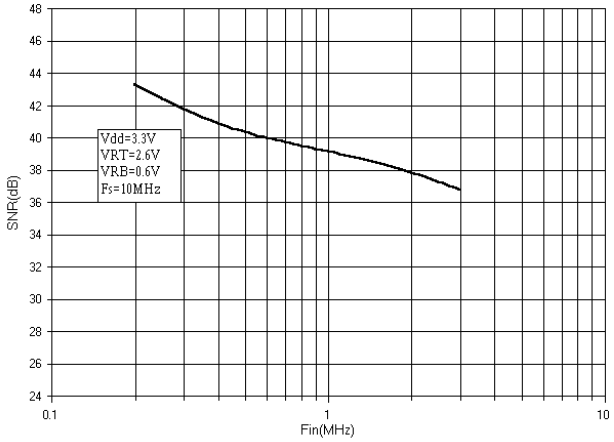
Graph 2. INL vs. Sampling Frequency



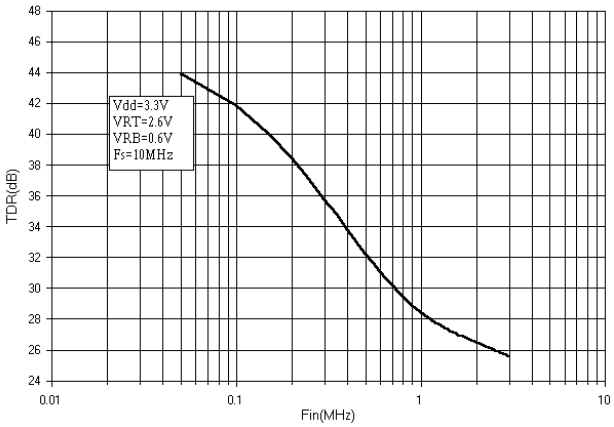
Graph 3. Supply Current vs. Sampling Frequency



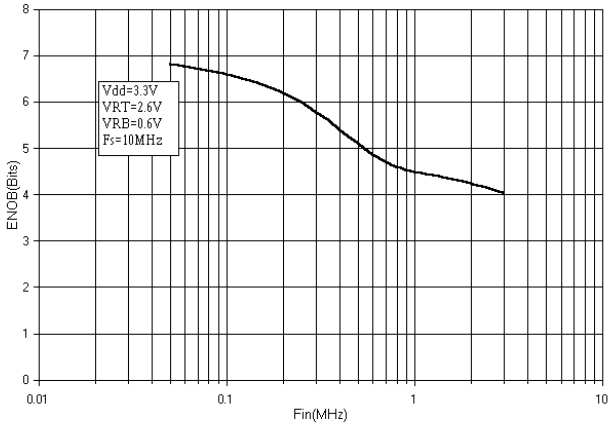
Graph 4. Reference Resistance vs. Temperature



Graph 5. SNR vs. Input Frequency

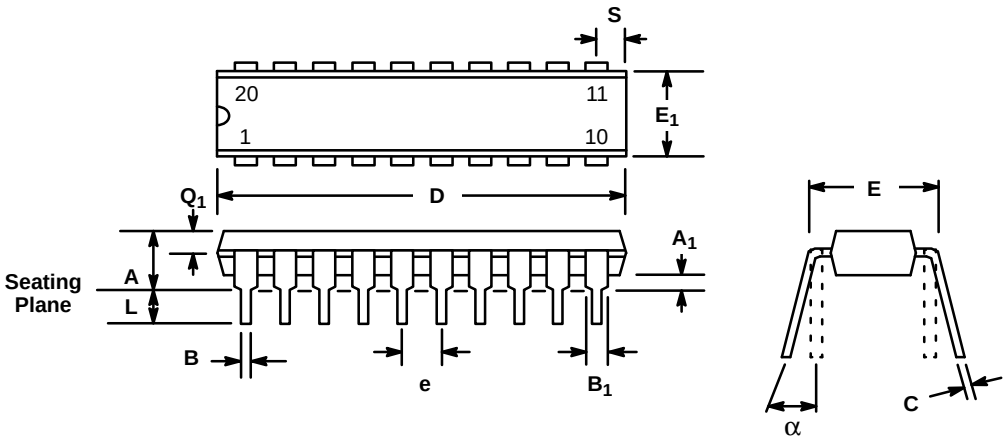


Graph 6. SINAD vs. Input Frequency



Graph 7. ENOB vs. Input Frequency

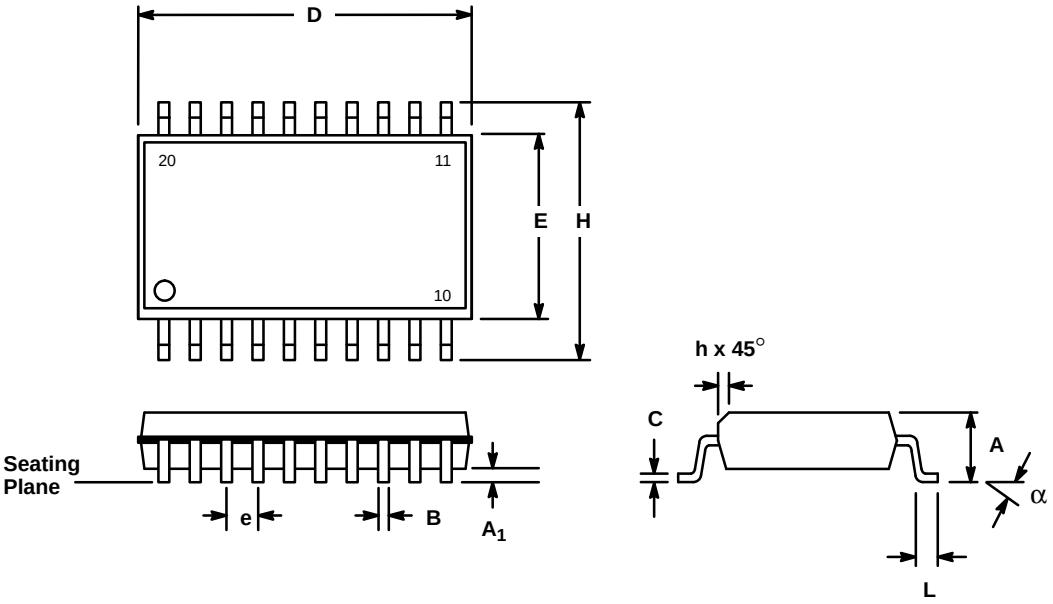
20 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.945	1.060	24.0	26.92
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.080	1.02	2.03

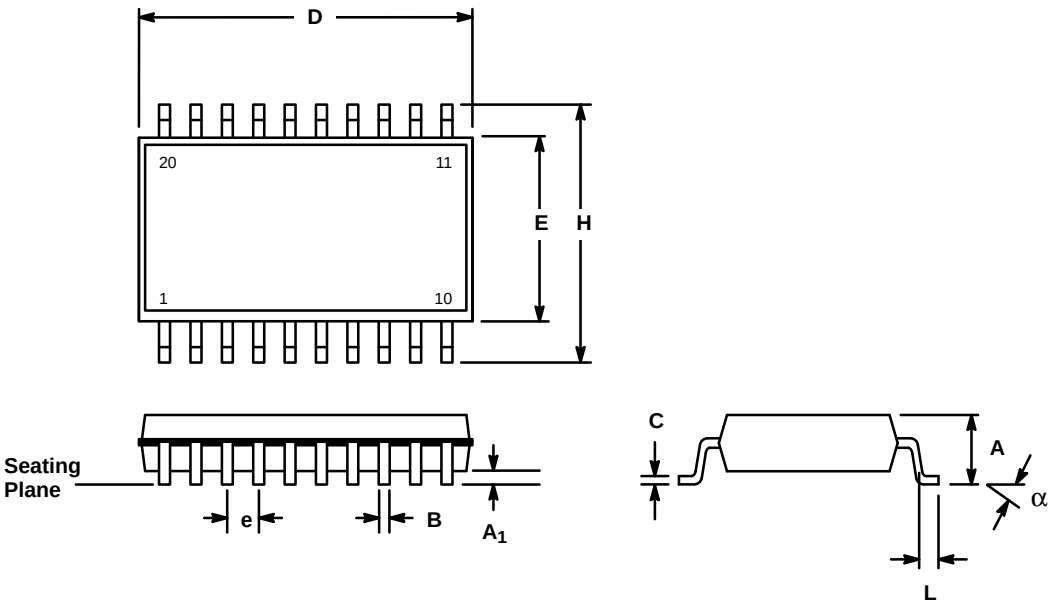
Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

20 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.642
A_1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.500	0.510	12.70	12.95
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

20 LEAD SHRINK SMALL OUTLINE PACKAGE (SSOP)
A20



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.73	2.05	0.068	0.081
A_1	0.05	0.21	0.002	0.008
B	0.20	0.40	0.008	0.016
C	0.13	0.25	0.005	0.010
D	7.07	7.40	0.278	0.291
E	5.20	5.38	0.205	0.212
e	0.65 BSC		0.0256 BSC	
H	7.65	8.1	0.301	0.319
L	0.45	0.95	0.018	0.037
α	0°	8°	0°	8°

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Datasheet April 1995