MP8791AB APPLICATION BOARD DOCUMENTATION

Evaluation Kit Parts List

This kit contains the following:

- One MP8791AB Applications Board with sample MP8791
- MP8791AB Documentation
- Circuit Diagram
- Layout Diagrams

Its uses provide the following features:

- Easy Evaluation of MP8791
- Optimized Printed Circuit Board Design
- Optimized Support Circuits
- User Friendly Interface
- Layout Applicable to Final Design

Introduction

The MP8791AB is a complete printed circuit test board designed to permit quick and accurate evaluation of EXAR's MP8791, 12-bit 2 MSPS analog-to-digital converter. This applications board combines a proven PC Board layout with optimized analog and digital interface circuitry to satisfy the stringent requirements needed in evaluating high performance devices of this type.

The board contains the device being tested (MP8791), operational amplifiers for input buffers, control logic and latches, and numerous connectors and jumper options.

With external laboratory equipment, complete DC and AC performance of the part can be evaluated.

Flexible user interface is provided by selectable jumper options and convenient connectors. Observation test points are available at commonly used locations.

A Preview of a Common Test Configuration

The board is set up as a general A/D test circuit where the references are fixed. *Figure 2.* shows the overall circuit, *Figure 5.* shows the PC board layout and jumper locations, also listed in Table 1. There are many other circuit possibilities built into the universal test board; however, starting with the default circuit is recommended.

Options for analyzing the output results are discussed in detail below. The most effective of these is the use of a high speed data acquisition system and FFT software to compute the performance parameters.

System Configuration

Two complete evaluation circuit block diagrams showing the MP8791AB with typical external test equipment is shown in *Figure 2. and Figure 3.* The following is a more detailed description of the major on-board and external components used in these systems as seen in *Figure 2., Figure 3., and Figure 6.*

Application Board Circuitry

The application board support circuitry is shown in *Figure 6.* The major components supporting the A/D under test are:

1. V_{REF} BUFFER – A dual op amp (EL2224C) can be used to isolate the externally supplied $V_{REF(+)}$ and $V_{REF(–)}$ from the device under test and provides a low source impedance. These buffers can be bypassed with onboard jumpers (J6 and J13). If voltage feedback op amps are used, holes for optional compensation caps are provided.
2. ANALOG INPUT AMPLIFIER – An operational amplifier (AD847) is used in an instrumentation amp configuration (gain –5) to provide a low source impedance to the A/D. Provisions are made for summing a dither signal and/or offset voltage with the input. Holes for optional compensation caps are provided on-board.
3. DATA LATCHES – The digital output of the A/D drive on-board latches which buffer the device under test from the external test equipment.
4. CONTROL LOGIC – Allows control of the data latch clocks as well as the $\overline{OE}$ pin of the DUT.

External Equipment Required

The system block diagrams (*Figure 2. and Figure 3.)* shows the external test equipment required to perform all test and evaluation functions. These include:

1. POWER SUPPLIES – ±15 volt and one (or two) +5 volt external power supplies are needed. Decoupling circuits are provided on the applications board, however, low noise, low output impedance supplies are necessary for best performance. A connector (CON3) is used for all power and ground connections. This connector is the 10 pin connector located next to the $V_{REF(-)}$ input. For best results, twist the power supply cable pairs. This minimizes coupling to and from these to unrelated sections of the setup.
2. CLOCK GENERATOR – A 1 KHz to 2 MHz symmetrical clock signal must be applied to the SMB coax connector labeled CLOCK. Note the 50Ω input impedance.
3. REFERENCE SUPPLIES – A positive and negative reference voltage is connected through the SMB coax connectors labeled $V_{REF(+)}$ and $V_{REF(-)}$ (typically +5 and 0 volts respectively). The external reference voltages can be configured to go through op amp buffers or go directly to the A/D by using jumpers J6 and J13. Note that $V_{REF(+)}$ must be more positive than $V_{REF(-)}$, since V_{RT} must be $>V_{RB}$ on chip.
4. INPUT SIGNAL GENERATOR – A clean, low distortion sine wave generator is used as a signal source. A band pass filter is sometimes required to further reduce harmonics and bandlimit noise as shown. The SMB coax connector labeled A_{IN} accepts the analog input. An on board op amp (AD847) is used to amplify this input (gain of –5) and provide low source impedance to drive the A/D under test. The socket has a standard 741 type pinout which allows experimentation with alternative amplifiers.
5. DITHER INPUT – The cross plot test configuration (later described) requires a triangle wave signal source. This signal is added to a DC input signal through the SMB connector labeled DITHER (an inverting input with gain of 1/50). J7 connects this point to ground via a 50Ω resistor.
6. A_{IN} COMMON – An alternate, non inverting input (gain of five). Connect to ground when not used. J11 connects A_{IN} COMMON to ground via a 50 Ω resistor. This input allows use of differential inputs or used for applying a DC offset for level shifting the A_{IN}.
7. OSCILLOSCOPE – The output of a dither DAC, TP3, is used to drive the vertical input of the oscilloscope for manual linearity testing using the “cross plot” method described on the following page.
8. DSP – Evaluation of dynamic and static performance is done by external processing devices that perform histogram and harmonic analysis to determine characteristics like linearity, noise, distortion, intermodulation effects, etc. The data is available at the CON1 connector, which is the inside column of jumper connectors labelled D0 through D11.

Optional Equipment

1. Precision External Output DAC – As an alternative to DSP, a high speed precision digital to analog converter can reconstruct the output in analog form. The analog measurements can be used to evaluate the A/D’s performance using conventional analog instrumentation. Use the DACEN output at CON1 to load the reconstruction DAC.
2. Reference Control DACS – The reference voltage at the top (V_{RT}) and bottom (V_{RB}) of the A/D can be changed by external DACs on alternate CLOCK cycles to change offset and scale factor. Data can be loaded into the DACs by using the logic signal DACEN on the output connector. The two DACs must have resolution and settling time characteristics consistent with the application. Note that C14, C13, C21, and C22 are decoupling capacitors at the reference pins. These have to be removed when V_{RT} and V_{RB} are driven dynamically.

SYSTEM OPERATION

Reference Inputs

With the reference op amps in circuit, the ADC's reference pins (V_{RB} and V_{RT}) are driven in an offset and range mode:

$V_{RB} = V_{REF(-)}$, $V_{RT} = V_{REF(-)} + V_{REF(+)}$

Hence $V_{REF(-)}$ defines the offset and $V_{REF(+)}$ defines the span.

Analog Inputs

A_{IN} and A_{IN} COMMON Input Only

Differential input can be achieved by using A_{IN} and (A_{IN} COMMON). If the DITHER input is left floating, then the differential input to the ADC is given by:

ADCIN – $V_{REF(-)}$ = 5 (A_{IN} COMMON) – 5 A_{IN}

under the assumption of ideal components. This allows reduction of common mode signals between A_{IN} and (A_{IN} COMMON).

DITHER and A_{IN} COMMON Input Only

With A_{IN} floating and a signal applied to DITHER:

ADCIN = 0.875 • A_{IN} COMMON – 0.05 • DITHER + 0.175 • $V_{REF(-)}$,
where ADCIN = A_{IN} (MP8791 pin 3).

Outputs

The parallel digital output of the A/D can be accessed on connector "CON1". A system clock (PTSCLK) and an external DAC enable (DACEN) are also available on that connector. This output data, in conjunction with various input stimuli, is used to evaluate the A/D and timing performance. The three common methods are described below.

Digital Signal Processing

A comprehensive dynamic performance evaluation is most often done by using external hardware capable of fast data acquisition and storage. The computation of integral linearity, differential linearity, signal to noise and distortion ratios, the effective number of bits, and other useful figures of merit is done using software having histogram and FFT capability. The accuracy of the test results depends upon the quality of the input sine wave. A low distortion sine wave generator with a band pass filter will be necessary.

Commercial software packages with the needed computational features are available. The Tektronix PTS101 is used by EXAR to acquire and analyze the ADC data.

Analog Testing with External DAC

The logic output of the system can be converted back to analog by using a high performance digital to analog converter. Laboratory spectrum analyzers and oscilloscopes can be used to measure linearity, frequency response, harmonic distortion, noise, intermodulation distortion, etc. These measurements can be converted to the specifications commonly used in specifying A/D's dynamically. In addition to a high quality sine wave input, the output D/A converter must be significantly more accurate than the A/D under test. The filtering effects of adding a zero order "hold" in the signal path are described in EXAR Application Note MPSAN27 which can be found in the 1993 data book.

Cross Plot

An evaluation of differential linearity can be simply done with an oscilloscope, a triangle wave generator and a low noise DC signal source. Input jacks are provided on the board so this "cross plot" method can be conveniently implemented (See *Figure 3.*). The oscilloscope must be set in the X-Y display mode.

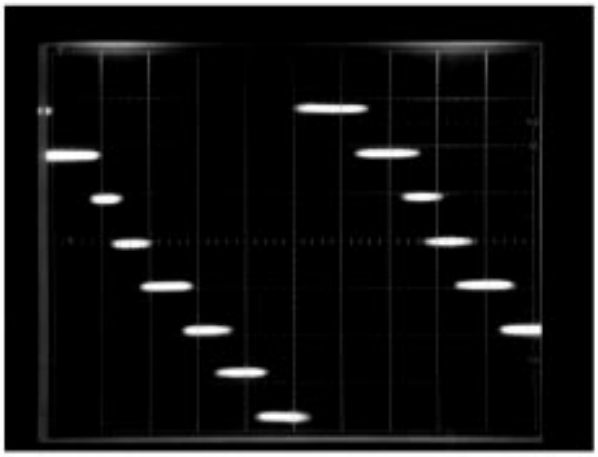


Figure 1. Cross Plot

A triangle wave (100 Hz) with a peak-to-peak amplitude of approximately 160 LSBs peak is supplied to the "DITHER" input. This is attenuated to 8 LSB's by the input amplifier. The triangle wave is also used to drive the x axis of the scope. The horizontal gain is set so that ±4 divisions are swept. Look at Test Point 3 (TP3) with the vertical input. Set the horizontal gain for 1 LSB per division.

A stair step waveform will result (See *Figure 1.*) By changing the DC input, eight code transitions can be observed about any DC input level. The horizontal distance between these transitions is the code width. Missing codes cause steps to be absent. By setting the endpoint thresholds to coincide with the scope grid lines, integral linearity errors are displayed as thresholds which are off-centered from these grid lines. A precision DC voltage source is necessary for the integral linearity measurement.

Since the conversion speed is much faster than the dither frequency, multiple readings are taken at each threshold. The horizontal variation of each threshold gives a qualitative measure of noise (in LSB's).

Using this "cross plot" method is a good way to prove out the lab setup prior to more sophisticated DSP test.

Jumper Options

The MP8791AB offers flexibility through configuration determining jumpers. These optional jumpers furnish choices for (1) input termination resistors, (2) bypassing of the reference input buffers, and (3) the selection of several logic and clock options. *Table I.*, *Figure 4., and Figure 5.* show the jumper functions along with the default configuration set-up prior to shipment.

Termination Options

Termination resistors (50 Ω) can be added to the five analog input coax SMB connectors as indicated in *Table I.* (J11, J4, J7, J9, and J12). Note that the CLOCK input is not optional. A permanent 50 Ω termination is connected from its input to digital ground (DGND). The default configuration for the other five coax inputs is — no termination resistors are connected.

Bypass Options

The reference input buffers can be bypassed with J6 and J13 or the V_{RB} pin of the A/D grounded if J8 is inserted. Remove U4, the dual op amp (EL2224C) when using these unbuffered modes. The default mode is — buffers are out.

Logic Options

The logic options are selected using the five jumpers as listed in *Table I.* and shown in detail in *Figure 6.* Note that three of these jumpers have multiple combinations. Note also that the clock connected to the A/D being tested is always the same as the external clock after a two inverter delay. A simplified logic diagram is given in *Figure 4.* The logic control jumpers are primarily set for two basic test configurations. The standard evaluation mode is shown in *Figure 4.*

Final Design Considerations

After the MP8791AB has been used to demonstrate that the MP8791, the clock timing, and the analog support circuits are acceptable, the design must be successfully transferred to the user's system. A close copy of the proven layout is recommended as is the use of identical support devices. Where this is not possible, the following advice should be heeded:

1. Be generous with analog and digital ground planes. Repeat as closely as possible the ground plane system on the application board.
2. Keep high frequency decoupling capacitors very close to the A/D pins and minimize the loop area included so less flux will induce less noise. Use decoupling capacitors in the same locations as on the MP8791AB.
3. Coupling between logic signals and analog circuitry can easily change a 12-bit system into an 8-bit system or worse. Completely separate them. Watch for coupling opportunities from other sources not immediately associated with the A/D. Don't use switching power supplies in adjacent locations for example.
4. Tri-state the output latches and the A/D enable during the A_{IN} sample time.
5. Use support devices equivalent to those used on the evaluation board. Use the application board to verify these devices up front, i.e. use very linear passive components in the signal path.
6. Select a driving op amp whose noise, speed, and linearity fits the application.
7. For sampling of high frequency signals, a sample and hold amplifier like the AD783 is recommended.
8. Decoupling capacitors on pins R1, R2 and R3 do not improve the ADC's performance.

Additional Documentation

A set of drawings showing the details of the electrical circuit and board layout are given in *Figure 8. Figure 10. Figure 7. and Figure 9. Figure 6.* is the complete electrical circuit. *Figure 5.* shows the jumper locations.

Technical Hotline

For any application hints, please call our hotline at (408) 562-3615.

Table I. Jumper Options

Termination of Input Coax Cables		
Jumper	**Description**	**Default**
J11	Connecting adds 50 Ω from A_{IN} COM to AGND	
J4	Connecting adds 50 Ω from A_{IN} to AGND	✔
J7	Connecting adds 50 Ω from DITHER to AGND	
J9	Connecting adds 50 Ω from $V_{REF(+)}$ to AGND	
J12	Connecting adds 50 Ω from $V_{REF(–)}$ to AGND	
Reference Amplifer/Buffer Bypass		
J6	Connecting shorts coax $V_{REF(+)}$ Jack to V_{REF}T of ADC	✔
J13	Connecting shorts coax $V_{REF(–)}$ Jack to V_{REF}B of ADC	
J8	Connecting shorts V_{REF}B (on ADC) to AGND	✔
Logic and Clock Jumpers		
J2 (2, 3)	Connecting makes the latch clock the same or inverted as the ADC clock. Dependent on J12A.	
J2 (2, 1)	Connecting delays latch clock by 2 prop delays	✔
J3	Divides latch clock by 2 for dynamic V_{REF} control	
J5	Usually connected – except for dynamic V_{REF} control	✔
J12A (2, 1)	Latch clock is inverted ADC clock	
J12A (2, 3)	Latch clock is same as ADC clock	✔
J12A (2, 4)	Used for dynamic V_{REF} control	
J13A (2, 1)	Connects clock to $\overline{OE}$ through 4.7kΩ (delays $\overline{OE}$)	✔
J13A (2, 4)	Connects Latch CLK to $\overline{OE}$	
J13A (2, 3)	Connects Aperture to $\overline{OE}$	

Notes:
1. J*x* (a, b) means short pin a and pin b of jumper *x*.
2. The ADC clock is not affected by the jumper combinations and is the same as the external clock – except for 2 inverter delay.
3. Connect either J3 or J5 but not both simultaneously.
4. When using the amplifier bypass jumpers, remove the op amps from the sockets.

Table II. Test Points

TP1	CLK into MP8791
TP2	V_{REFT} via 100Ω resistor
TP3	Crossplot output
TP6	D0 output of MP8791 i.e. LSB
TP7	$\overline{OE}$ of MP8791
TP9	V_{REFB} via 100Ω resistor

Table III. List of Components

Qty	Value	Ref Designators
1	74HC02	U2
1	74HC04	U1
3	74HC174	U3,U5,U6
1	MP8791	U7
1	AD847	U8
1	EL22224C or equiv.	U4 (optional)
7	10µF	C13, C20, C21, C27, C4, C8, C9
13	0.1µF	C11, C14, C19, C2, C22, C23, C24, C25, C3, C5, C6, C7
6	1.5KΩ	R1, R10, R19, R2, R22, R8
1	20KΩ	R11
1	10KΩ	R12
1	5.1KΩ	R13
4	10Ω	R14, R18, R25, R3
1	150KΩ	R15
7	49.9Ω	R17, R20, R26, R29, R31, R4, R6
3	39Ω	R21, R28, R7
1	4.7KΩ	R24
2	1KΩ	R27, R9
2	100Ω	R30, R5
2	7.5KΩ	R16, R23
6	SMB CONNECTOR	A_{IN}, A_{IN} COM, CLOCK, DITHER, $V_{REF(+)}$, $V_{REF(-)}$
6	TESTPOINT	TP1, TP2, TP3, TP6, TP7, TP9
3	50 Ω Cables	BNC Male to SMB Jack. Can be purchased from Pasternack, Irvine, CA.
7	Jumpers	J4, J6, J5, J8, J2, J12A, J13A
2	8 Pin DIP Socket	SU4, SU8
28	IC Socket Pins	
1	10 Pin Header Connector	CON3
1	30 Pin Header Connector	CON1, CON2
1	PCB–Rev 1	MP8791AB PC Board

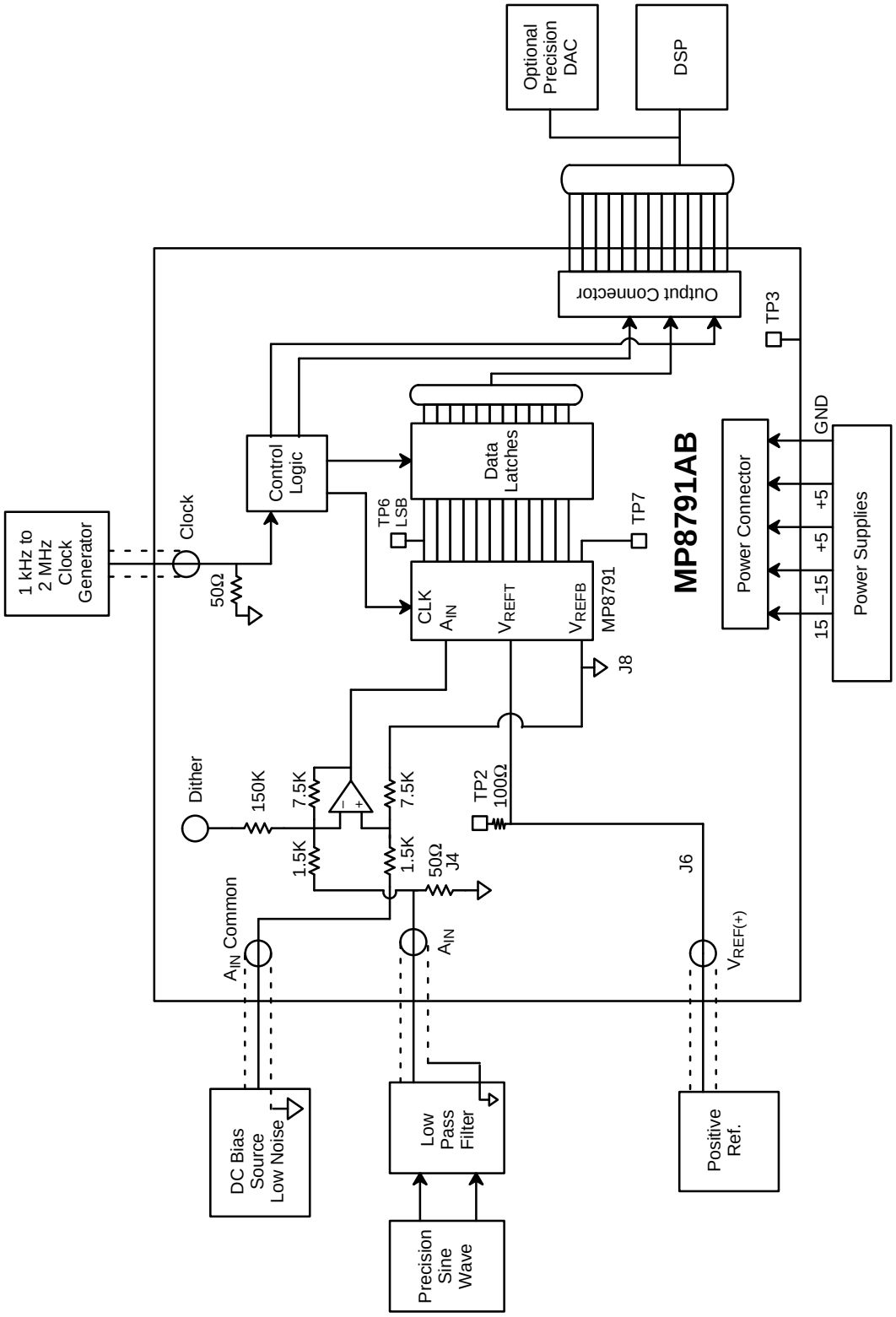


Figure 2. General A/D Test Circuit with Fixed Reference

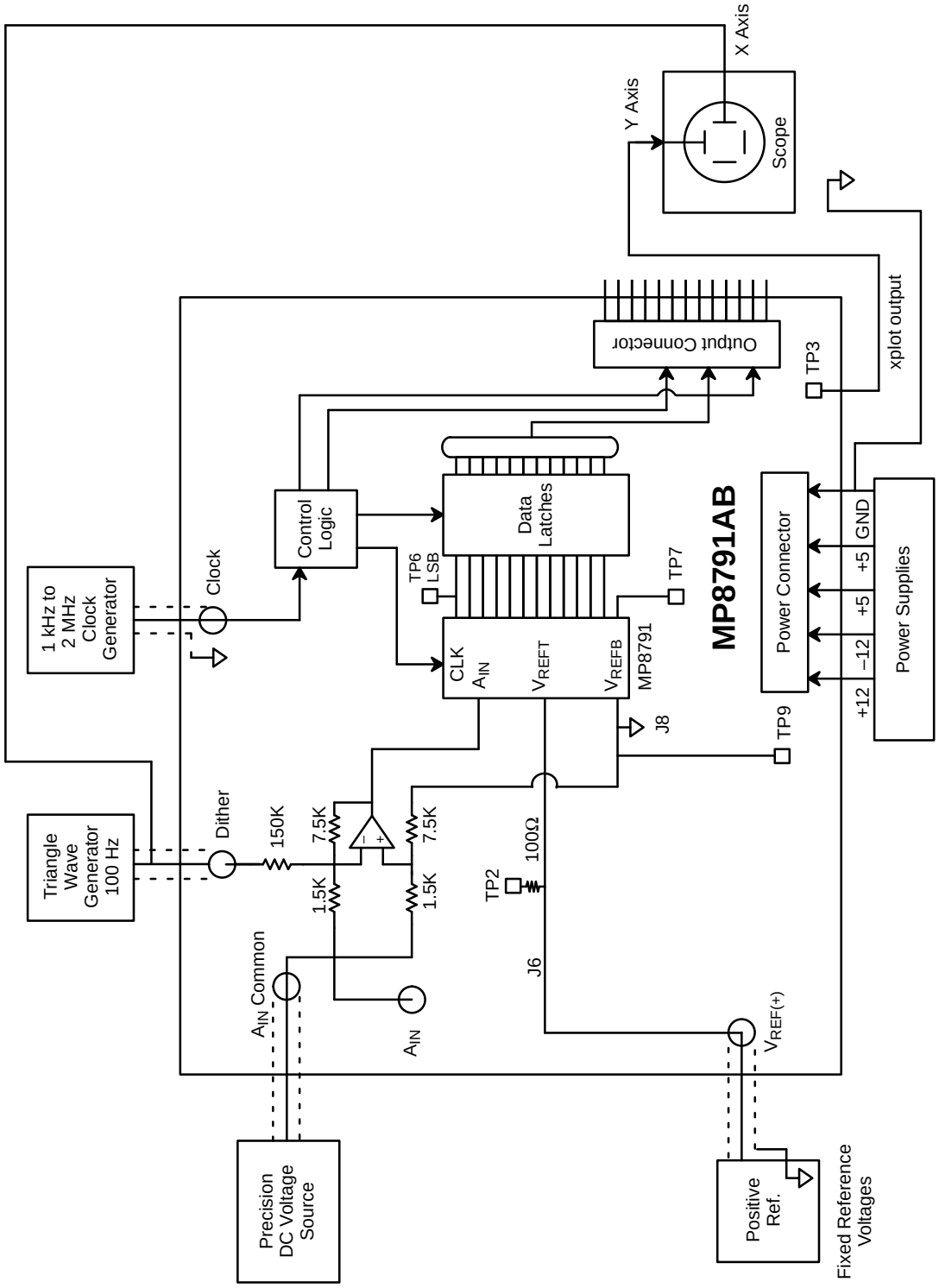


Figure 3. "Cross Plot" Set-Up

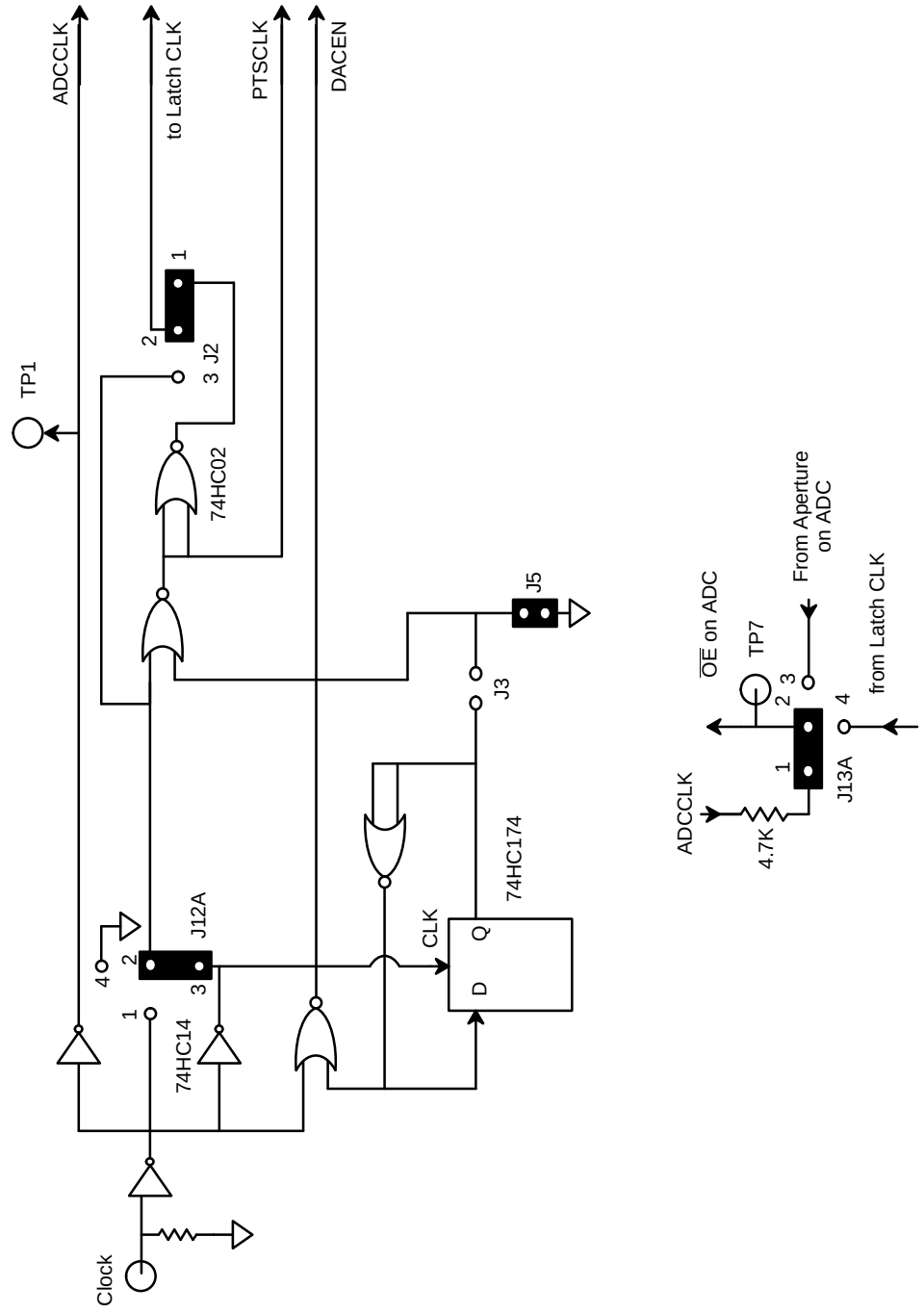
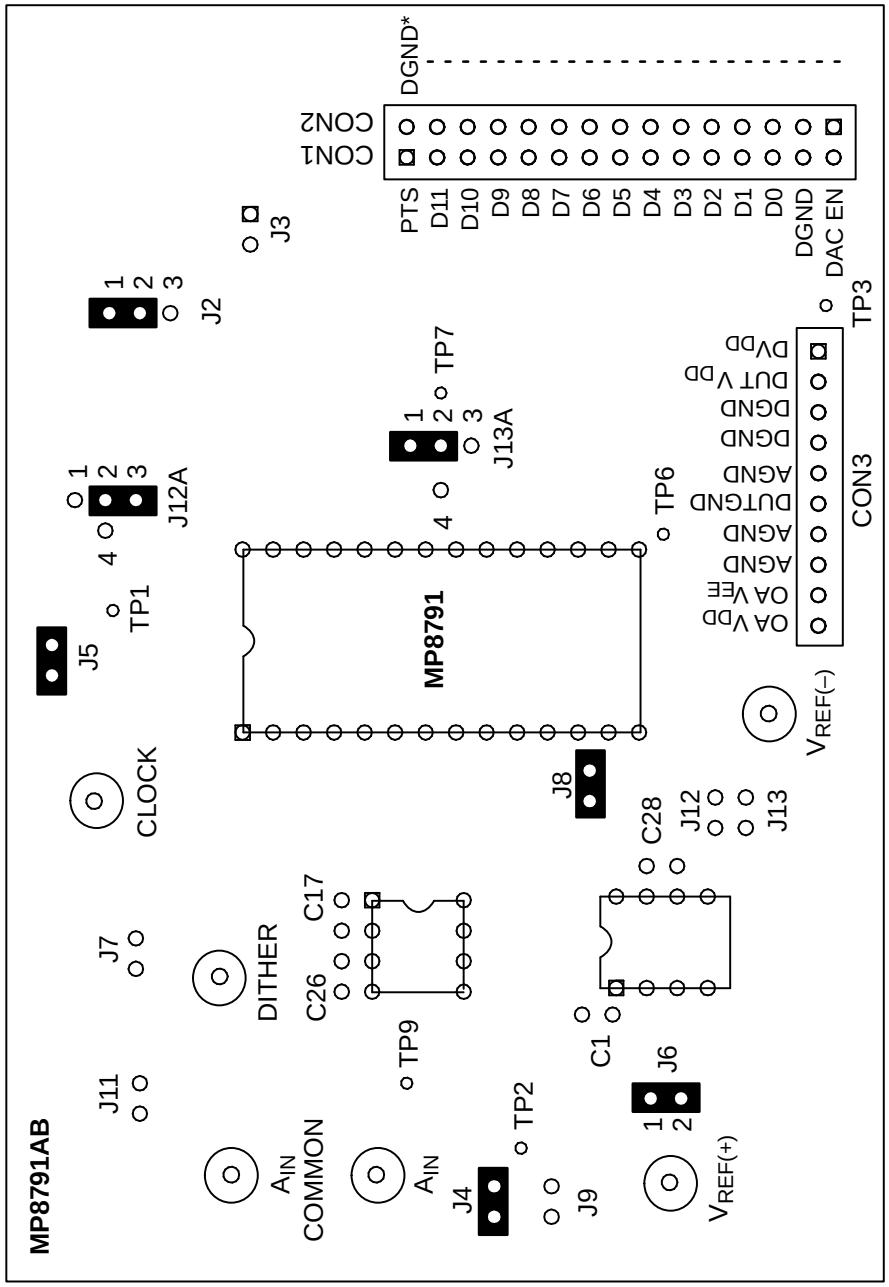


Figure 4. Default Jumper Configuration



*Note: All pins of CON2 are DGND.

Figure 5. MP8791AB Standard Jumper Settings

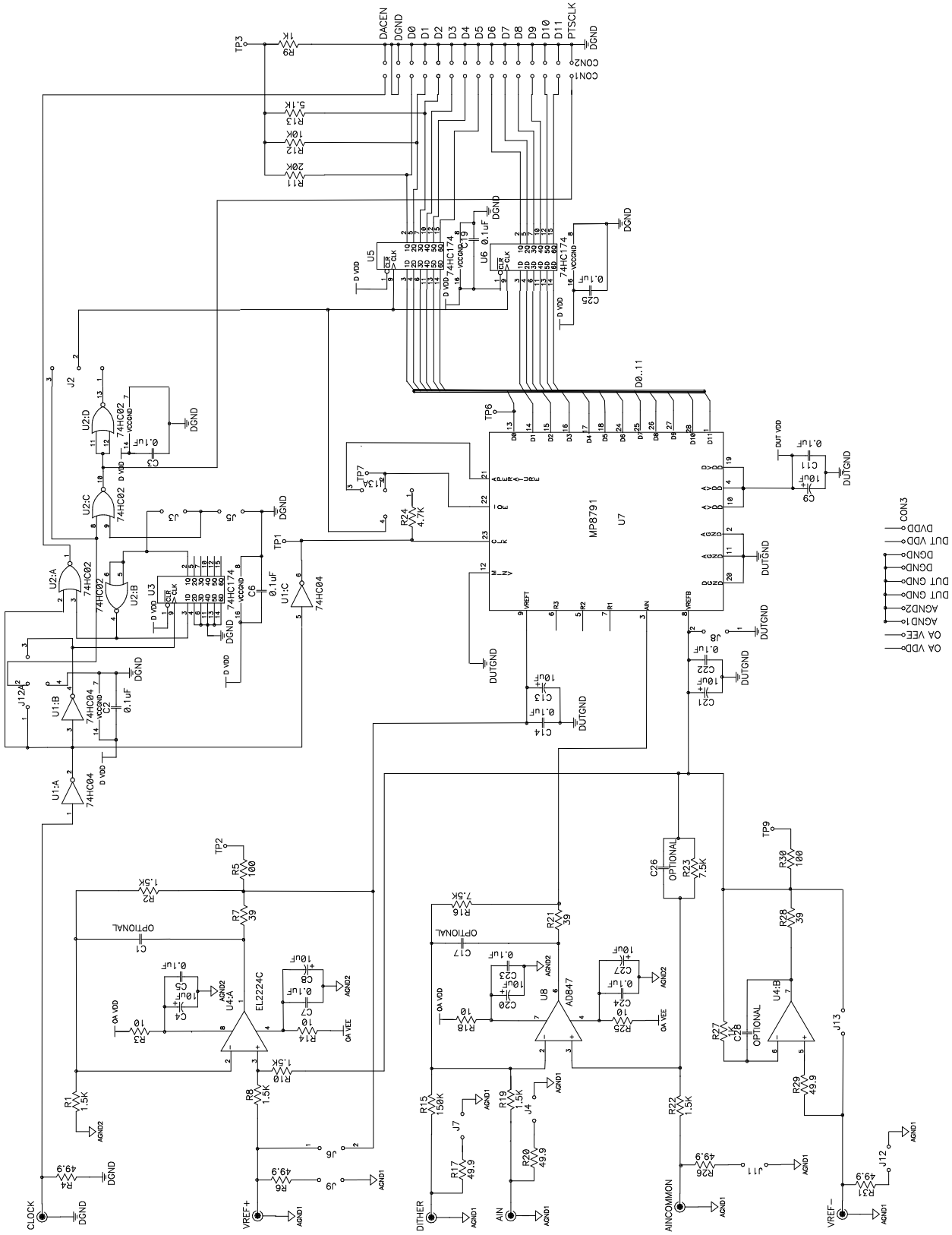


Figure 6. MP8791AB Schematic

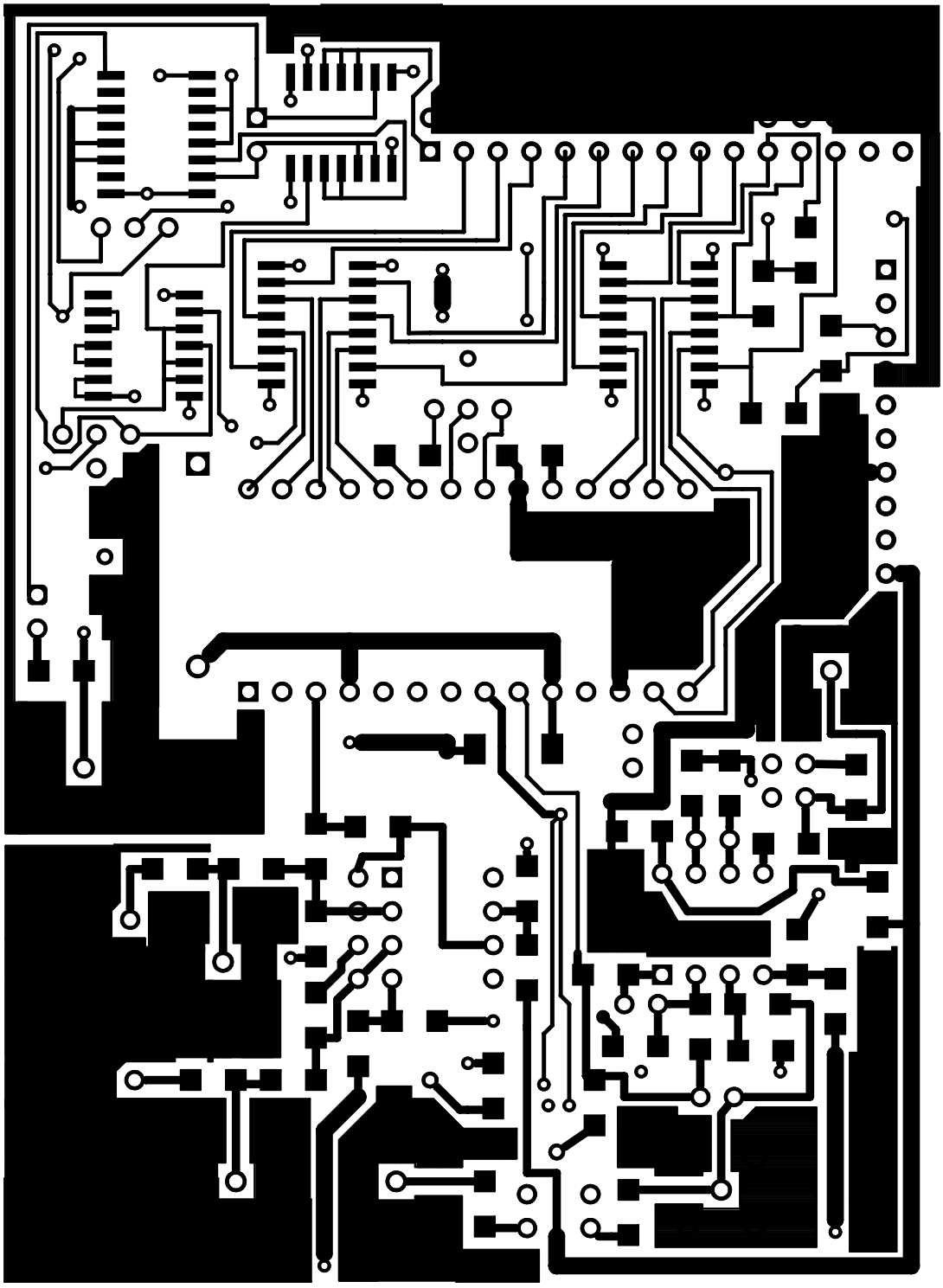


Figure 7. Top Trace

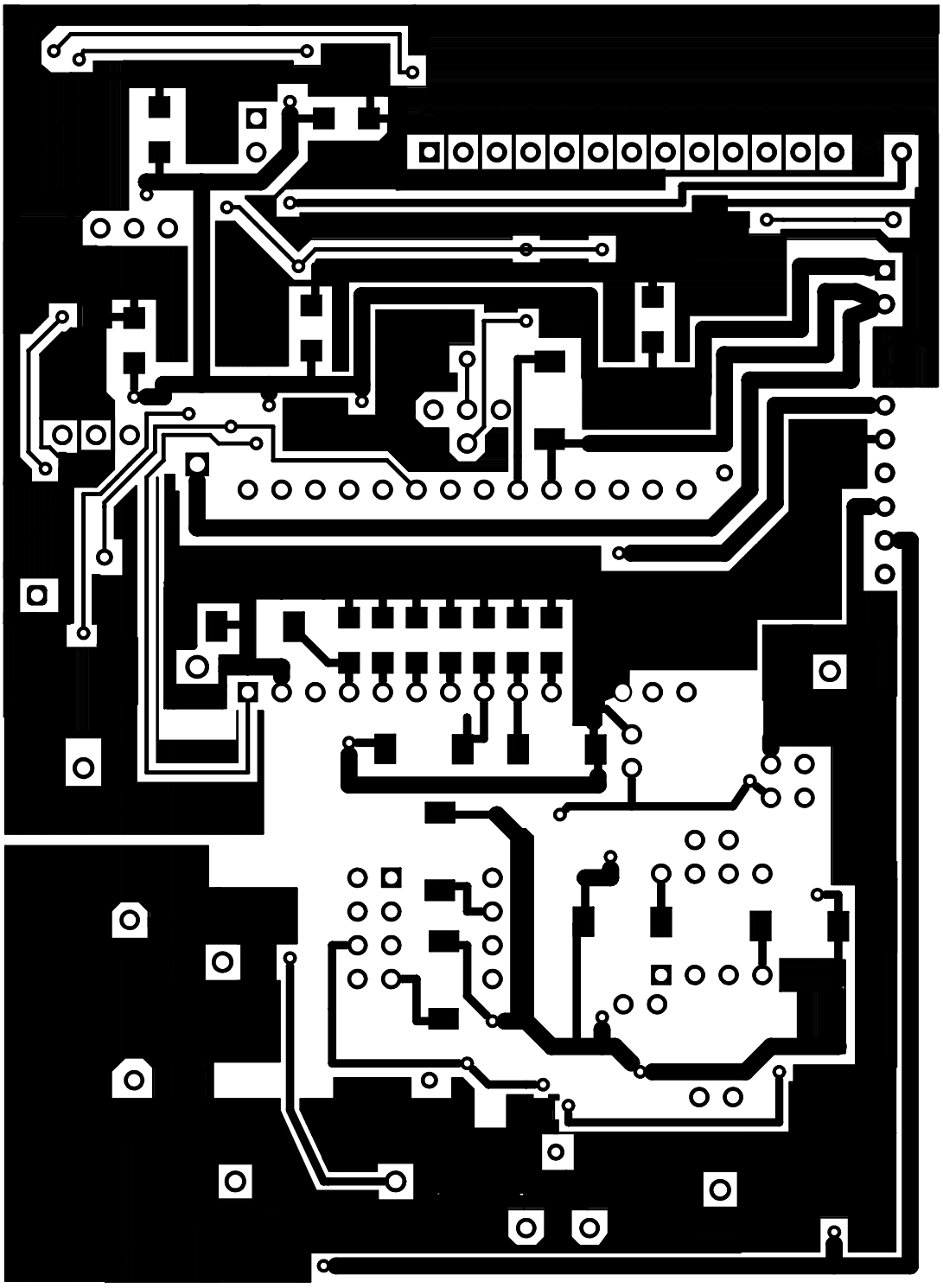


Figure 8. Bottom Trace

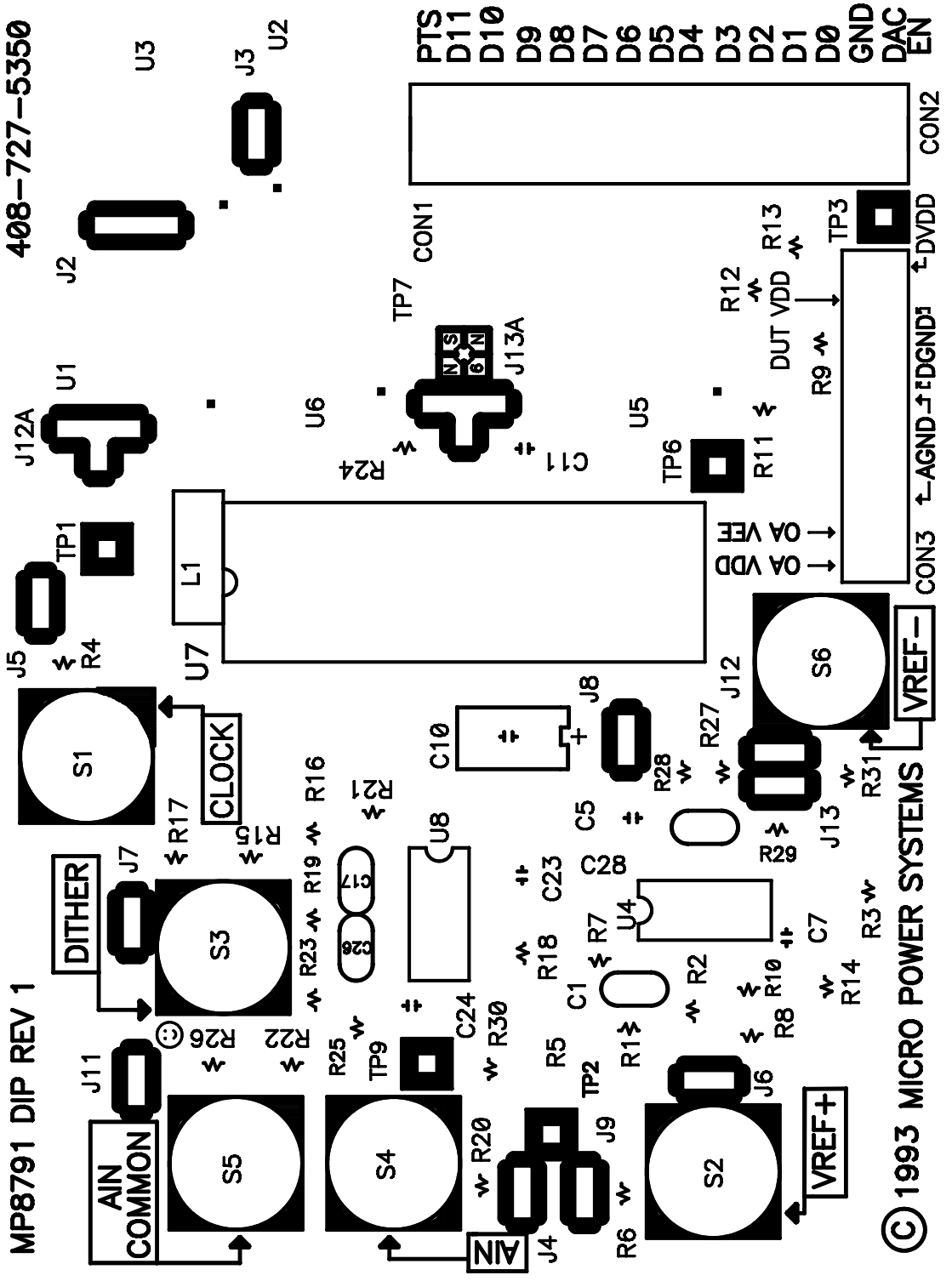


Figure 9. Top Silk

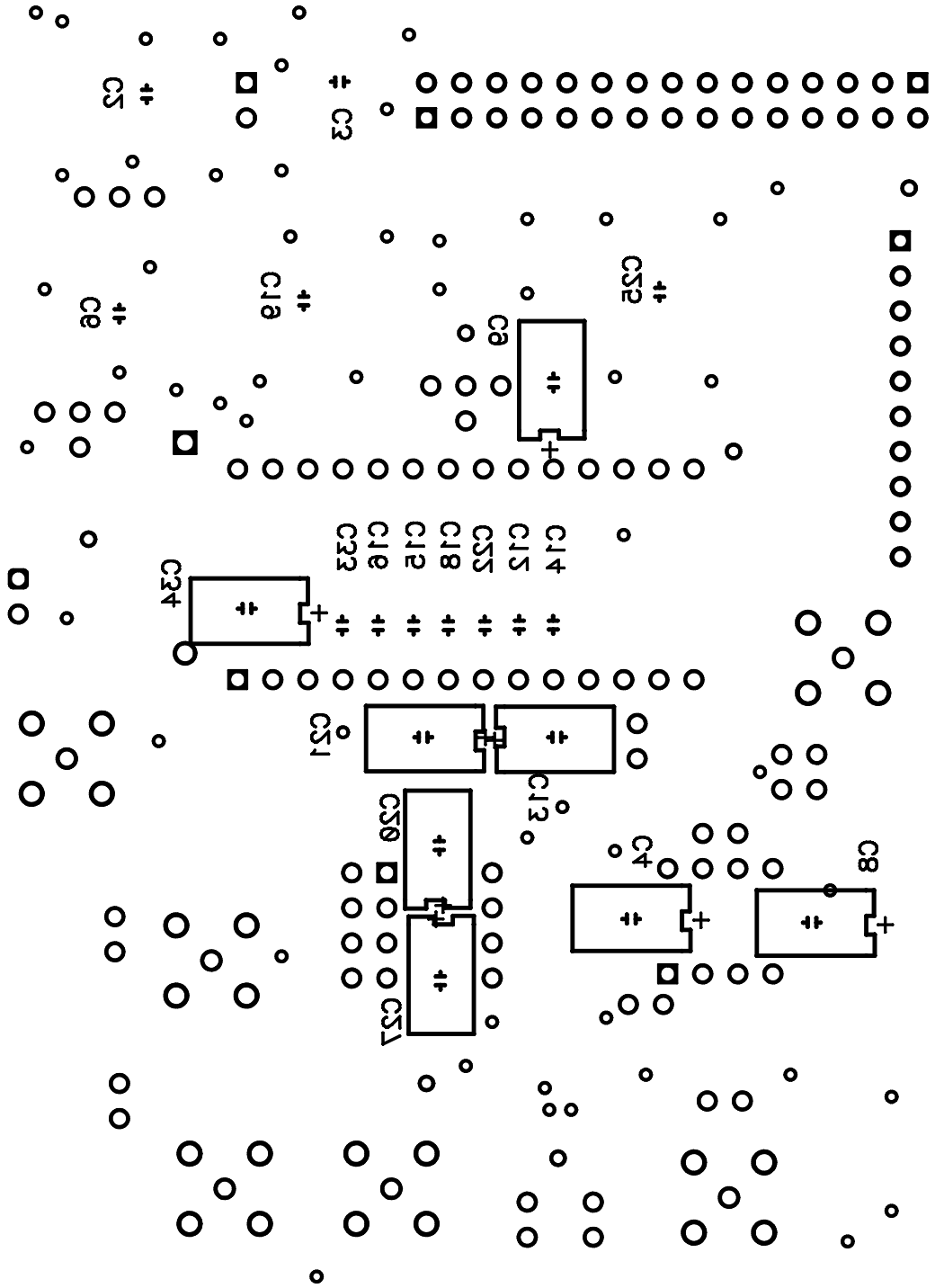


Figure 10. Bottom Silk – Top View