MP8785AB APPLICATION BOARD DOCUMENTATION

Evaluation Kit Parts List

This kit contains the following:

- One MP8785AB Applications Board with sample MP8785
- MP8785AB Documentation
- Circuit Diagram
- Layout Patterns

Features include:

- Easy Evaluation of the MP8785 8-bit ADC
- Optimized Printed Circuit Board Design
- Optimized Support Circuits
- User Friendly Interface
- Layout Applicable to Final Design

Introduction

The MP8785AB is a complete printed circuit test board designed to permit quick and accurate evaluation of the MP8785, 8-bit analog-to-digital converter. This application board combines a proven PC Board layout with optimized analog and digital interface circuitry to satisfy the stringent requirements needed in evaluating high performance devices of this type.

The board contains the device being tested (MP8785), an operational amplifier for input buffering, control logic and latches, and numerous connectors and jumper options.

With external laboratory equipment, complete DC and AC performance of the part can be evaluated.

Flexible user interface is provided by selectable jumper options and convenient connectors. Observation test points are available at commonly used locations.

A Preview of a Common Test Configuration

The board is set up as a general A/D test circuit where the references are fixed. *Figure 5.* shows the overall circuit, *Figure 4.* shows the defalt jumper settings, also listed in *Table I. Figures 6 through 9* show the PC board layout and component locations. There are many circuit possibilities built into the universal test board; however, starting with the default circuit is recommended.

Options for analyzing the output results are discussed in detail below. The most effective of these is the use of a high speed data acquisition system and FFT software to compute the performance parameters.

System Configuration

Two complete evaluation circuit block diagrams showing the MP8785AB with typical external test equipment are shown in *Figure 2. and Figure 3.* The following is a more detailed description of the major on-board and external components used in these systems as seen in *Figure 2., and Figure 3.*

Application Board Circuitry

The application board support circuitry is shown in *Figure 5.* The major components supporting the A/D under test are:

1. ANALOG INPUT AMPLIFIER – An operational amplifier is used in an instrumentation amp configuration (gain –1) to provide a low source impedance to the A/D. Provisions are made for summing a dither signal and/or offset voltage with the input. Holes for optional compensation caps are provided on-board.
2. DATA LATCH – The digital output of the A/D drive on-board latches which buffer the device under test from the external test equipment.
3. CONTROL LOGIC – Allows control of the data latch clocks as well as the $\overline{OE}$ pin of the DUT.

External Equipment Required

The system block diagrams (*Figure 2. and Figure 3.*) show the external test equipment required to perform all test and evaluation functions. These include:

1. POWER SUPPLIES – ±15 volt and one (or two) +5 volt external power supplies are needed. Decoupling circuits are provided on the applications board, however, low noise, low output impedance supplies are necessary for best performance. A connector (CON3) is used for all power and ground connections. This connector is the 10 pin connector located along the top of the board. For best results, twist the power supply cable pairs. This minimizes coupling to and from these to unrelated sections of the setup.

2. CLOCK GENERATOR – A symmetrical clock signal must be applied to the SMB coax connector labeled CLOCK. Note the 50Ω input impedance. This drives the MP8785 via a two inverter delay.

3. INPUT SIGNAL GENERATOR – A clean, low distortion sine wave generator should be used as a signal source. A band pass or low pass filter is sometimes required to further reduce harmonics and bandlimit noise as shown in *Figure 2.* The SMB coax connector labeled A_{IN} accepts the analog input. An on board op amp is used to buffer this input (gain of –1) and provide low source impedance to drive the A/D under test. The socket has a standard 741 type pinout which allows experimentation with alternative amplifiers. J9 provides a 50Ω input termination impedance.

4. DITHER INPUT – The cross plot test configuration (described later) requires a triangle wave signal source. This input is attenuated by a factor of 10 and added to the A_{IN} signal. J6 connects this input to a 50Ω termination resistor.

5. COMMON – An alternate, non inverting input (gain of one when dither is disconnected). Connect to ground when not used. J12 connects COMMON to ground via a 50 Ω resistor. This input allows use of differential inputs or is used for applying a DC offset for level shifting the A_{IN}.

6. OSCILLOSCOPE – The output TP2 of a dither DAC, is used to drive the vertical input of the oscilloscope for manual linearity testing using the “cross plot” method described on the following page.

Optional Equipment

1. DSP – Evaluation of dynamic and static performance is done by external processing devices that perform histogram and harmonic analysis to determine characteristics like linearity, noise, distortion, intermodulation effects, etc. The data is available at the CON2 connector.

2. REFERENCE SUPPLIES – Internal reference voltages can be used by connecting V_{RT} to V_{RTS} through jumper J3 (top position) and connecting V_{RB} to V_{RBS} through jumper J7 (top position). This generates 2.6 V at V_{RT} and 0.6 V at V_{RB}. Alternatively, J3 and J7 can be placed in their bottom positions to connect V_{RT} to V_{DD} and V_{RB} to GND.

3. PRECISION EXTERNAL OUTPUT DAC – As an alternative to DSP, a high speed precision digital to analog converter can reconstruct the output in analog form. The analog measurements can be used to evaluate the A/D’s performance using conventional analog instrumentation. Use the CLK pin of the output connector (CON2) to load the reconstruction DAC.

SYSTEM OPERATION

Analog Inputs

A_{IN} and COMMON Input Only

Differential input can be achieved by using A_{IN} and COMMON. If the dither input is left floating, then the differential input to the ADC is nominally given by:

$V_{IN} – V_{RB} = COMMON – A_{IN}$
where V_{IN} = MP8785 (pin 19)
V_{RB} = MP8785 (pin 23)

This allows reduction of common mode signals between A_{IN} and COMMON.

Dither and COMMON Input Only

With A_{IN} floating and a signal applied to DITHER:

$V_{IN} = 0.55 (COMMON + V_{RB}) – 0.1 (Dither)$
where V_{IN} = MP8785 (pin 19)
V_{RB} = MP8785 (pin 2)

Outputs

The parallel digital output of the A/D can be accessed on connector “CON1”. A system clock (CLK) is available on that connector. This output data, in conjunction with various input stimuli, is used to evaluate the A/D and timing performance. The three common methods are described below.

Digital Signal Processing

A comprehensive dynamic performance evaluation is most often done by using external hardware capable of fast digital data acquisition, storage and analysis. The computation of integral linearity, differential linearity, signal to noise and distortion ratios, the effective number of bits, and other useful figures of merit is done using software having histogram and FFT capability. The accuracy of the test results depends upon the quality of the input sine wave. A low distortion sine wave generator with a low pass filter will be necessary.

Commercial software packages with the needed computational features are available.

Analog Testing with External DAC

The logic output of the system can be converted back to analog by using a high performance digital to analog converter. Laboratory spectrum analyzers and oscilloscopes can be used to measure linearity, frequency response, harmonic distortion, noise, intermodulation distortion, etc. These measurements can be converted to the specifications commonly used in specifying A/D’s dynamically. In addition to a high quality sine wave input, the output D/A converter must be significantly more accurate than the A/D under test. The filtering effects of adding a zero order “hold” in the signal path are described in the Application Note MPSAN27 which can be found in the Micro Power Systems 1995 data book.

Cross Plot

An evaluation of differential linearity can be simply done with an oscilloscope, a triangle wave generator and a low noise DC signal source. Input jacks are provided on the board so this “cross plot” method can be conveniently implemented (See *Figure 3*.) The oscilloscope must be set in the X-Y display mode.

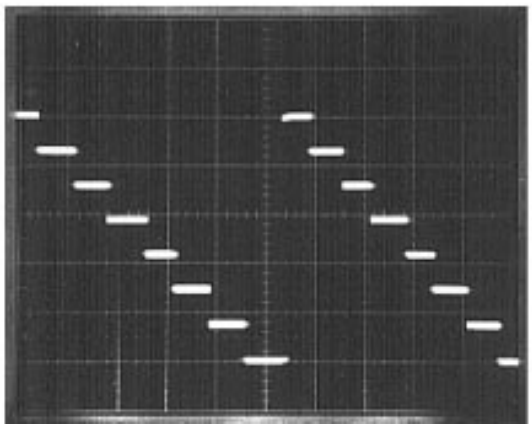

Figure 1. Cross Plot

A triangle wave (100 Hz) with a peak-to-peak amplitude of approximately 160 LSBs peak is supplied to the “dither” input. This is attenuated to 16 LSBs by the input amplifier. The triangle wave is also used to drive the x axis of the scope. The horizontal gain is set so that ±8 divisions are swept. Look at Test Point 2 (TP2) with the vertical input. Set the horizontal gain for 1 LSB per division.

A stair step waveform will result (See *Figure 1*.). By changing the DC input, eight code transitions can be observed about any DC input level. The horizontal distance between these transitions is the code width. Missing codes cause steps to be absent. By setting the endpoint thresholds to coincide with the scope grid lines, integral linearity errors are displayed as thresholds which are offcentered from these grid lines. A precision DC voltage source is necessary for the integral linearity measurement.

Since the conversion speed is much faster than the dither frequency, multiple readings are taken at each threshold. The horizontal variation of each threshold gives a qualitative measure of noise (in LSB's).

Using this "cross plot" method is a good way to prove out the lab setup prior to more sophisticated DSP test.

Jumper Options

The MP8785AB offers flexibility through configuration determining jumpers. These optional jumpers furnish choices for (1) input termination resistors, and (2) the selection of several logic and clock options. *Table I.* and *Figure 4.* show the jumper functions along with the default configuration set up prior to shipment.

Termination Options

Termination resistors (50 Ω) are provided for all inputs. The CLOCK input has a permanent termination resistor to DGND. The Dither, A_{IN} & COMMON inputs have termination resistors which are selected by shorting jumpers J6, J9 or J12 as indicated in Table I. The default configuration terminates A_{IN} & COMMON, but not Dither: J9 & J12 shorted, J6 open.

Reference Options

Jumpers J3 and J7 are used to set the top and bottom reference voltages for the ADC. Both of these are two position jumpers that connect V_{RT} (top reference) and V_{RB} (bottom reference) to either the internal reference bias (V_{RTS} & V_{RBS}) or to the supply rails. See Table I for a complete description. The default connects V_{RT} to V_{DD} and V_{RB} to GND: J3(1,2) J7(1,2).

Logic Options

There are two logic option configured by jumpers. The ADC always receives a clock that is delayed by two inverters from the externally applied clock input. Jumper J1 (next to CLOCK SMB) configures the output register to either latch every output from the ADC or every other output. Jumper J11 is used to connect the $\overline{OE}$ input of the ADC to GND (ADC outputs always active) or to a delayed version of the ADC clock (disable ADC outputs on high phase of clock to reduce digital noise). The default positions will latch every ADC output, J1(1,2), and connect $\overline{OE}$ to the delayed clock signal, J11(1,2).

Final Design Considerations

After the MP8785AB has been used to demonstrate that the MP8785, the clock timing, and the analog support circuits are acceptable, the design must be successfully transferred to the user's system. A close copy of the proven layout is recommended as is the use of identical support devices. Where this is not possible, the following advice should be heeded:

1. Be generous with analog and digital ground planes. Repeat as closely as possible the ground plane system on the application board. A four layer board with the two internal layers dedicated to power and ground planes is ideal.
2. Keep high frequency decoupling capacitors very close to the A/D pins and minimize the loop area included so less flux will induce less noise. Use decoupling capacitors in the same locations as on the MP8785AB.
3. Coupling between logic signals and analog circuitry can easily degrade an 8-bit system to a 6-bit system or worse. Completely separate them. Watch for coupling opportunities from other sources not immediately associated with the A/D. Don't use switching power supplies in adjacent locations for example.
4. Hi Z the A/D outputs during the V_{IN} sample time (when CLK is high).
5. Use support devices equivalent to those used on the evaluation board. Use the application board to verify these devices up front. Use very linear passive components in the signal path.
6. Select a driving op amp whose noise, speed, and linearity fits the application.

Additional Documentation

A set of drawings showing the details of the printed circuit board layout are given in *Figure 6., Figure 7., Figure 8. and Figure 9. Figure 5.* is the complete electrical circuit. *Figure 4.* shows the jumper locations.

Technical Hotline

For any application hints, please call our USA hotline at (408) 562-3615.

Table I. Jumper Options

Jumper	Description	Default
J1 (2, 1)	Output data at same rate as ADC clock	✓
J1 (2, 3)	Divides output latch clock by 2 for dynamic V_{REF} testing	
J3 (2, 1)	V_{RT} tied to AV_{DD} of MP8785	✓
J3 (2, 3)	V_{RT} tied to V_{RTS}: 2.6 V at V_{RT}	
J6	Dither terminated to GND via 50 Ω	
J7 (2, 1)	V_{RB} tied to GND	✓
J7 (2, 3)	V_{RB} tied to V_{RBS}: V_{RB} at 0.6 V	
J9	A_{IN} terminated to GND via 50 Ω	✓
J11 (2, 1)	$\overline{OE}$ tied to CLK via 2K Ω : $\overline{OE}$ delayed	✓
J11 (2, 3)	$\overline{OE}$ tied to GND: The data is continuously available to the latches	
J12	COMMON terminated to GND via 50 Ω	✓

Notes:
1. J*x* (a, b) means short pins a and b of jumper *x*.
2. The ADC clock is not affected by the jumper combinations and is the same as the external clock – except for a 2 inverter delay.

Table II. Test Points

TP1	Output Data Latch Clock
TP2	Cross Plot Output

Table III. List of Components

Qty	Value	Ref Designators
1	74HC574	U3
1	74HC04	U1
1	74HC174	U2
1	MP8785	U4
1	Op Amp (AD811 AN)	U5
8	10µF	C5, C6, C8, C9, C12, C16, C18, C22
12	0.1µF	C1, C2, C3, C4, C7, C10, C11, C13, C15, C17, C19, C20
2	1 pF	C14, C21
1	2 KΩ	R15
4	1.5KΩ	R7, R10, R14, R17
1	10KΩ	R3
1	5KΩ	R4
1	2.5KΩ	R5
2	10Ω	R9, R16
1	15KΩ	R6
6	49.9Ω	R1, R11, R12, R13, R8, R18
1	1KΩ	R2
4	SMB CONNECTOR	A_{IN}, CLOCK, DITHER, COMMON
2	TESTPOINT	TP1, TP2
3	50 Ω Cables	BNC Male to SMB Jack. Can be purchased from Pasternack, Irvine, CA.
7	Jumpers	J1, J3, J7, J9, J11, J12, J7
18	IC Socket Pins	
3	10 Pin Header Connector	CON 1, CON2, CON3
1	PCB–Rev 0	MP8785AB PC Board

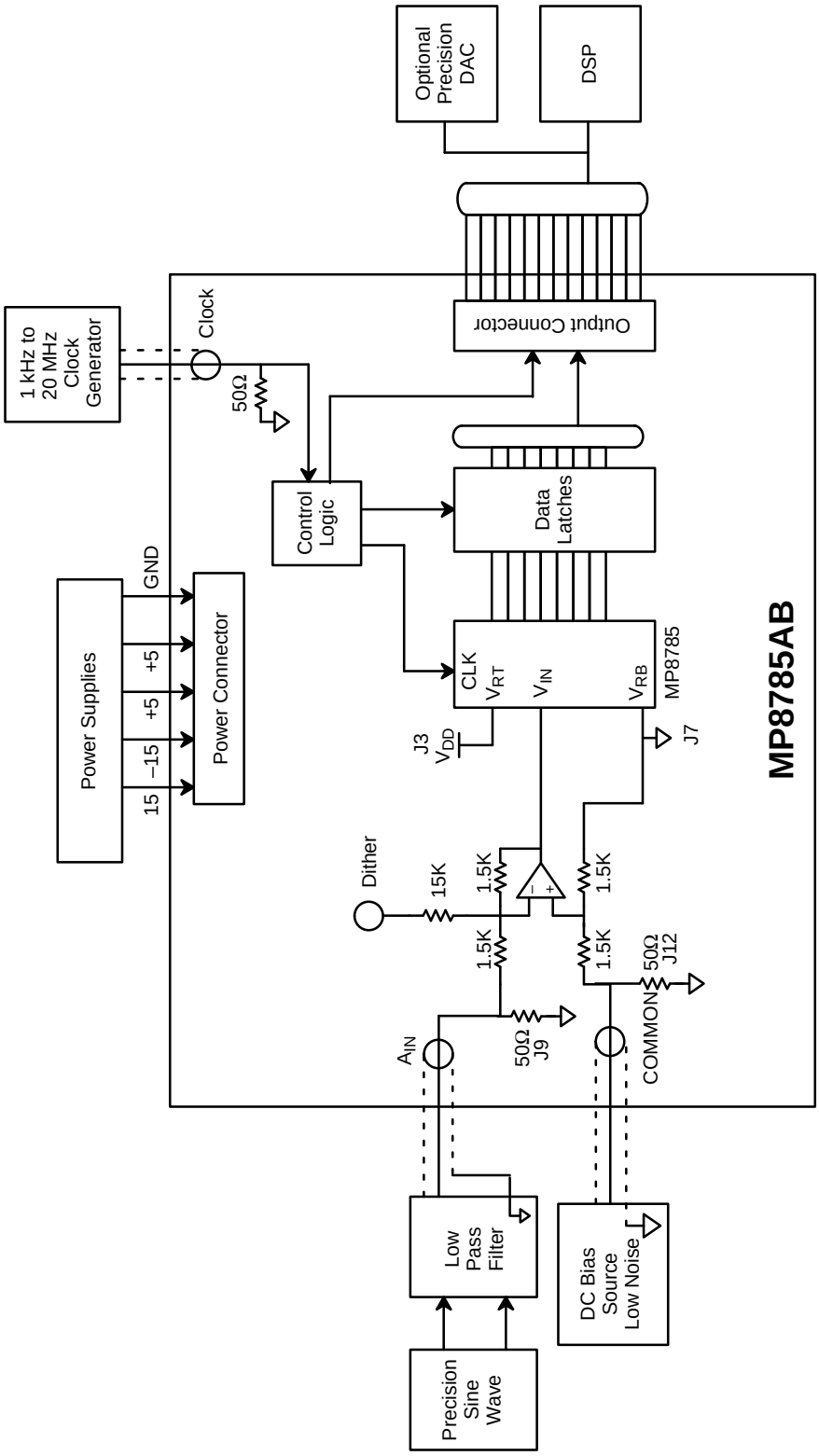

Figure 2. General A/D Test Circuit with Fixed Reference

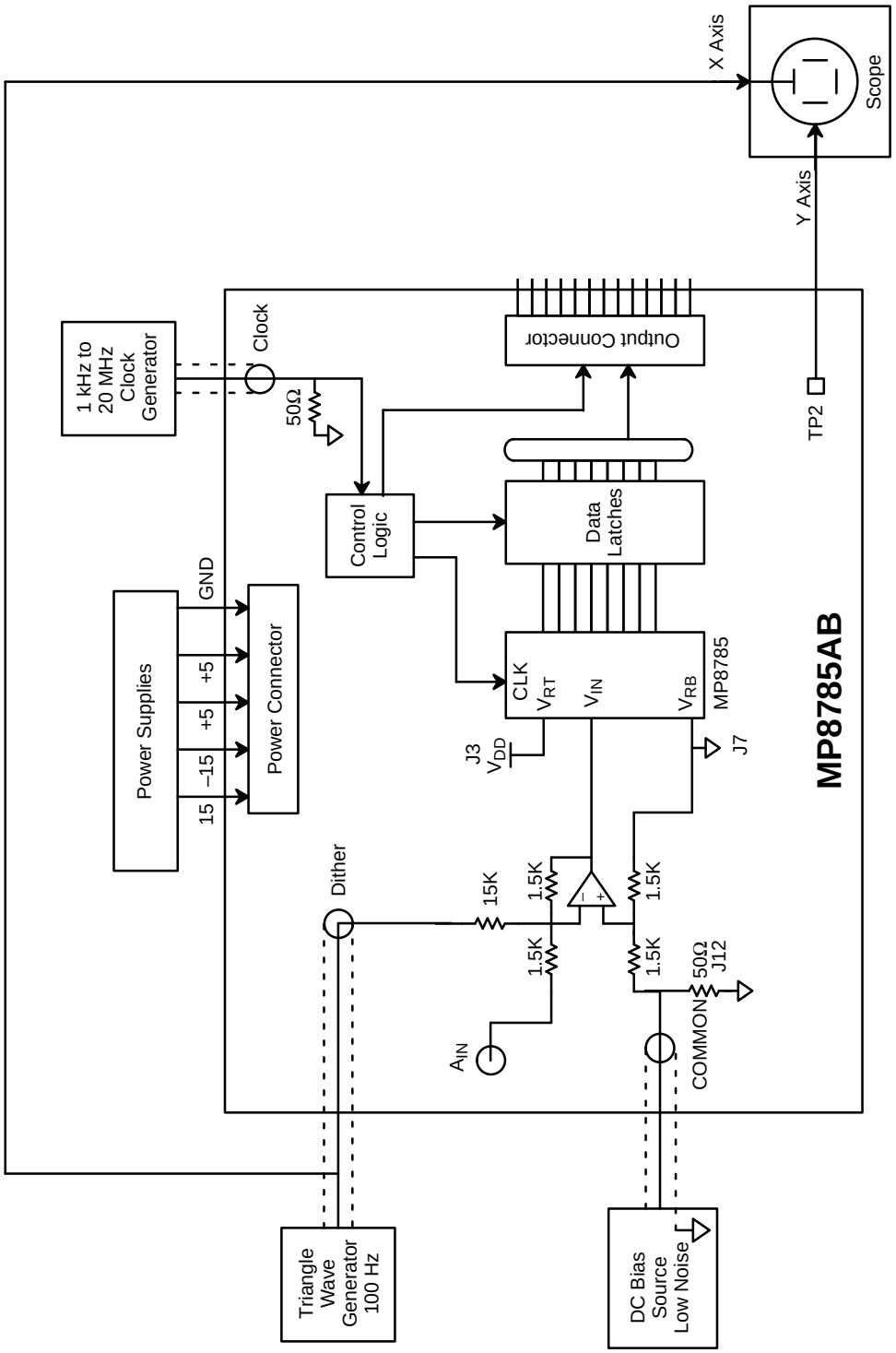

Figure 3. "Cross Plot" Set-Up

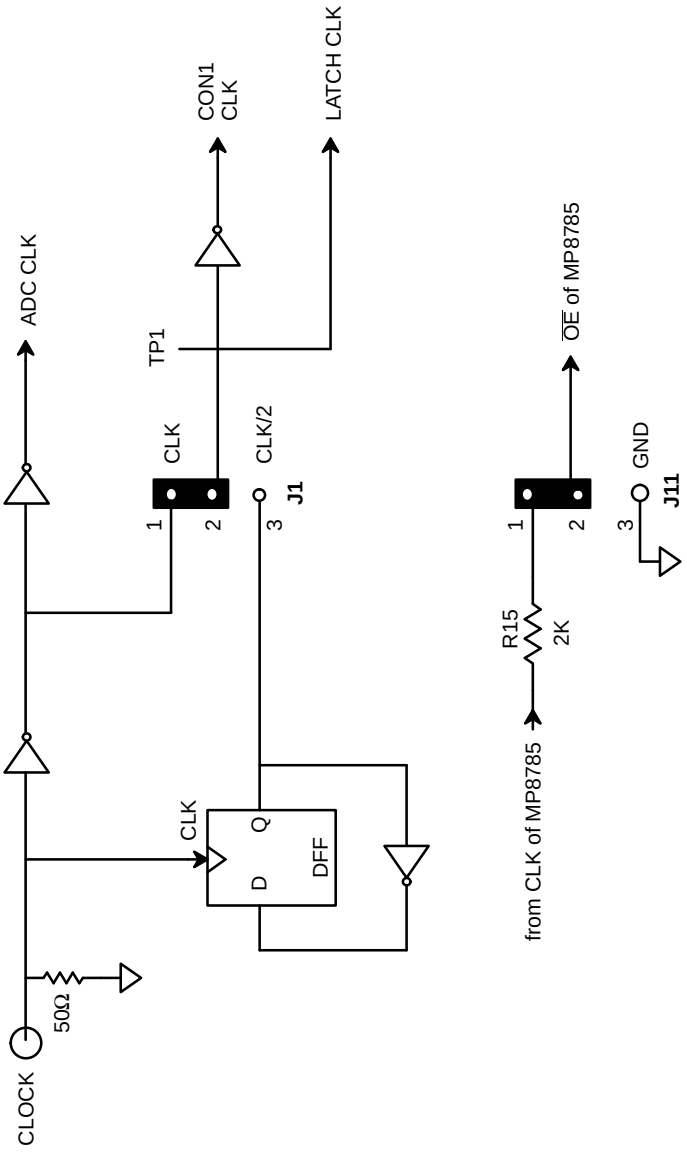

Figure 4. Default Jumper Configuration

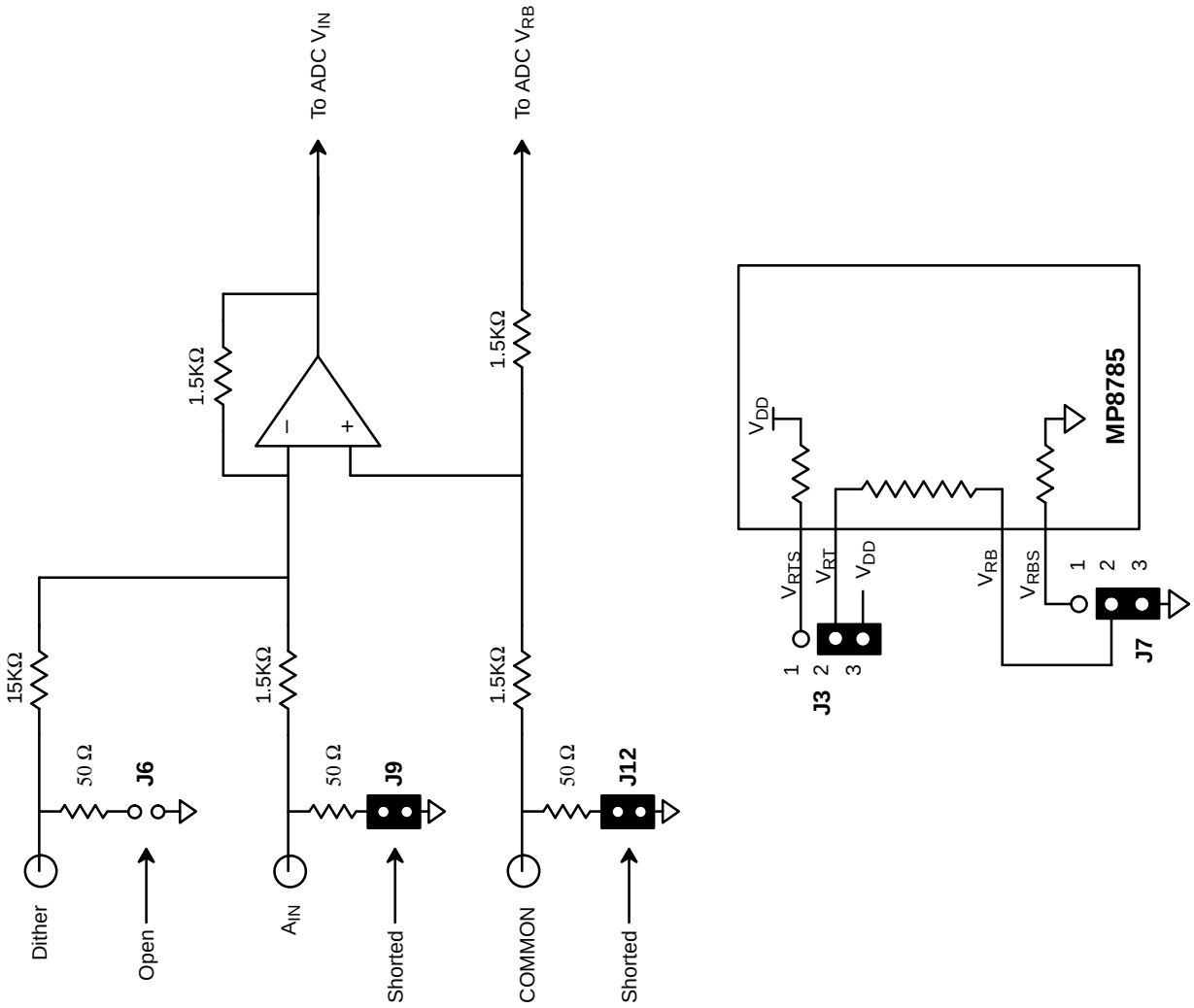

Figure 4. (Cont'd) Default Jumper Configurations

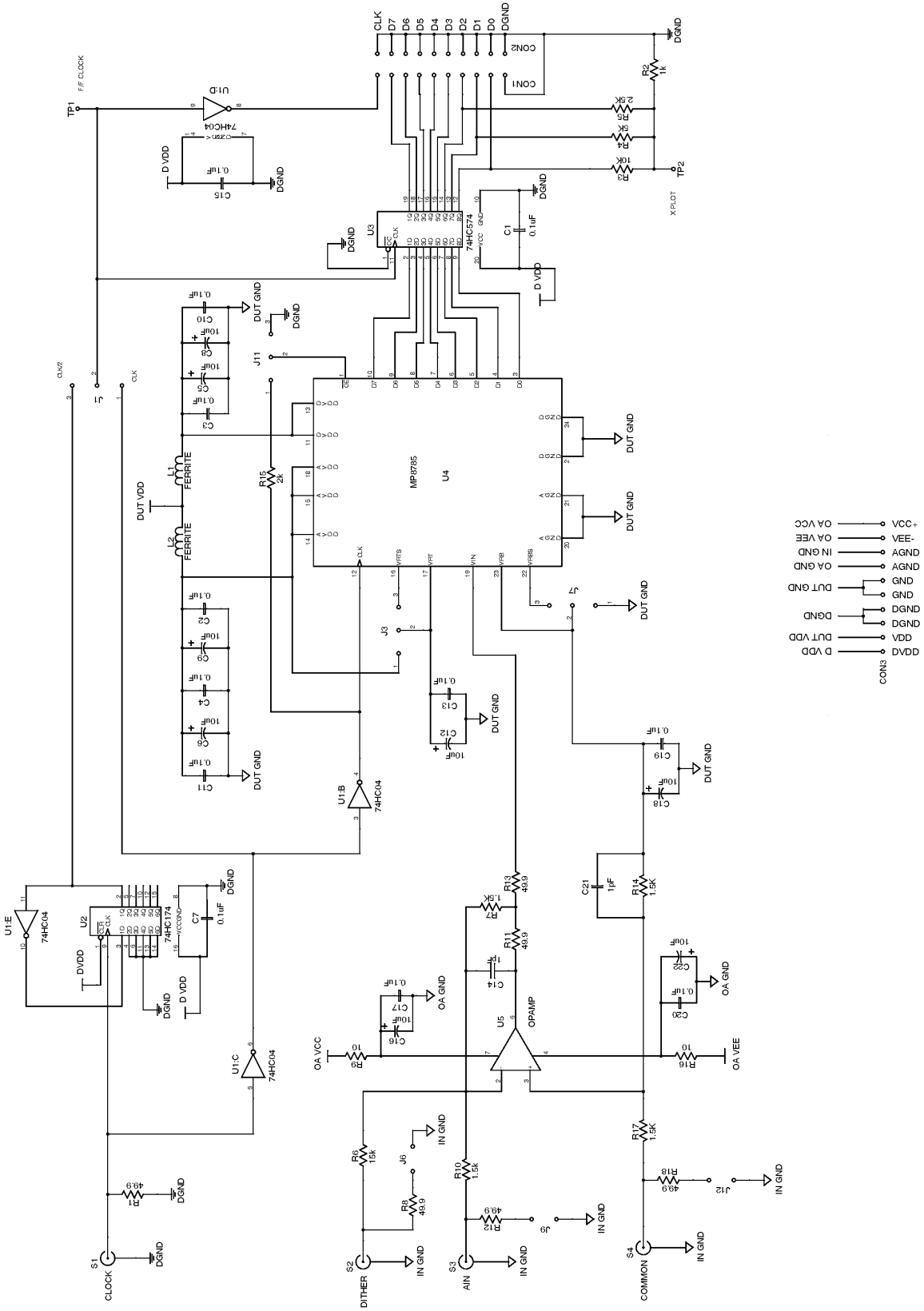

Figure 5. MP8785AB Schematic

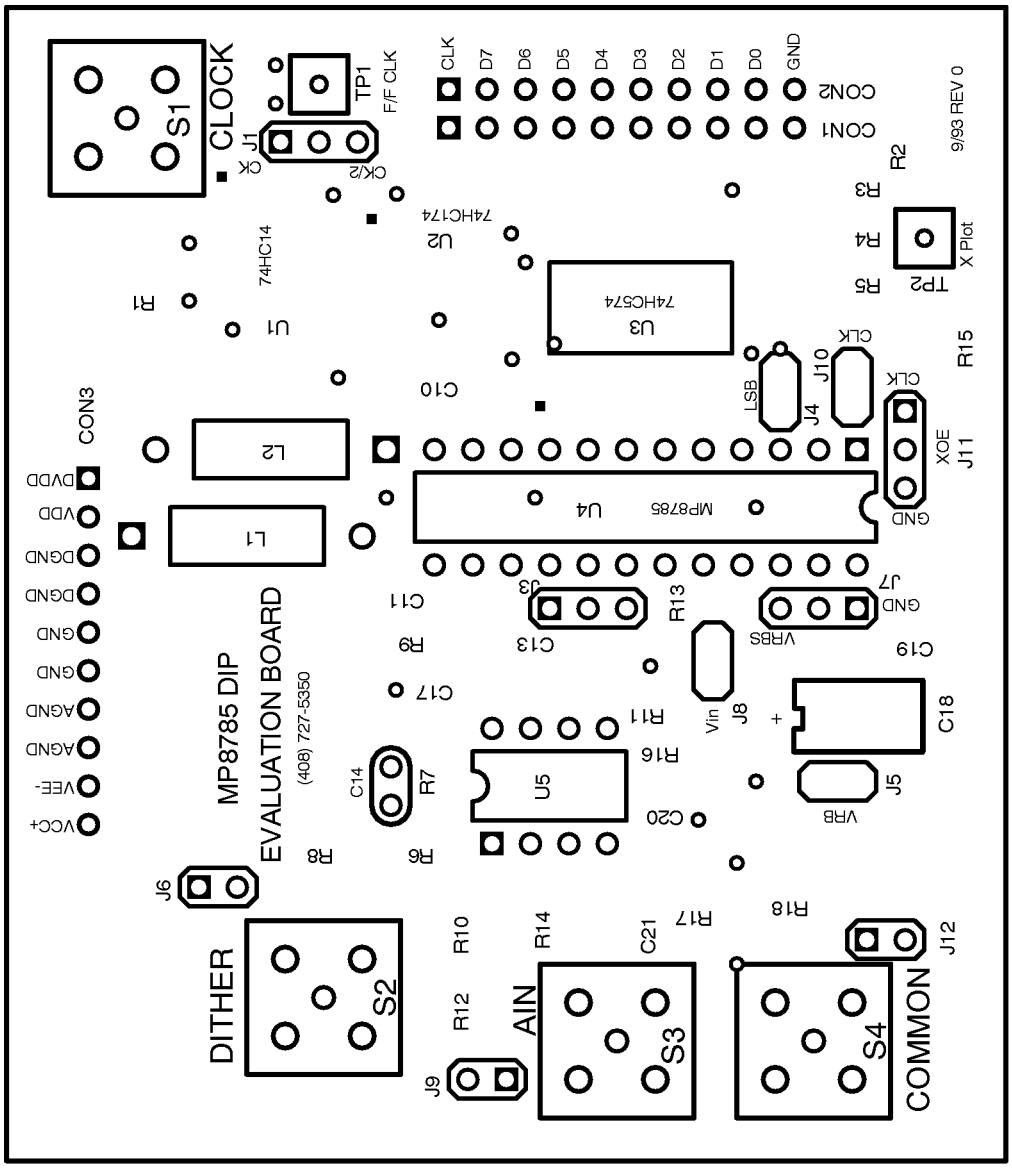

Figure 6. Top Silk

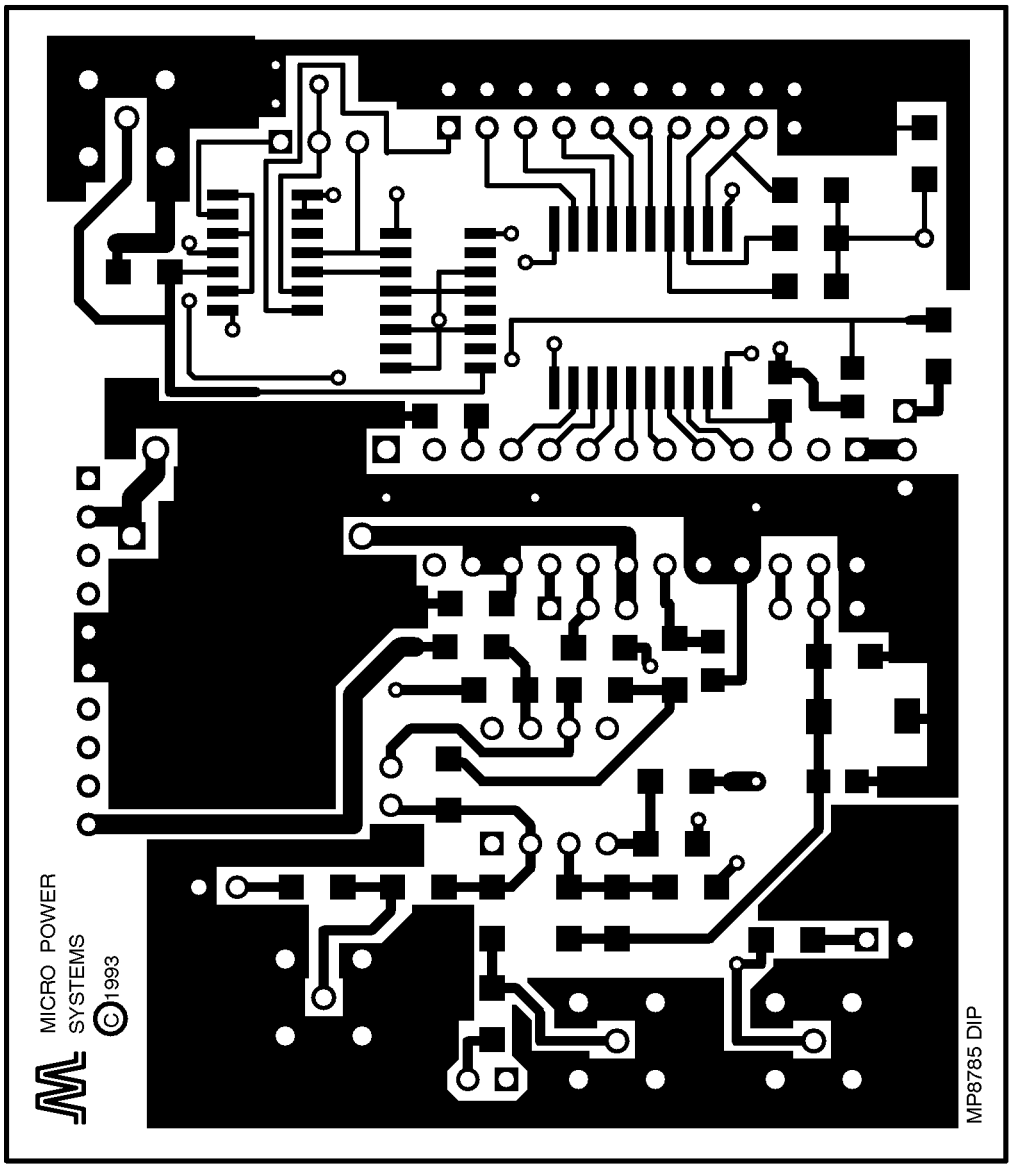

Figure 7. Top Trace

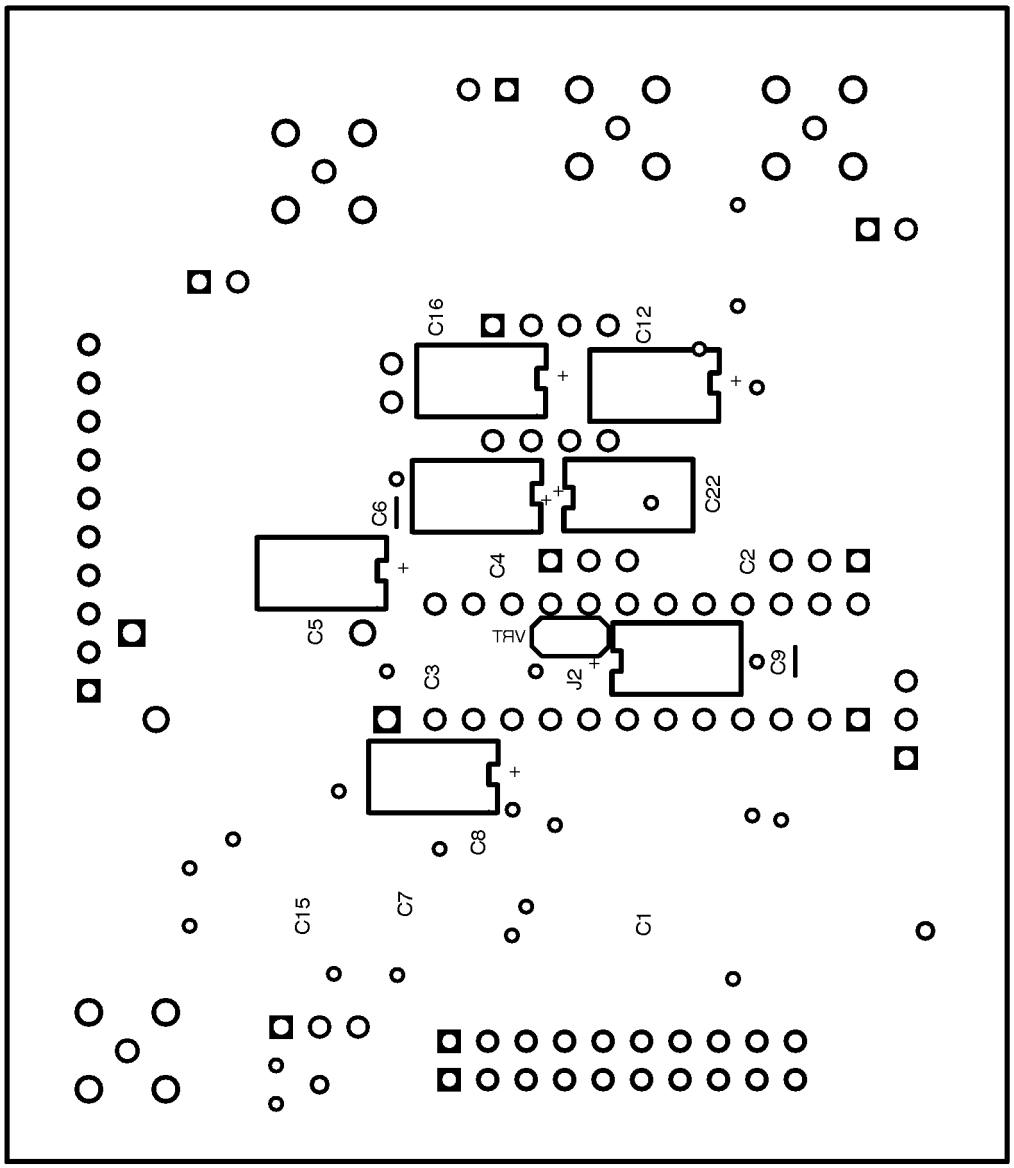

Figure 8. Bottom Silk (Bottom View)

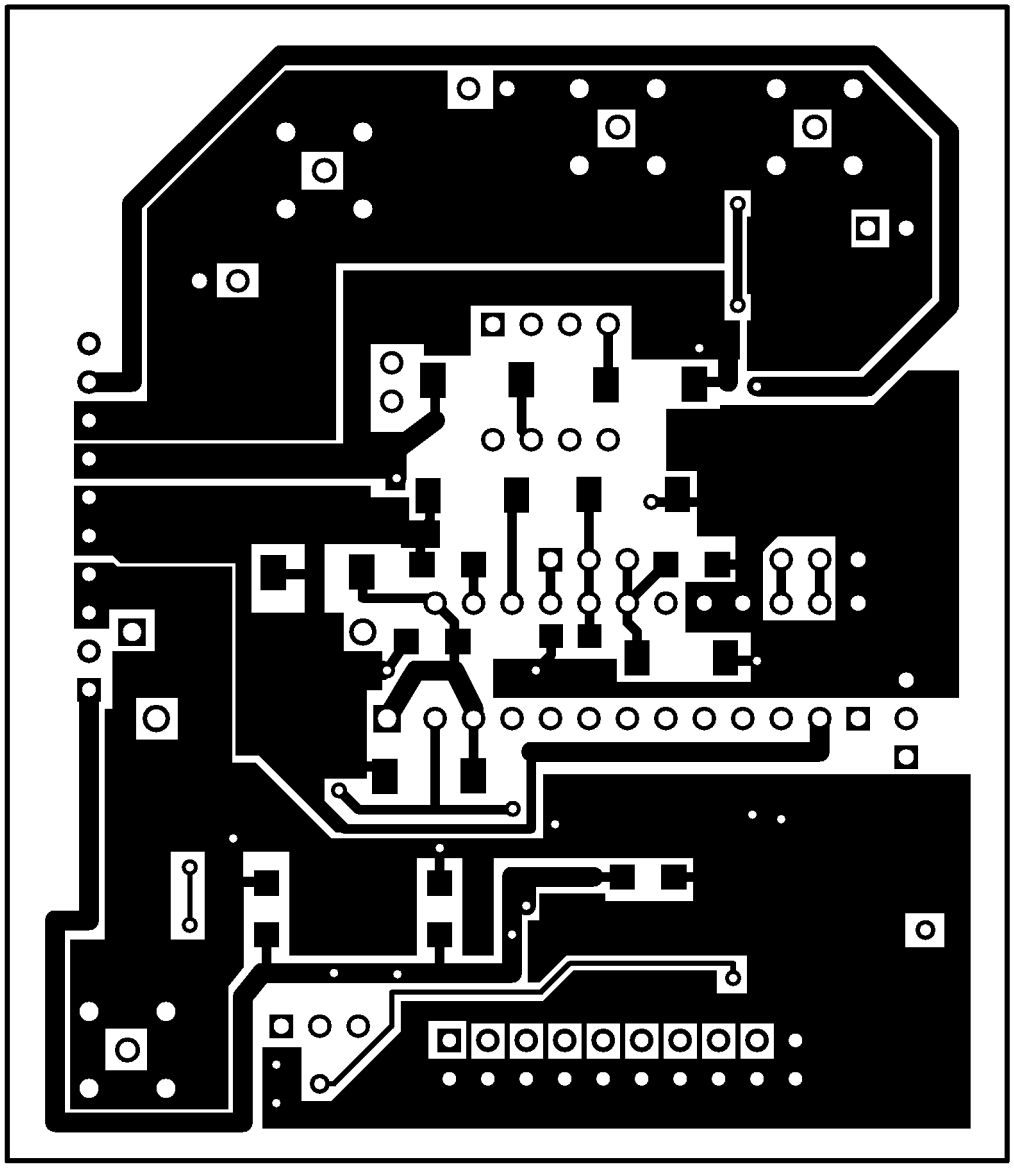

Figure 9. Bottom Trace (Bottom View)