MP8782

CMOS
5 MSPS, 10-Bit High Speed
Analog-to-Digital Converter

FEATURES

- **10-Bit Resolution**
- **5 MHz Sampling Rate**
- **DNL = ±1 LSB, INL = ±2 LSB**
- **Internal S/H Function**
- **Single 5 V Power Supply**
- **V_{IN} DC Range: 0 V to V_{DD}**
- **V_{REF} DC Range: 1 V to V_{DD}**
- **Low Power: 175 mW**
- **Bipolar Range using RTS & RBS; +1.4 V to –1.4 V**
- **R1 - R7 Reference Ladder Taps (1/8th – 7/8th points)**
- **Aperture Delay Sync Signal**
- **MINV & LINV Digital Output Format Controls**
- **PHASE Control**
- **Overflow and Underflow bits**
- **Dual 3-State Controls ($\overline{OE1}$ & OE2)**
- **Three-State Digital Outputs**
- **Latch-Up Free**
- **3 V Version: MP87L82**

APPLICATIONS

- **Digital Color Copiers**
- **Digital Cellular Telephones**
- **Precision CCDs and Scanners**
- **Medical Scanners**
- **Ultrasonics**
- **Digital Radio**

BENEFITS

- **Simplified Analog Design**
- **Rugged**
- **Few External Components, no S/H Needed**
- **Reduced Board Space**

GENERAL DESCRIPTION

The MP8782 is a full featured 10-bit, 5 MSPS, Analog-to-Digital Converter for applications that require high speed and high accuracy. Designed using an advanced 5 V CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

The MP8782 uses a subranging architecture to maintain low power consumption at high conversion rates. Our proprietary comparator design achieves a low analog input capacitance. The input circuitry of the MP8782 includes a S/H function and internal resistors that allows this part to digitize analog input signals between – V_{RT} to V_{DD} using a single supply.
(Unipolar and Bipolar Conversion capability)

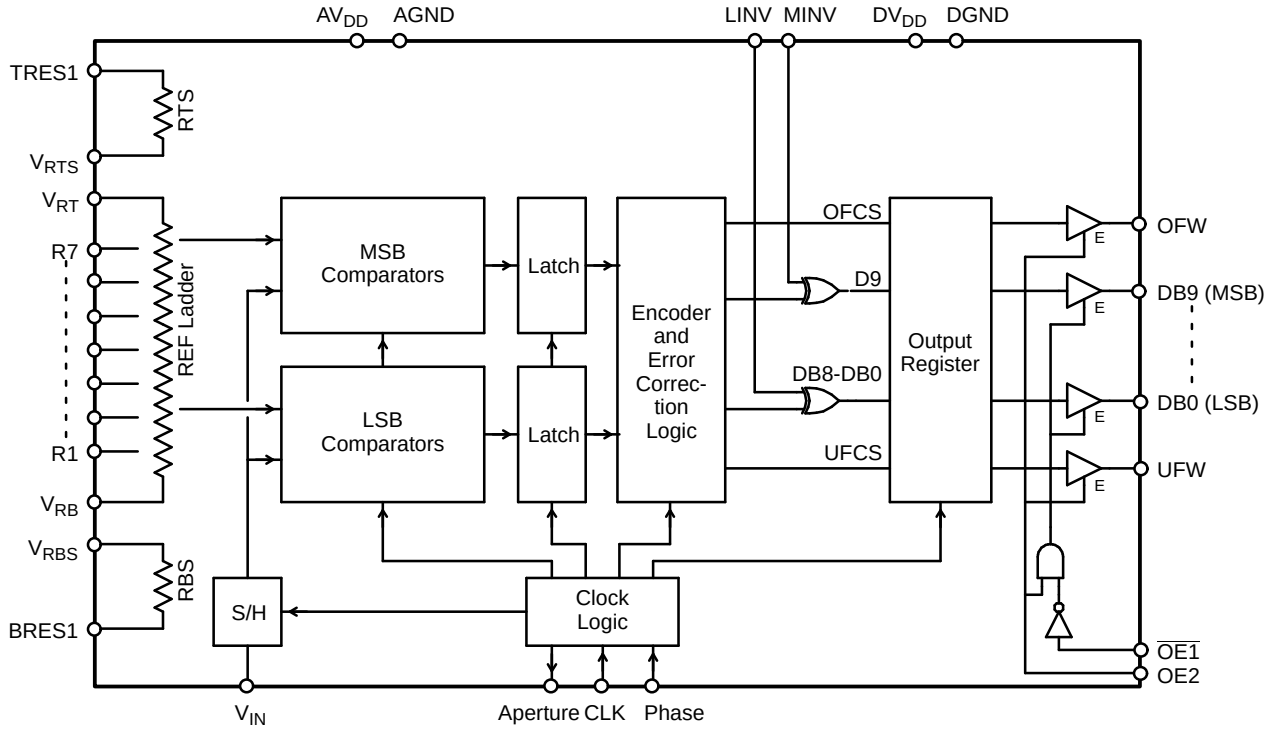
The designer can choose the internally generated reference voltages, or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 1.0 V at V_{RB} and 4.0 V at V_{RT}. Providing external reference voltages allows easy interface to any input signal range between AGND and AV_{DD}. This also allows the system to cancel zero scale and full scale errors. The Reference Ladder taps (R1 to R7) can be used to externally trim any INL errors, or to shape the A/D converter transfer function.

This device operates from a single 5 V supply. Power consumption from a 5 V supply is typically 175 mW at F_S=5MHz, and only 150 mW at F_S=1MHz.

ORDERING INFORMATION

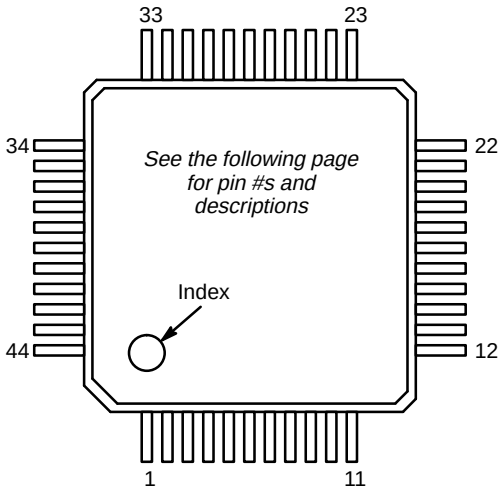
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PQFP	–40 to +85°C	MP8782AE	±1	±2

SIMPLIFIED BLOCK DIAGRAM



PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



44 Pin PQFP
Q44

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	V_{RT}	Top of Ladder
2	R7	Reference Ladder Tap @ 7/8
3	R6	Reference Ladder Tap @ 3/4
4	R5	Reference Ladder Tap @ 5/8
5	R4	Reference Ladder Tap @ 1/2
6	AV_{DD}	Analog Power Supply
7	A_{IN}	Analog Input
8	AGND	Analog Ground
9	R3	Reference Ladder Tap @ 3/8
10	R2	Reference Ladder Tap @ 1/4
11	R1	Reference Ladder Tap @ 1/8
12	V_{RBS}	Bottom Bias Resistor Terminal 2
13	N/C	No Connection
14	V_{RB}	Bottom of Ladder
15	Bres1	Bottom Bias Resistor Terminal 1
16	DGND	Digital Ground
17	OE2	Output Enable 2 (Input, Active High)
18	$\overline{OE1}$	Output Enable 1 (Input, Active Low)
19	UFW	Underflow (Output)
20	DB0	Data Output Bit 0 (LSB)
21	DB1	Data Output Bit 1
22	N/C	No Connection
23	DB2	Data Output Bit 2
24	DB3	Data Output Bit 3
25	DB4	Data Output Bit 4
26	N/C	No Connection
27	PHASE	Clock Polarity Control (Input)
28	LINV	Non MSB Digital Output Format (Input)
29	MINV	MSB Digital Output Format (Input)
30	N/C	No Connection
31	DB5	Data Output Bit 5
32	DB6	Data Output Bit 6
33	DB7	Data Output Bit 7
34	N/C	No Connection
35	N/C	No Connection
36	DB8	Data Output Bit 8
37	DB9	Data Output Bit 9 (MSB)
38	OFW	Overflow (Output)
39	CLK	Clock Input
40	Aperture	Aperture Delay Sync (Output)
41	DV_{DD}	Digital Power Supply
42	Tres1	Top Bias Resistor Terminal 1
43	V_{RTS}	Top Bias Resistor Terminal 2
44	N/C	No Connection

The MP8782 is the full featured version of Exar's 5 MSPS 10-bit A/D Converter. The MP8784 is one alternate pinout with reduced pin count and reduced features.

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, FS = 5 MHz (50% Duty Cycle), V_{RT} = 4.0, V_{RB} = 1.0, TA = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution			10		Bits	
Sampling Rate	FS			5	MHz	
ACCURACY (A, S Grades)[1]						
Differential Non-Linearity	DNL			±1	LSB	
Integral Non-Linearity	INL			±2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		10		LSB	
Full Scale Error	EFS		6		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	V_{RT}			AV_{DD}	V	
Negative Ref. Voltage	V_{RB}	AGND			V	
Differential Ref. Voltage[3]	V_{REF}	1.0		AV_{DD}	V	$V_{REF} = V_{RT} – V_{RB}$
Ladder Resistance	R_L		375		Ω	
Ladder Temp. Coefficient	R_{TCO}		2000		ppm/°C	
Top Internal Reference	V_{RTS}		4		V	V_{RT} connected to V_{RTS} &
Bottom Internal Reference	V_{RBS}		1		V	V_{RB} connected to V_{RBS}
ANALOG INPUT[2]						
Input Bandwidth (–1 dB)[4]	BW		10		MHz	
Input Voltage Range	V_{IN}	V_{RB}		V_{RT}	V	
Input Capacitance Sample[5]	C_{IN}		25		pF	
Input Capacitance Convert[5]			5		pF	
Aperture Delay	t_{AP}		25		ns	
Aperture Delay from Aperture Out			0		ns	5pF Load
Aperture Uncertainty (Jitter)	t_{AJ}		50		ps	
DIGITAL INPUTS						
Logical “1” Voltage	V_{IH}	4			V	
Logical “0” Voltage	V_{IL}			1	V	
DC Leakage Currents[6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK			5		µA	
$\overline{OE1}$, MINV, LINV (Internal Res to DGND)[7]			15		µA	
$\overline{OE2}$, Phase (Internal Res to DV_{DD})[7]			15		µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1*)						
Clock Period	1/FS		200		ns	
Rise & Fall Time[8]	t_R, t_F		5		ns	
“High” Pulse Width	t_{PWH}		100		ns	
“Low” Pulse Width	t_{PWL}		100		ns	
Duty Cycle			50		%	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	4.5			V	I_{LOAD} = 4 mA
Logical "0" Voltage	V_{OL}			0.4	V	I_{LOAD} = 4 mA
Tristate Leakage	I_{OZ}		10		µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay	t_{DL}		40		ns	
Data Enable Delay	t_{DEN}		25		ns	
Data Tristate Delay	t_{DHZ}		25		ns	
POWER SUPPLIES						
Operating Voltage (AV_{DD}, DV_{DD})[9, 10]	V_{DD}		5		V	
Current (AV_{DD} + DV_{DD})	I_{DD}		35	45	mA	

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/1024) is the DNL error (*Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 4.*). Accuracy is a function of the sampling rate (FS).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 –1 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.

5 See V_{IN} equivalent circuit (*Figure 8.*). Switched capacitor analog input requires driver with low output resistance.

6. All inputs have diodes to DV_{DD} and DGND. Input $\overline{OE}$ has internal pull down. Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.

7 Internal resistor to DGND biases unconnected input to active low logical level.

8 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.

9 The AGND & DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.

10 The AV_{DD} & DV_{DD} pins should go to the same voltage and separately decoupled.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +7 V
RTS & RBS terminals ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V

Storage Temperature ..... –65 to +150°C
PQFP Package Dissipation @ 75°C ..... 800 mW
Derates above 75°C ..... 11mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

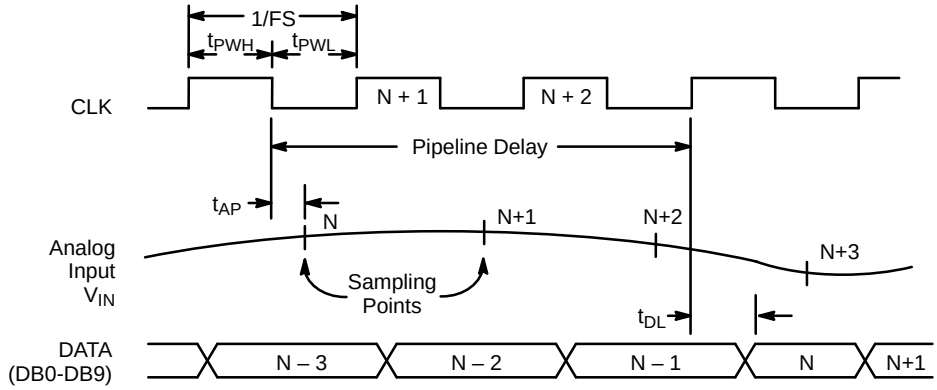


Figure 1. MP8782 Timing Diagram

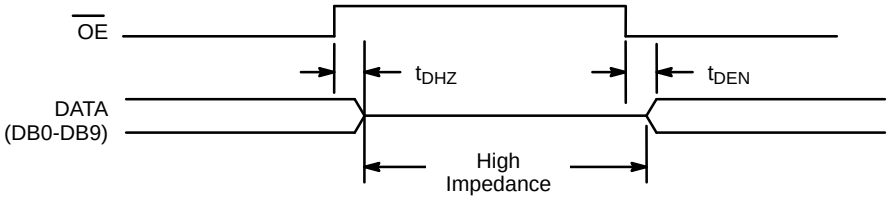
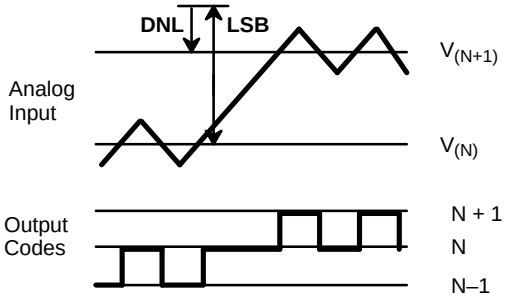


Figure 2. 3-State Timing Diagram



Code Width (N) = $V_{(N+1)} – V_{(N)}$
LSB = [$V_{RT} – V_{RB}$] / 1024

$DNL_{(N)}$ = [$V_{(N+1)} – V_{(N)}$] – LSB

Figure 3. DNL Measurement

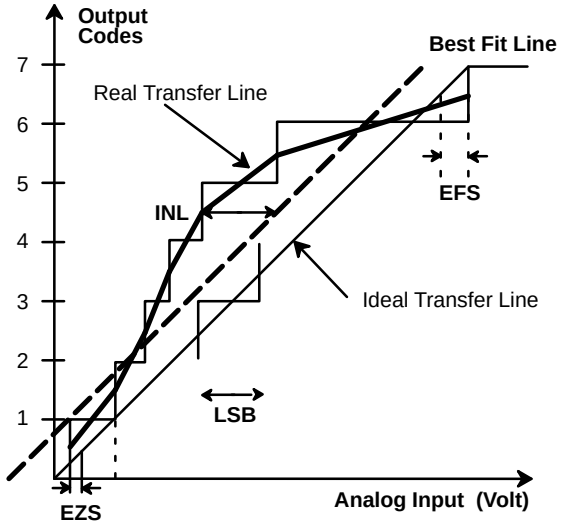


Figure 4. INL Error Calculation

APPLICATION NOTES

V_{IN} signals should not exceed AV_{DD} +0.5V or go below AGND –0.5V. All pins have internal protection diodes that will protect them from short transients (<100µs) outside the supply range.

AGND and DGND pins are connected internally through the P– substrate. DC voltage differences between these pins will cause undesirable internal substrate currents.

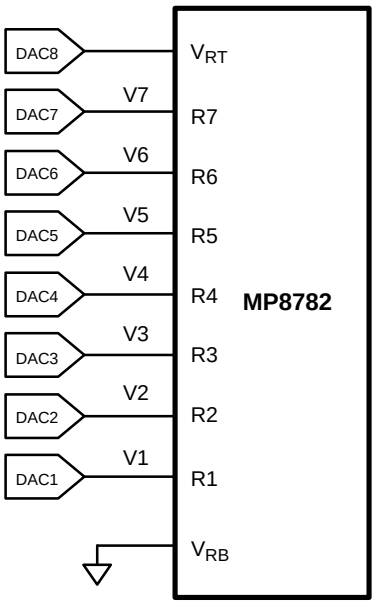
The power supply (AV_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to AGND, placed as close to the chip as possible.

The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

The application resistors, RTS and RBS allow for applied voltages in the range of AV_{DD} + 5 V to AGND – 5V. If the internal reference pins V_{RTS} and/or V_{RBS} are not used they should be left unconnected.

The reference tap pins (R1-R7) should be decoupled with 0.1µF to 1µF capacitors. This will help stabilize the internal reference voltages thus reducing any INL errors.

The reference tap pins (R1-R7) can be used to create piecewise-linear transfer functions. By forcing custom voltages on these pins, an eight segment transfer function can be made. See *Figure 5. and Figure 6.*



DAC MP7228

Only the Ladder detail shown.

Figure 5. A/D with Programmed Ladder Control for Creating a Piecewise Linear Transfer Function

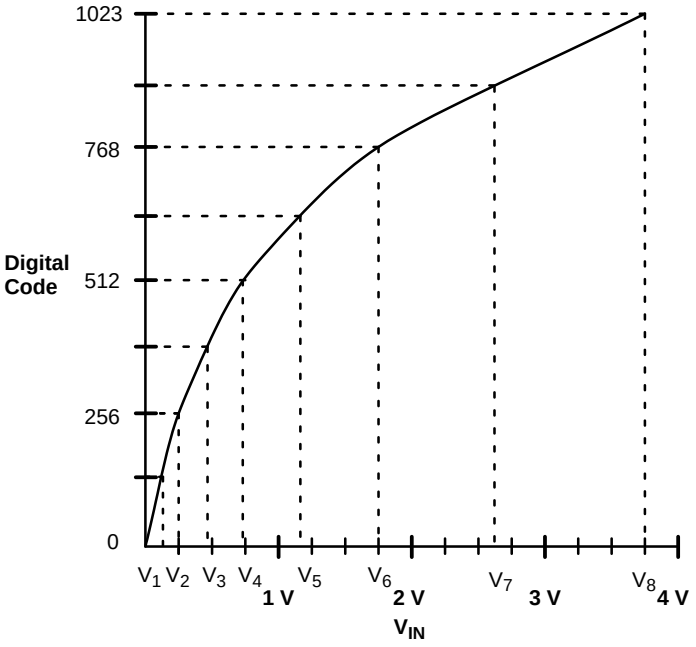


Figure 6. A Piecewise Linear, Logarithmic Transfer Function

OPTIONS on the 8782 DIE & OPERATION NOTES:

OFW & UFW Overflow & Underflow (outputs)

These signals indicate when the Analog Input (V_{IN}) goes outside the V_{RB} to V_{RT} range. Both pins are normally at low logic levels. When $V_{IN} > V_{RT}$, OFW will go high and the data bits (DB0 – DB9) will show full scale (i.e. all 1s if MINV & LINV are low). When $V_{IN} < V_{RB}$, UFW will go high and the data bits will show negative full scale (i.e. all 0s if MINV & LINV are low).

$\overline{OE1}$ & OE2 Output Enable (inputs)

These signals control the 3-state drivers on the digital outputs DB0 – DB9, OFW and UFW. During normal operation $\overline{OE1}$ should be held low and OE2 should be held high so that all outputs are enabled (NOTE: internal resistors will pull $\overline{OE1}$ and OE2 to these levels if they are not connected). When $\overline{OE1}$ is driven high DB0 – DB9 go into high impedance mode. When OE2 is driven low DB0 – DB9, OFW and UFW all go into high impedance mode (please refer to the truth table below). These controls operate asynchronous to the clock and they only control the output drivers. The internal output register will get updated if the clock is running while the outputs are in 3-state mode.

$\overline{OE1}$	OE2	DBO-DB9	OFW & UFW
0	1	enabled	enabled
1	1	3-state	enabled
X	0	3-state	3-state

PHASE Clock Polarity Control (input)

This signal controls the phase relationship between the signal applied at the CLK pin and the internal clock signals. When PHASE is high, V_{IN} is sampled at the high to low CLK transition and the digital data changes after a low to high CLK transition. When PHASE is low, V_{IN} is sampled at the low to high CLK transition and the digital data changes after a high to low CLK transition. See timing diagram *Figure 7.* PHASE has an internal pull up device.

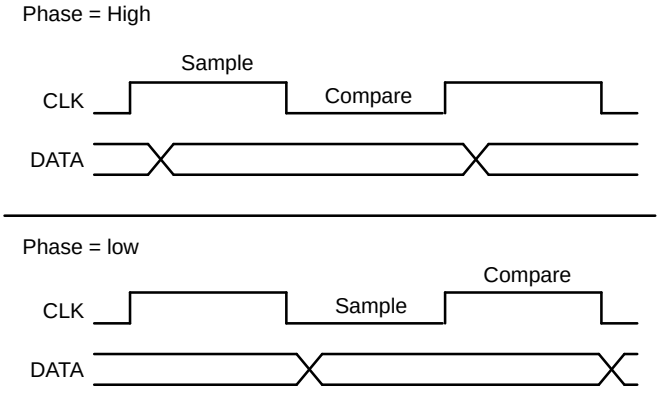


Figure 7. Clock Phase Relationship

APERTURE Aperture Delay Sync (output)

This signal is high when the internal sample/hold function is sampling V_{IN}, and goes low when it is in the hold mode (when the ADC is comparing the stored input value to the reference ladder). The value of V_{IN} at the high to low transition of APERTURE is the value that will be digitized. A system can monitor this signal and adjust the CLK to accurately synchronize the sampling point to an external event.

V_{IN} Analog Input

This part has a switched capacitor type input circuit. This means that the input impedance changes with the phase of the input clock. V_{IN} is sampled at the high to low clock transition and the digital data changes at the low to high clock transition. The diagram *Figure 8.* shows an equivalent input circuit.

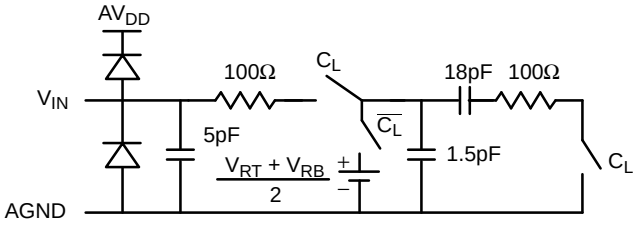


Figure 8. Equivalent Input Circuit

MINV & LINV Digital Output Format (inputs)

These signals control the format of the digital output data bits DB0 – DB9 (*see Table 1.)* Normally both pins are held low so the data is in straight binary format (all 0s when $V_{IN}=V_{RB}$; all 1s when $V_{IN}=V_{RT}$). If MINV is pulled high, then the MSB (DB9) will be inverted. If LINV is pulled high, then the LSB's (DB0 – DB8) will be inverted. The OFW and UFW bits are not affected by these signals.

MINV LINV	0 0	0 1	1 0	1 1
V_{RT}	111 . . . 11 111 . . . 10	100 . . . 00 100 . . . 01	011 . . . 11 011 . . . 10	000 . . . 00 000 . . . 01
V_{IN} mid scale	100 . . . 01 100 . . . 00	111 . . . 10 111 . . . 11	000 . . . 01 000 . . . 00	011 . . . 10 011 . . . 11
	011 . . . 11	000 . . . 00	111 . . . 11	100 . . . 00
V_{RB}	000 . . . 01 000 . . . 00	011 . . . 10 011 . . . 11	100 . . . 01 100 . . . 00	111 . . . 10 111 . . . 11
	binary	inverted 2's complement	2's complement	inverted binary

Table 1. Output Data Format Truth Table

MINV & LINV are meant to be static digital signals. If they are to change during operation, they should only change when the CLK is low (assuming PHASE is high, if PHASE is low then these signals should only change when CLK is high). Changing MINV and/or LINV on the wrong phase of the CLK will not hurt anything, but the effects on the digital outputs will not be seen until the output latch of the output register is enabled. See the simplified logic circuit *Figure 9.* MINV and LINV have internal pull down devices.

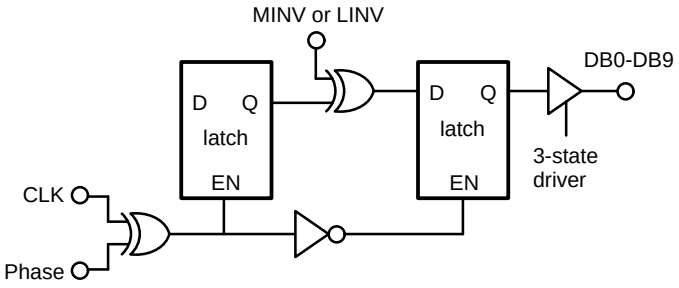


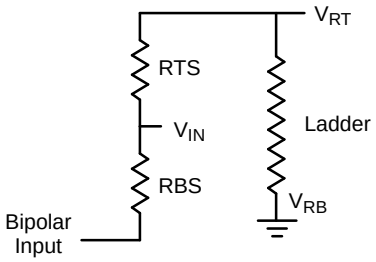
Figure 9. MINV, LINV Simplified Logic Circuit

RTS & RBS Internal Bias Resistors

Two matched resistors are provided on the chip. These resistors can be used to generate on chip reference voltages, or to extend the analog input range. Each resistor has a value equal to 1/3 of the reference ladder resistor.

By connecting RTS between AV_{DD} (5 volts) and V_{RT}, and connecting RBS between AGND and V_{RB}, the reference ladder will be biased to 1 volt at V_{RB} and 4 volts at V_{RT}.

A bipolar input range (+V_{RT} to –V_{RT}) can be achieved by connecting RTS and RBS as shown in *Figure 10. (a) and (b)*, and fixing V_{RT} with a positive reference voltage. Due to current density limitations for RTS and RBS, V_{RT} should be limited to +1.4 volts in this configuration. The protection pads used for the resistor terminals are designed to allow voltages that go beyond the supply rails.



(a) Bipolar Input Configuration

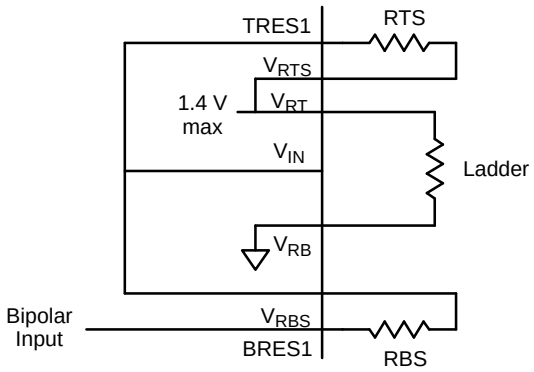
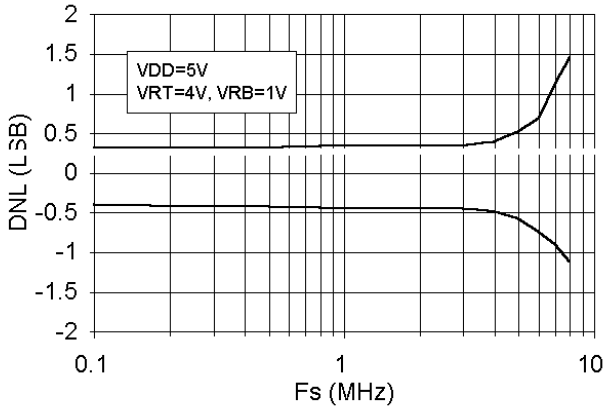


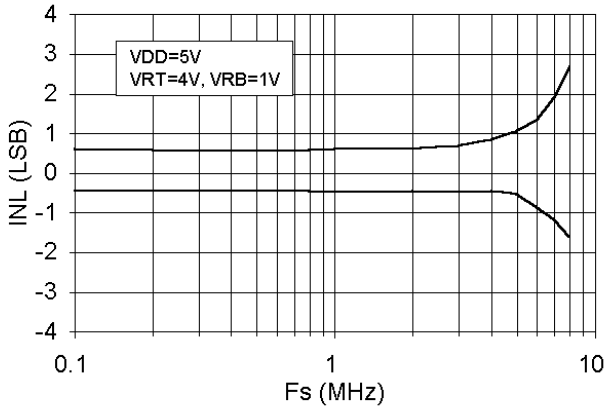
Figure 10. (b) Bipolar Input Connections

R1 thru R7 Reference Ladder Taps. These taps connect to every eighth point along the reference ladder; R1 is 1/8th up from V_{RB}, R7 is 7/8ths up from V_{RB} (or 1/8th down from V_{RT}). Normally these pins should have 0.1 µF capacitors to AGND, this helps reduce the INL errors by stabilizing the reference ladder voltages. These taps can also be used to alter the transfer curve of the ADC. An eight segment, piecewise linear, custom transfer curve can be designed by connecting voltage sources to these pins.

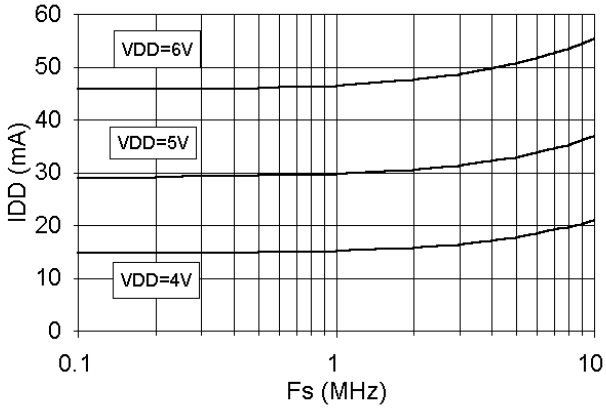
PERFORMANCE CHARACTERISTICS



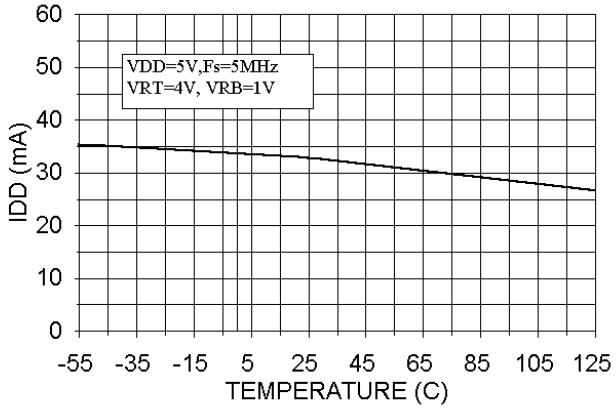
Graph 1. DNL vs. Sampling Frequency



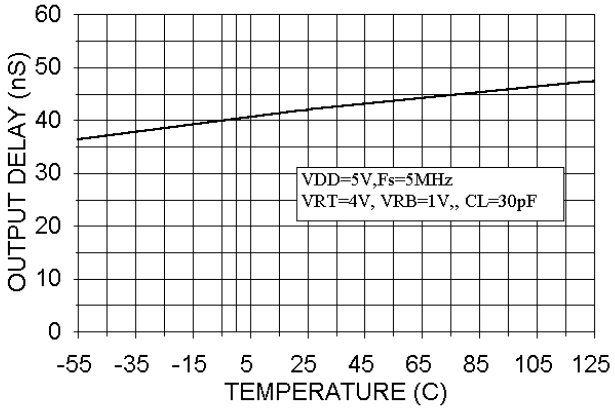
Graph 2. INL vs. Sampling Frequency



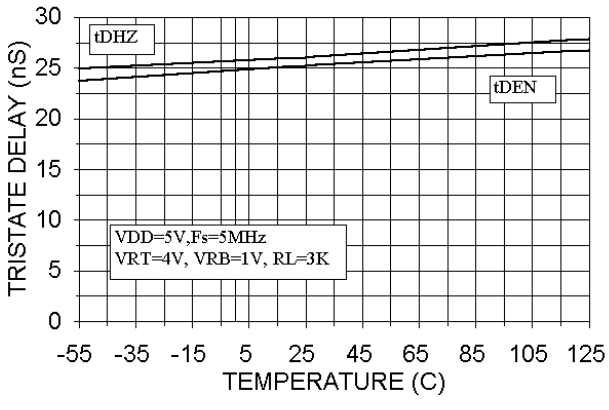
Graph 3. Power Supply Current vs. Sampling Frequency



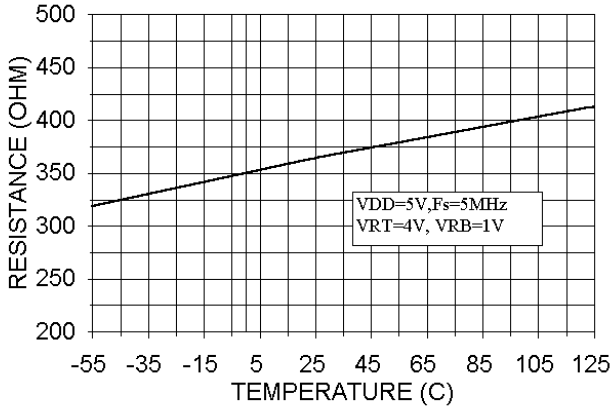
Graph 4. Power Supply Current vs. Temperature



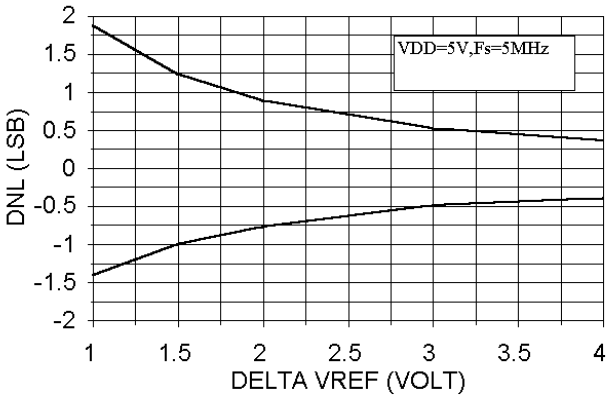
Graph 5. Output Delay vs. Temperature



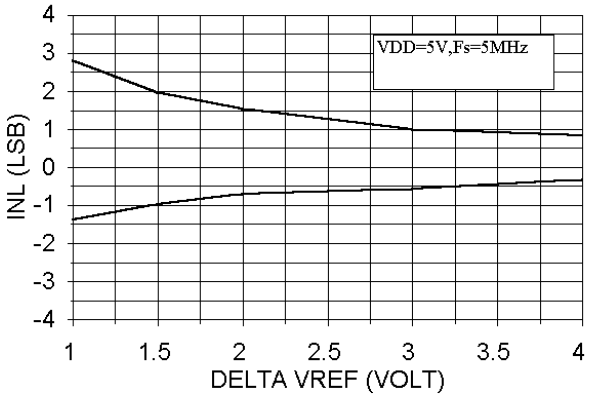
Graph 6. 3-state Delay vs. Temperature



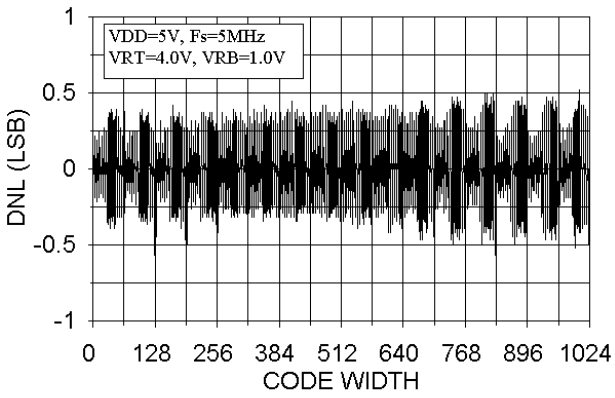
Graph 7. Reference Resistance vs. Temperature



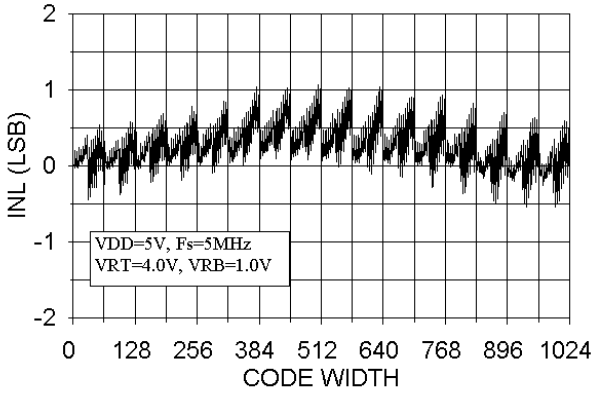
Graph 8. DNL vs. ΔV_{REF}



Graph 9. DNL vs. ΔV_{REF}

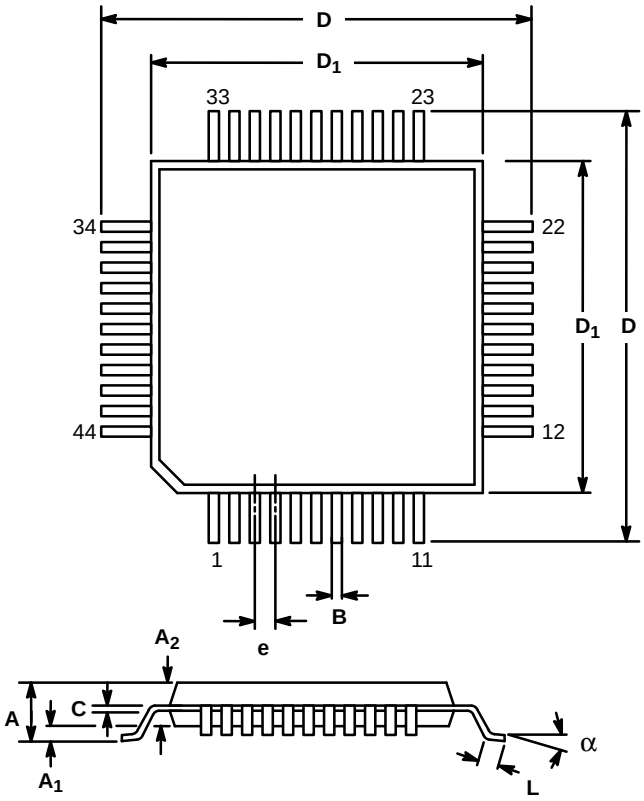


Graph 10. DNL Error Plot



Graph 11. INL Error Plot

44 LEAD PLASTIC QUAD FLAT PACK
(14mm x 14mm PQFP, METRIC)
Q44



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	3.15	—	0.124
A_1	0.25	—	0.01	—
A_2	2.6	2.8	0.102	0.110
B	0.3	0.4	0.012	0.016
C	0.13	0.23	0.005	0.009
D	16.95	17.45	0.667	0.687
D_1	13.9	14.1	0.547	0.555
e	1.00 BSC		0.039 BSC	
L	0.65	1.03	0.026	0.040
α	0°	7°	0°	7°
Coplanarity = 4 mil max.				

Notes

Notes

Notes

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contains here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Datasheet April 1995