MP8776

CMOS
8-Bit High Speed, Low Power
Analog-to-Digital Converter with Power Down

FEATURES

- **8-Bit Resolution**
- **Sampling Rate to 30 MHz**
- **Low Power: 110 mW typ. (excluding reference)**
- **Power Down Mode: 100μA (typ)**
- **DNL = ±1/4 LSB, INL = ±1/2 LSB (typ)**
- **Internal S/H Function**
- **Single Supply: 5 V**
- **V_{IN} Range: 0 V to V_{DD}**
- **V_{REF} Range: 1 V to V_{DD}**
- **Latch-Up Tolerant**
- **ESD Protection: 2000 V Minimum**
- **3 State Digital Outputs**
- **20 Pin PDIP, SOIC and SSOP Packages**
- **24 Pin Package Available: MP8786**
- **3 V Version: MP87L76**
- **Improved Version of MP8775**

APPLICATIONS

- **Wireless Communications**
- **Digital Cellular Telephones**
- **Telecommunications**
- **CCD's and Scanners**
- **Video Boards**
- **Digital Color Copiers**
- **Battery Powered Devices**

GENERAL DESCRIPTION

The MP8776 is an 8-bit Analog-to-Digital Converter designed for high speed digitizing applications requiring low power. The MP8776 offers exceptional performance, flexible input architecture, low power consumption, power down capability, latch-up tolerant operation and is manufactured using an advanced 5 volt CMOS process.

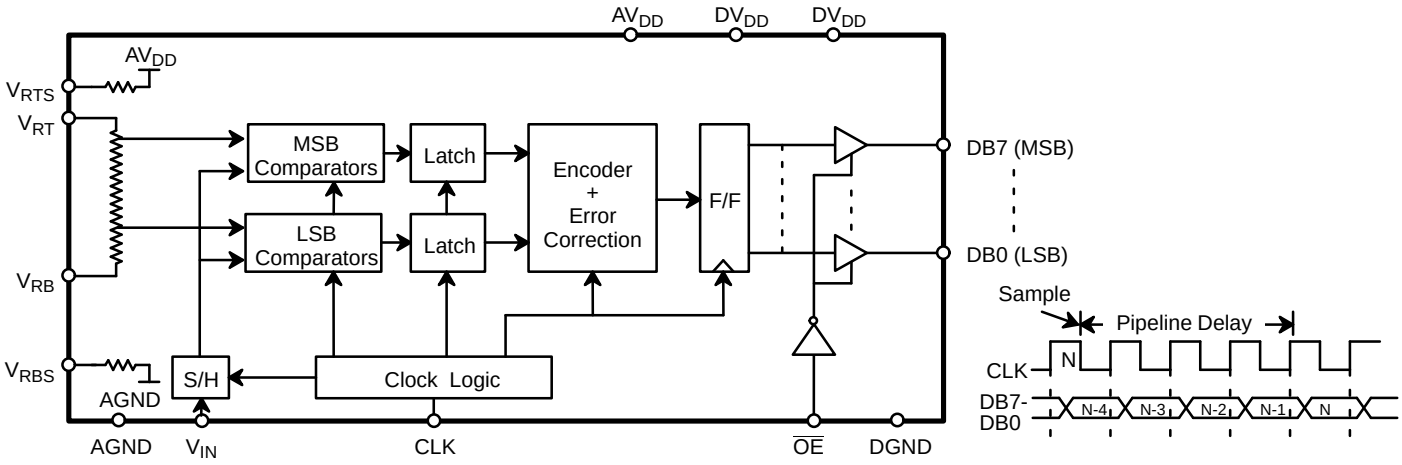
This device uses a two-step flash architecture to maintain low power consumption at high conversion rates. The input circuitry of the MP8776 includes an on-chip S/H function and allows the user to digitize analog input signals between GND and V_{DD}. Careful design and chip layout have achieved a low analog input capacitance. This reduces "kickback" and eases the requirements of the buffer/amplifier used to drive the MP8776.

The designer can choose the internally generated reference voltages by connecting V_{RB} to V_{RBS} and V_{RT} to V_{RTS}, or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 0.6 V at V_{RB} and 2.6 V at V_{RT}. Providing external reference voltages allows easy interface to any input signal range between GND and V_{DD}. This also allows the system to adjust these voltages to cancel zero scale and full scale errors, or to change the input range as needed.

The device operates from a single +5 volt supply. Power consumption is 110 mW (typ) at FS = 20 MHz. Power down is accomplished by dropping V_{RT} below 0.55 V.

Specified for operation over the commercial / industrial (–40 to +85°C) temperature range, the MP8776 is available in surface mount (SOIC), shrink small outline (SSOP) and plastic dual-in-line (PDIP) packages.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

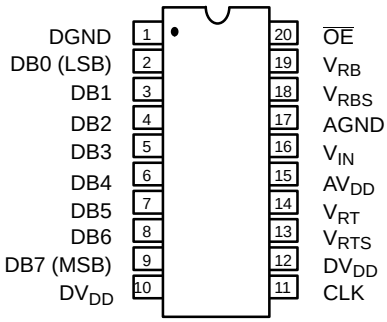


ORDERING INFORMATION

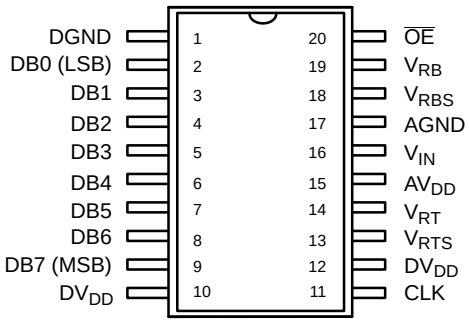
Package Type	Temperature Range	Part No.
SOIC	–40 to +85°C	MP8776AS
PDIP	–40 to +85°C	MP8776AN
SSOP	–40 to +85°C	MP8776AQ

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



20 Pin PDIP (0.300”)
N20



20 Pin SOIC (Jedec, 0.300”) – S20
20 Pin SSOP – A20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DGND	Digital Ground
2	DB0	Data Output Bit 0 (LSB)
3	DB1	Data Output Bit 1
4	DB2	Data Output Bit 2
5	DB3	Data Output Bit 3
6	DB4	Data Output Bit 4
7	DB5	Data Output Bit 5
8	DB6	Data Output Bit 6
9	DB7	Data Output Bit 7 (MSB)
10	DV_{DD}	Digital Power Supply

PIN NO.	NAME	DESCRIPTION
11	CLK	Sample Clock
12	DV_{DD}	Digital Power Supply
13	V_{RTS}	Generates 2.6 V if tied to V_{RT}
14	V_{RT}	Top Reference
15	AV_{DD}	Analog Power Supply
16	V_{IN}	Analog Input
17	AGND	Analog Ground
18	V_{RBS}	Generates 0.6 V if tied to V_{RB}
19	V_{RB}	Bottom Reference
20	$\overline{OE}$	Output Enable

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, FS = 20 MHz (50% Duty Cycle), V_{RT} = 2.6 V, V_{RB} = 0.6 V, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		8			Bits	
Sampling Rate	FS	0.01		20	MHz	For specified performance
	FS			30	MHz	
ACCURACY[1]						
Differential Non-Linearity	DNL		±1/4	±1/2	LSB	
Integral Non-Linearity	INL		±1/2	1	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		±35		mV	
Full Scale Error	EFS		±35		mV	
REFERENCE VOLTAGES						
Positive Ref. Voltage	V_{RT}		2.6	AV_{DD}	V	
Negative Ref. Voltage	V_{RB}	AGND	0.6		V	
Differential Ref. Voltage[3]	V_{REF}	1.0		AV_{DD}	V	$V_{REF} = V_{RT} – V_{RB}$
Ladder Resistance	R_L	245	350	455	Ω	
Ladder Temp. Coefficient	R_{TCO}		2000		ppm/°C	
Self Bias 1	V_{RB}		0.6		V	Short V_{RB} to V_{RBS} and V_{RT} to V_{RTS}
	V_{REF}		2		V	Short V_{RB} to V_{RBS} and V_{RT} to V_{RTS}
Self Bias 2	V_{RT}		2.3		V	V_{RB} = AGND, Short V_{RT} and V_{RTS}
ANALOG INPUT[2]						
Bandwidth (–1 dB)[4]	BW		14		MHz	
Input Voltage Range	V_{IN}	0		AV_{DD}	V	
Input Capacitance Sample[5]	C_{IN}		22		pF	Clock High
Input Capacitance Convert[5]	C_{IN}		7		pF	Clock Low
Aperture Delay	t_{AP}		10		ns	
Aperture Jitter	t_{AJ}		30		ps	
DYNAMIC PERFORMANCE						F_{IN} = 1 MHz
Signal to Noise Ratio	SNR		46		dB	
Signal to Noise plus Distortion	SINAD		42		dB	
Harmonic Distortion	THD		–46		dB	
Effective No. of Bits	ENOB		6.8		Bits	
DIGITAL INPUTS						
Logical “1” Voltage	V_{IH}	3.5			V	
Logical “0” Voltage	V_{IL}			1.5	V	
DC Leakage Currents[6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK			5		µA	
$\overline{OE}$			5		µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 6.*)[7]						
Clock Period	1/FS	50			ns	For Specified Performance
High Pulse Width	t_{PWH}	25			ns	For Specified Performance
Low Pulse Width	t_{PWL}	25			ns	For Specified Performance

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	4.5			V	I_{LOAD} = 4 mA
Logical "0" Voltage	V_{OL}			0.4	V	I_{LOAD} = 4 mA
3-state Leakage	I_{OZ}		10		µA	V_{OUT}=GND to DV_{DD}
Data Valid Delay[2, 8]	t_{DL}		20		ns	
Data Enable Delay[2, 8]	t_{DEN}		20	25	ns	
Data 3-state Delay[2, 8]	t_{DHZ}		12	15	ns	
Pipeline Delay				3.5	clock cycles	Constant relationship between clock and output
POWER SUPPLIES						
Operating Voltage (AV_{DD}, DV_{DD})[9]	V_{DD}		5		V	
Current (AV_{DD} + DV_{DD})	I_{DD}		22	35	mA	Does not include ref. current
POWER DOWN						
Power Down Point	V_{RTPD}	0.4	0.55		V	Chip goes to power down mode
Power Up Point				0.9	V	when V_{RT} < 0.55 V
Power Down Current	I_{DDPD}			100	µA	Does not include ref. current
Power Control Delay	PDD			200	ns	V_{RT} @ 0.4→0.9 V

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (*Figure 10.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 11.*) Accuracy is a function of the sampling rate (FS).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 The bandwidth represents the gain of the ADC and does not imply accuracy

5 See V_{IN} input equivalent circuit (*Figure 2.*). Switched capacitor analog input requires driver with low output resistance.

6 All inputs have diodes to V_{DD} and GND. Input DC currents will not exceed specified limits for any input voltage between GND and V_{DD}.

7 t_R, t_F should be limited to >5 ns for best results.

8 Depends on the RC load connected to the output pin.

9 AGND and DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted) [1, 2, 3]

V_{DD} to GND ..... 7 V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND –0.5 V
V_{IN} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
All Outputs ..... V_{DD} +0.5 to GND –0.5 V
Storage Temperature ..... –65 to +150°C

Lead Temperature (Soldering 10 seconds) ..... 300°C
Maximum Junction Temperature ..... 150°C
Package Power Dissipation Rating @ 75°C
SOIC, PDIP, SSOP ..... 680 mW
Derates above 75°C ..... 9 mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

THEORY OF OPERATION

Analog to Digital Conversion

The MP8776 uses a two step, sub-ranging architecture to convert analog voltages into 256 digital codes.

A full conversion (sampling V_{IN}, converting MSB & LSB, and performing any error correction) requires 3 1/2 clock cycles to complete (*see Figure 6.*) The pipelined architecture allows the chip to maintain a one conversion per cycle sample rate. Digital logic combines the MSB and LSB data and performs error correction to produce 8-bit output codes.

Internal Reference Bias

The MP8776 includes two on-chip resistors that can be used to bias the reference ladder without external circuitry. These two resistors are designed to track the reference ladder and are used to create a voltage divider between the supplies (AV_{DD} and AGND).

To use this feature, simply connect V_{RT} to V_{RTS} and connect V_{RB} to V_{RBS}. This will nominally generate:

AV_{DD} x (0.3/2.5) at V_{RB}, and

AV_{DD} x (1.3/2.5) at V_{RT}

This will generate 0.6 V at V_{RB} and 2.6 V at V_{RT} (see *Figure 1.)* Bypass capacitors on V_{RT} and V_{RB} are suggested to stabilize the ladder.

If the internal reference pins V_{RTS} and/or V_{RBS} are not used they should be left unconnected.

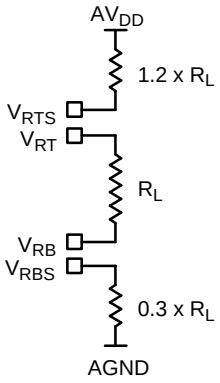


Figure 1. Internal Reference Bias

Transfer Characteristics

The ideal ADC is a linear building block that has infinite bandwidth and no phase distortion. A real ADC, however, exhibits finite bandwidth and non-constant group delay characteristics as well as non-linear behavior due to the non-zero INL characteristic. When modeling the ADC as a linear element and a quantizer, the circuit shown in *Figure 2.* can be used in order to represent the ADC's bandwidth.

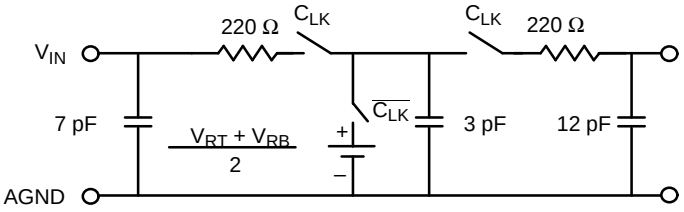


Figure 2. Input Equivalent Circuit

Sample and Hold Timing

The ADC's internal sample and hold tracks the input signal when CLK is high. After a delay of t_{AP} from the falling clock edge, the analog signal is sampled and held for conversion as seen in *Figure 3.*

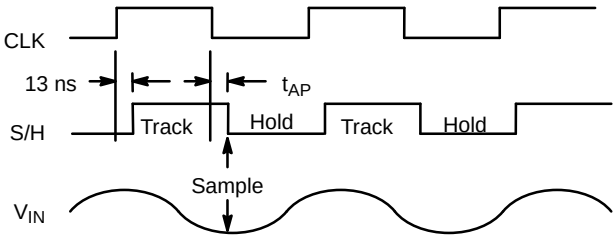


Figure 3. Sample and Hold Timing

Output Enable ($\overline{OE}$)

The $\overline{OE}$ pin controls the state of the digital output drivers. When forced low, the drivers are active. When pulled high the drivers are 3-stated. Please note that the $\overline{OE}$ pin only controls the output drivers; the rest of the chip is still active. Therefore if the clock is running, the internal registers are updated even if the digital outputs are 3-stated (*Figure 4.*).

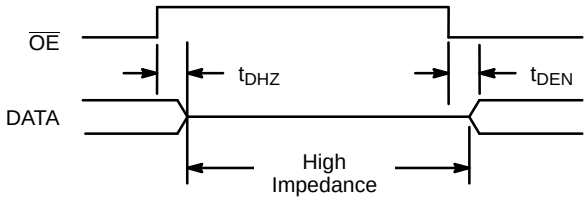


Figure 4. Output Enable/Disable Timing Diagram

Power Down Mode

For systems that are battery powered, the MP8776 has a power down feature to help extend battery life. When the voltage at the V_{RT} pin drops below 0.4 V, the chip goes into power down mode. In this state, conversions are halted, the outputs are 3-stated and I_{DD} drops to less than 100 µA. Then, when the voltage at the V_{RT} pin rises above 0.9 V, the chip will power up. Note that after power up, four clock cycles are required to get valid data at the digital outputs (see *Figure 6.*). One way to achieve power down is to disconnect or disable the buffer/amp driving V_{RT}, and let the internal reference resistance pull V_{RT} down. Remember, any bypass capacitors at V_{RT} will increase the time for V_{RT} to drop below 0.4 V.

APPLICATION NOTES

Power Supplies and Grounding

AV_{DD} and DV_{DD} should be connected to the sample power supply source (*Figure 5.*). The power supply (AV_{DD} and DV_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to GND, placed as close to the chip as possible.

AGND and DGND pins are connected internally through the P-substrate. AGND and DGND pins should be connected together as close to the chip as possible.

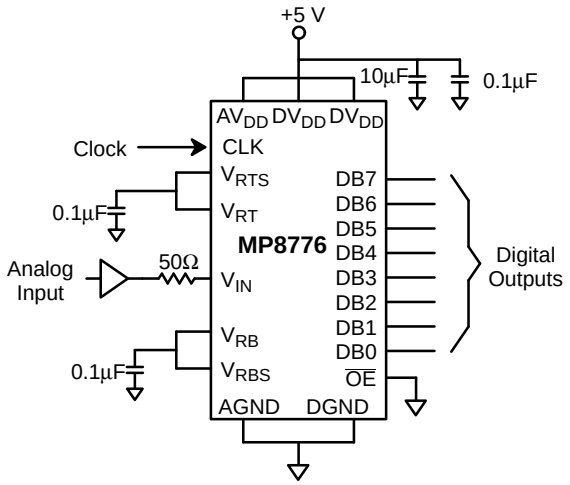


Figure 5. Typical Circuit Connections

The Analog Input

When designing with the MP8776, the following points can help optimize performance.

1. Driving the analog input – The input impedance can be represented as a switched capacitor type input circuit, ie. the input impedance changes with the phase of the input clock. *Figure 2.* shows an equivalent input circuit. In many applications, the input impedance can be treated as capacitive. For fast signals and a high driving impedance, a wide bandwidth op amp is recommended.
2. It is important to note that op amps have inductive output impedances at high frequencies which is a consequence of the emitter impedance of the typical push-pull output stage. The resulting transient ringing should be damped by inserting a resistor in series with the ADC input – typically about 50Ω. See *Figure 5.* The exact value may be obtained from the op amp manufacturer's data sheet.
3. Signals should not exceed V_{DD} +0.5V or go below GND –0.5V. All pins have internal protection diodes that will protect them from short transients (*See Note 2, Absolute Maximum Ratings*) outside the supply range.

Digital Outputs

Refer to *Figure 6.* for details on the data availability timing. The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion. The output enable pin ($\overline{OE}$) should not be left unconnected. If it is not controlled by an active signal, it must be tied to ground.

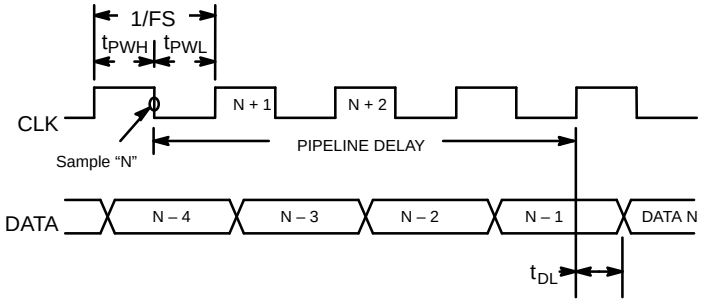


Figure 6. Data Available Timing

Dynamic Reference Control

The MP8776 allows for dynamically adjusted V_{RT} and V_{RB}. When this is done, V_{RT} and V_{RB} have to be kept static during a certain period.

The A/D conversion is done in a two-step method. During the first clock period, the MSB comparator bank compares the V_{IN} with the reference voltage string in order to determine in which subrange the exact V_{IN} lies. During the subsequent clock period, an LSB comparator bank compares a subrange of the V_{REF} to the V_{IN}. Thus, the reference inputs have to be stable during two compare cycles. This implies that while the ADC is clocked with FS, the conversion only occurs at a rate of FS/2. Every second sample and resulting data must be discarded because the reference changes during its conversion.

The reference inputs V_{RT} and V_{RB} have to have settled to within 1 LSB, at least 50 ns before the rising edge which occurs after the sampling instant. The reference has to be kept constant until (t_{AP} + 10 ns) after the second rising edge. See *Figure 7.* for timing details. The digital data of the N + 1, N +3, N + 5 etc. samples are invalid if the reference is changed every second clock cycle. The data for the N, N + 2, N + 4 etc. samples are valid.

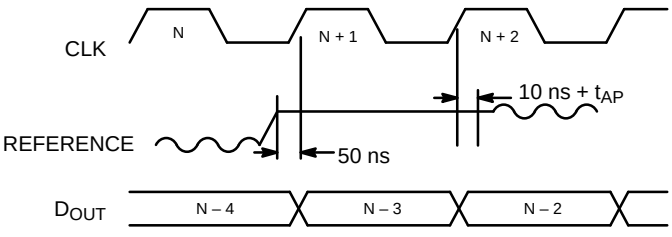


Figure 7. Dynamic Reference Control

LINEARITY DEFINITION

The Ideal ADC

The transfer function for an ideal A/D converter is shown in *Figure 8.*

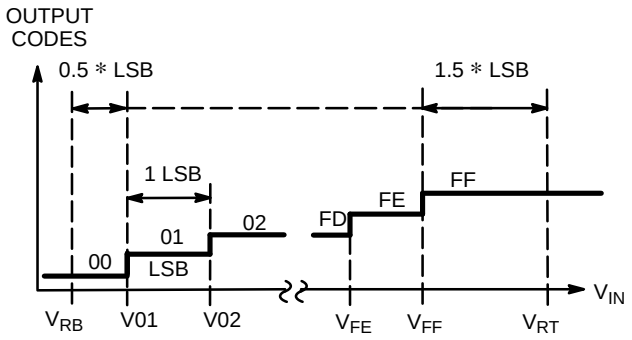


Figure 8. Ideal A/D Transfer Function

The first transition for the data bits takes place when:

$V_{IN} = V01 = V_{RB} + 0.5 * LSB$

The last transition of the data bits takes place when:

$V_{IN} = V_{FF} = V_{RT} – 1.5 * LSB$

where: $LSB = V_{REF} / 256$

$= (V_{FF} – V01) / 254$

and $V_{REF} = (V_{RT} – V_{RB})$

The Real ADC

In a “real” converter, the code-to-code transitions do not fall exactly every $V_{REF}/256$ volts.

A positive DNL (Differential Non Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSBs.

A specification of Max DNL = $\pm$ 0.5 LSB means that all codes are within 0.5 LSB and 1.5 LSB. For example, if V_{REF} = 4.096 V then 1 LSB = 16mV and every code width is between 8 and 24 mV.

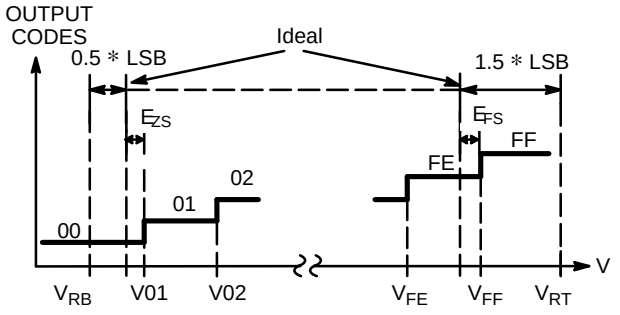


Figure 9. Real A/D Transfer Curve

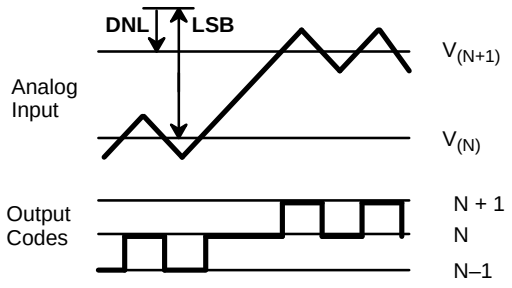


Figure 10. DNL Measurement

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) are:

DNL (01) = V02 – V01 – LSB

: : :

DNL (FE) = $V_{FF} – V_{FE}$ – LSB

Thus $DNL_{(N)} = [V_{(N+1)} – V_{(N)}] – LSB$

Code Width (N) = $V_{(N+1)} – V_{(N)}$

Similarly, the zero scale and full scale errors are defined as:

EFS (full scale error) = $V_{FF} – (V_{RT} – 1.5 * LSB)$

EZS (zero scale error) = $V01 – (V_{RB} + 0.5 * LSB)$

where: $LSB = [V_{RT} – V_{RB}] / 256$

Figure 9. shows the zero scale and full scale error terms while *Figure 10.* shows the definition of DNL.

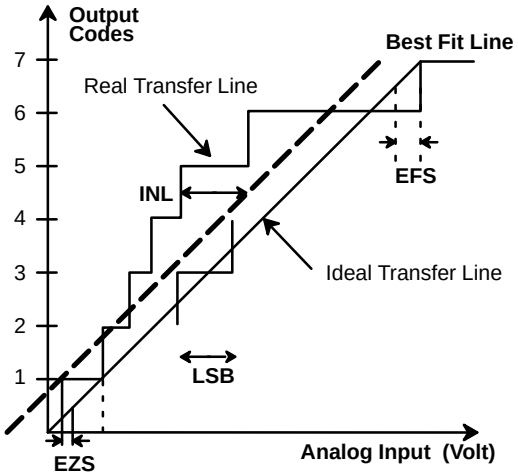
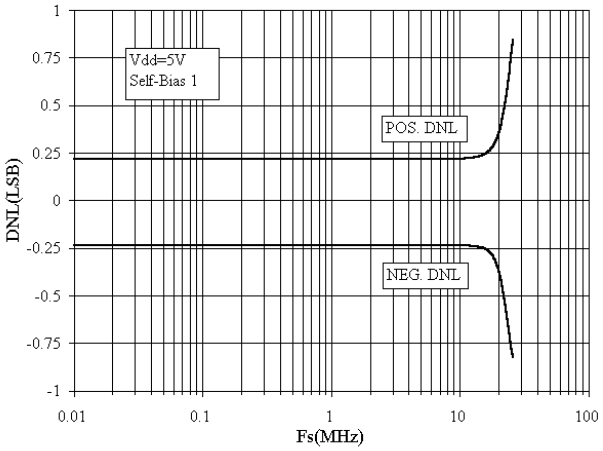


Figure 11. INL Error Calculation (3-Bit)

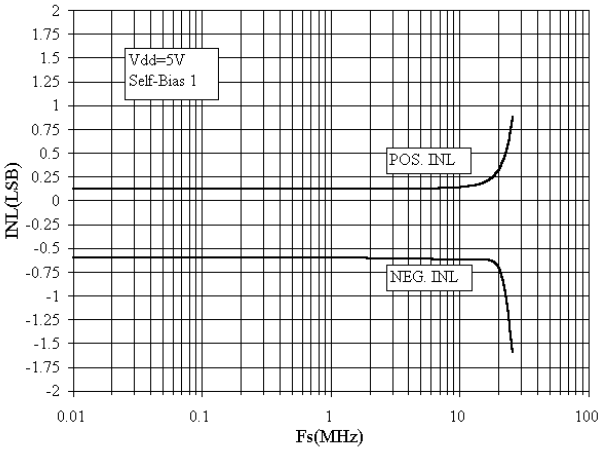
Figure 11. gives a visual definition of the INL error. The graph shows a 3-bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, a line is drawn parallel to the ideal transfer line. By definition, the best fit line makes equal the positive and the negative INL errors. This may change an INL of –1 to +2 LSBs relative to the ideal line into a $\pm$1.5 relative to the best fit line.

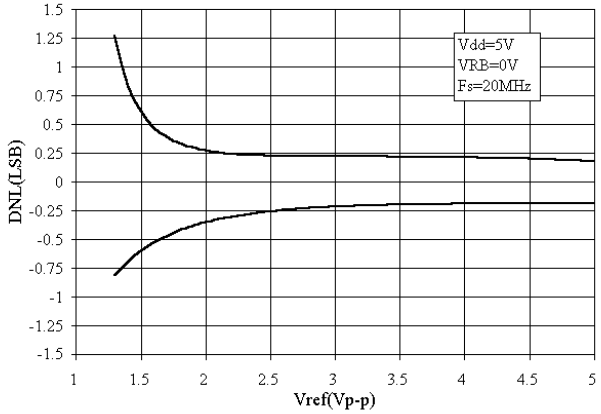
PERFORMANCE CHARACTERISTICS



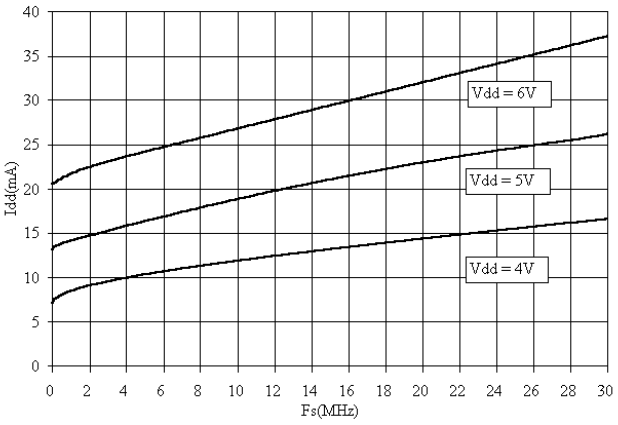
Graph 1. DNL vs. Sampling Frequency



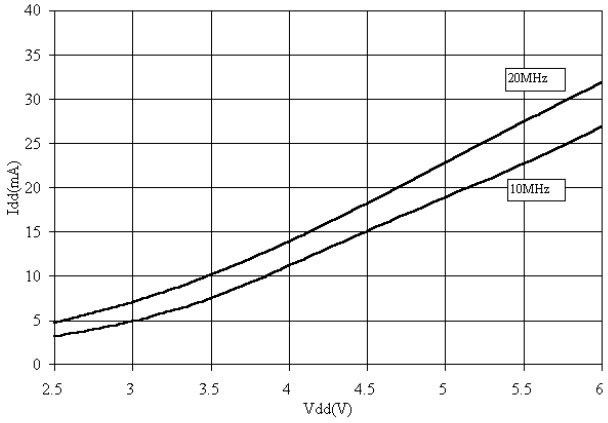
Graph 2. INL vs. Sampling Frequency



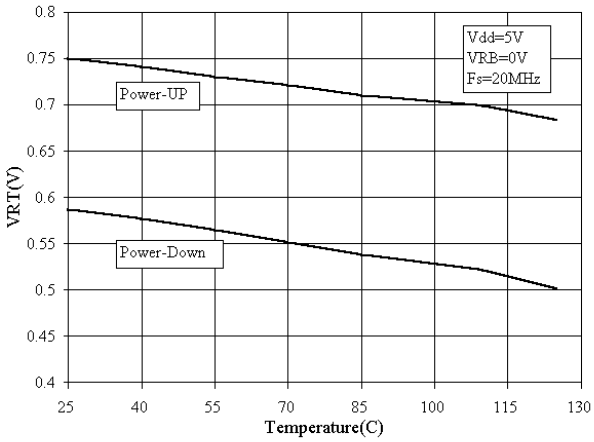
Graph 3. DNL vs. Reference Voltage



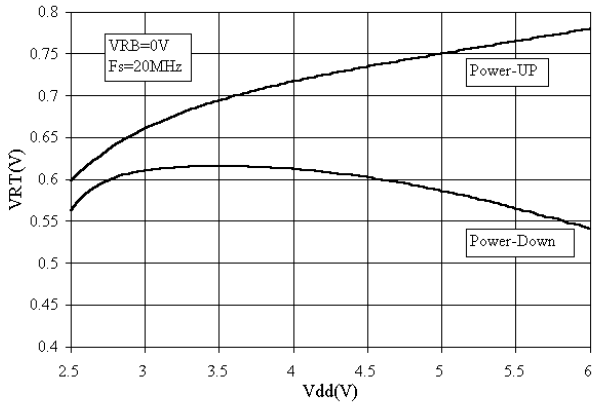
Graph 4. Supply Current vs. Sampling Frequency



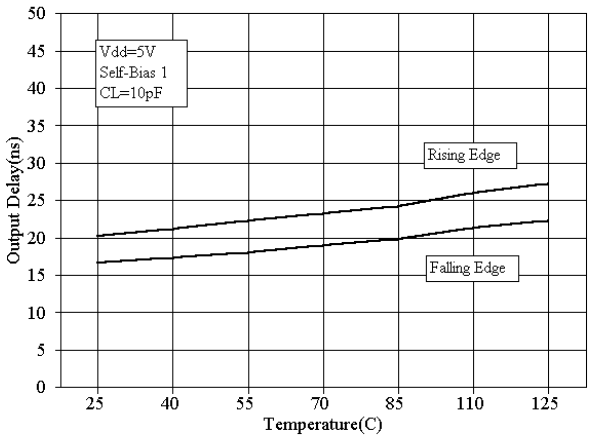
Graph 5. Supply Current vs. Supply Voltage



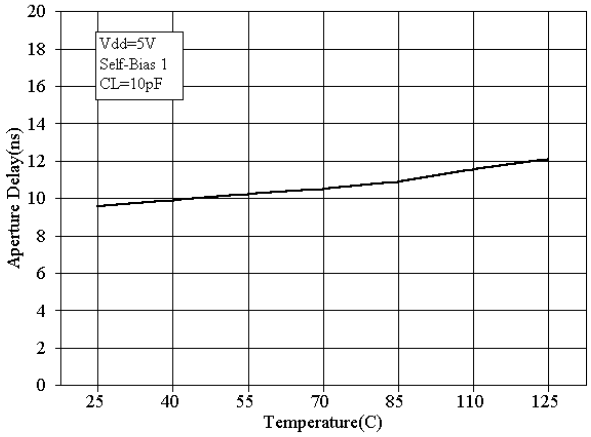
Graph 6. Power Up/Down Voltage vs. Temperature



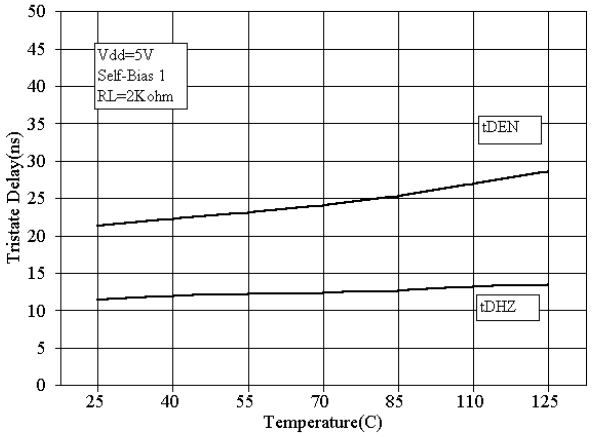
Graph 7. Power Up/Down Voltage vs. Supply Voltage



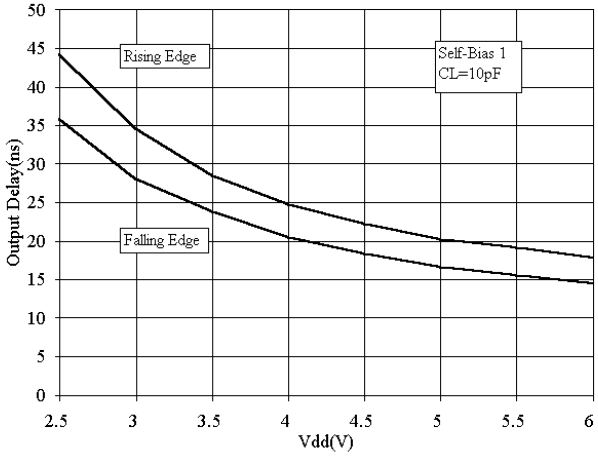
Graph 8. Output Delay (t_{DL}) vs. Temperature



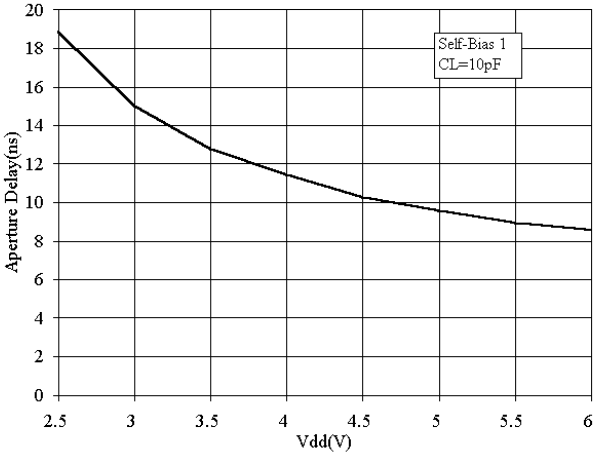
Graph 9. Aperture Delay (t_{AP}) vs. Temperature



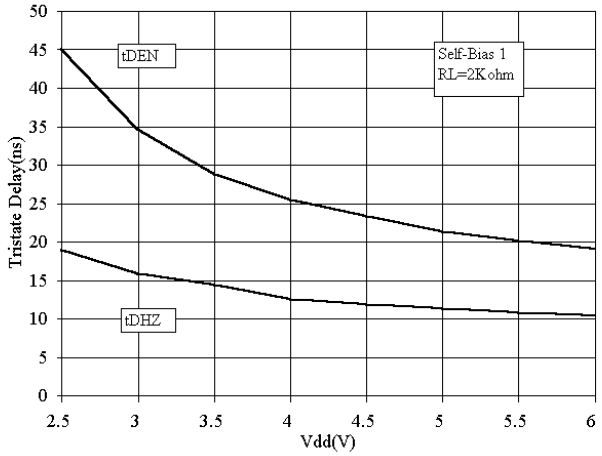
Graph 10. 3-state/Enable Delay vs. Temperature



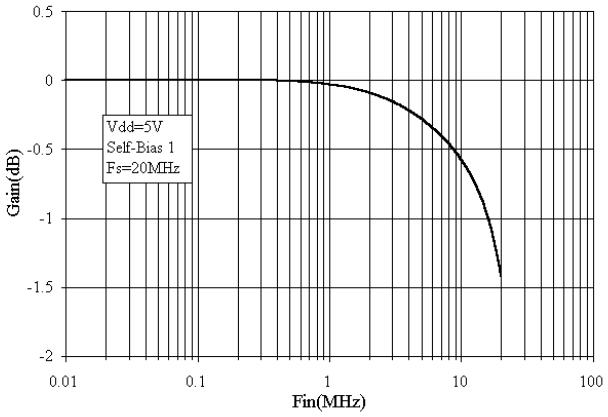
Graph 11. Output Delay vs. Supply Voltage



Graph 12. Aperture Delay (t_{DL}) vs. Supply Voltage

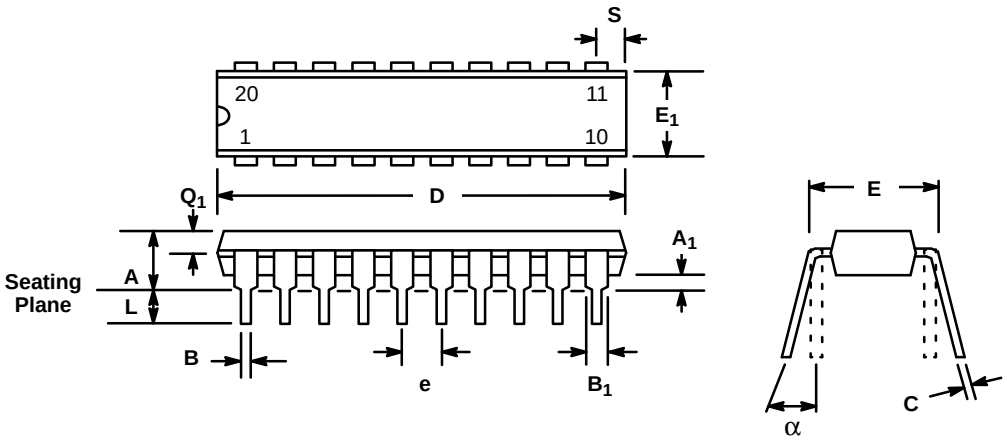


Graph 13. 3-state/Enable Delay vs. Supply Voltage



Graph 14. Gain vs. Input Frequency

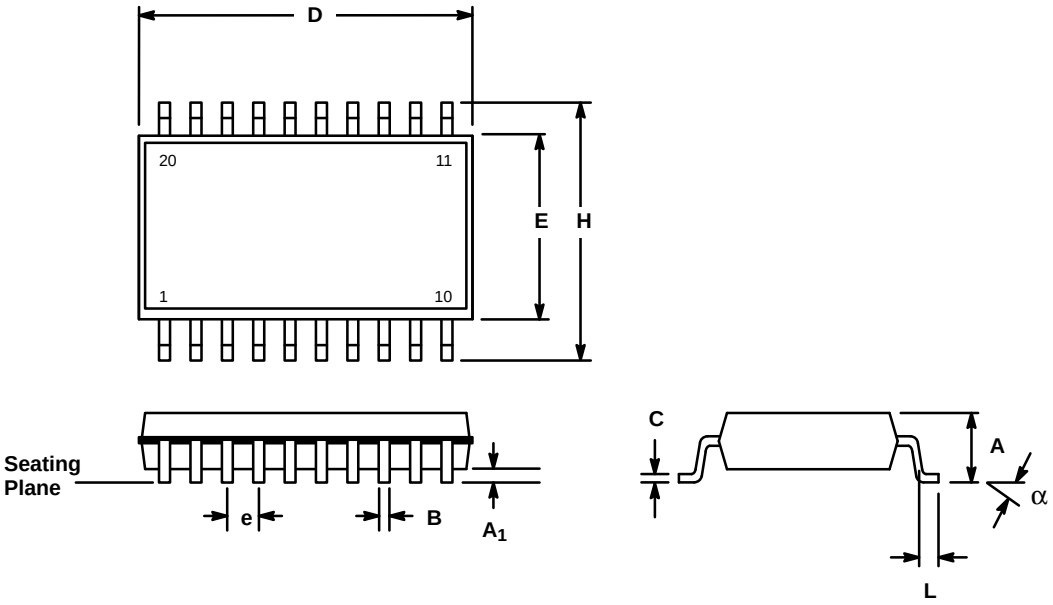
20 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.945	1.060	24.0	26.92
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.080	1.02	2.03

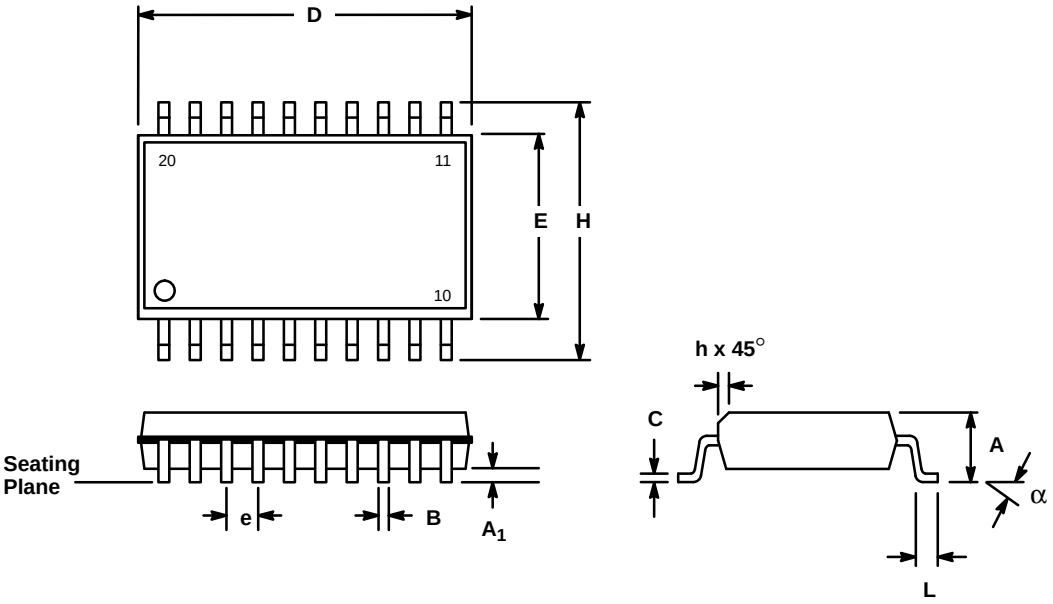
Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

20 LEAD SHRINK SMALL OUTLINE PACKAGE (SSOP) A20



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.73	2.05	0.068	0.081
A_1	0.05	0.21	0.002	0.008
B	0.20	0.40	0.008	0.016
C	0.13	0.25	0.005	0.010
D	7.07	7.40	0.278	0.291
E	5.20	5.38	0.205	0.212
e	0.65 BSC		0.0256 BSC	
H	7.65	8.1	0.301	0.319
L	0.45	0.95	0.018	0.037
α	0°	8°	0°	8°

20 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.642
A_1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.500	0.510	12.70	12.95
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

Notes

Notes

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