



MP87098

CMOS

Very Low Power, 750 KSPS, 10-Bit
Analog-to-Digital Converter with 4-Channel Mux

FEATURES

- 10-Bit Resolution
- 4-Channel Mux
- Sampling Rates from <1 kHz to 750 kHz
- Very Low Power CMOS - 30 mW (typ)
- Power Down; Lower Consumption – 3 mW (typ)
- Input Range between GND and V_{DD}
- No S/H Required for Analog Signals less than 100 kHz
- No S/H Required for CCD Signals less than 750 kHz
- Single Power Supply (4 to 6 Volts)
- Latch-Up Free CMOS Technology
- High ESD Protection: 4000 Volts Minimum

BENEFITS

- Reduced Board Space (Small Package)
- Reduced External Parts, No Sample/Hold Needed
- Suitable for Battery & Power Critical Applications
- Designer Can Adapt Input Range & Scaling

APPLICATIONS

- μ P/DSP Interface and Control Applications
- Multiplexed Data Acquisition
- Low Power A/D Applications

GENERAL DESCRIPTION

The MP87098 is a flexible, easy to use, precision 10-bit Analog-to-Digital Converter with a 4-channel mux that operates over a wide range of input and sampling conditions. The MP87098 can operate with pulsed “on demand” conversion operation or continuous “pipeline” operation for sampling rates up to 750 kHz. The elimination of the S/H and small package size offer the designer a low cost solution. No sample and hold is required for charge couple device applications up to 750 kHz, or multiplexed input applications when the signal source bandwidth is limited to 100 kHz. The input architecture of the MP87098 allows direct interface to any analog input range between AGND and AV_{DD} (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

Scaled reference resistor tap 1/2 R allows for customizing

the transfer curve as well as providing a 1/2 span reference voltage. Digital outputs are CMOS and TTL compatible.

The MP87098 uses a subranging technique. The first segment converts the 4 MSBs and consists of 15 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

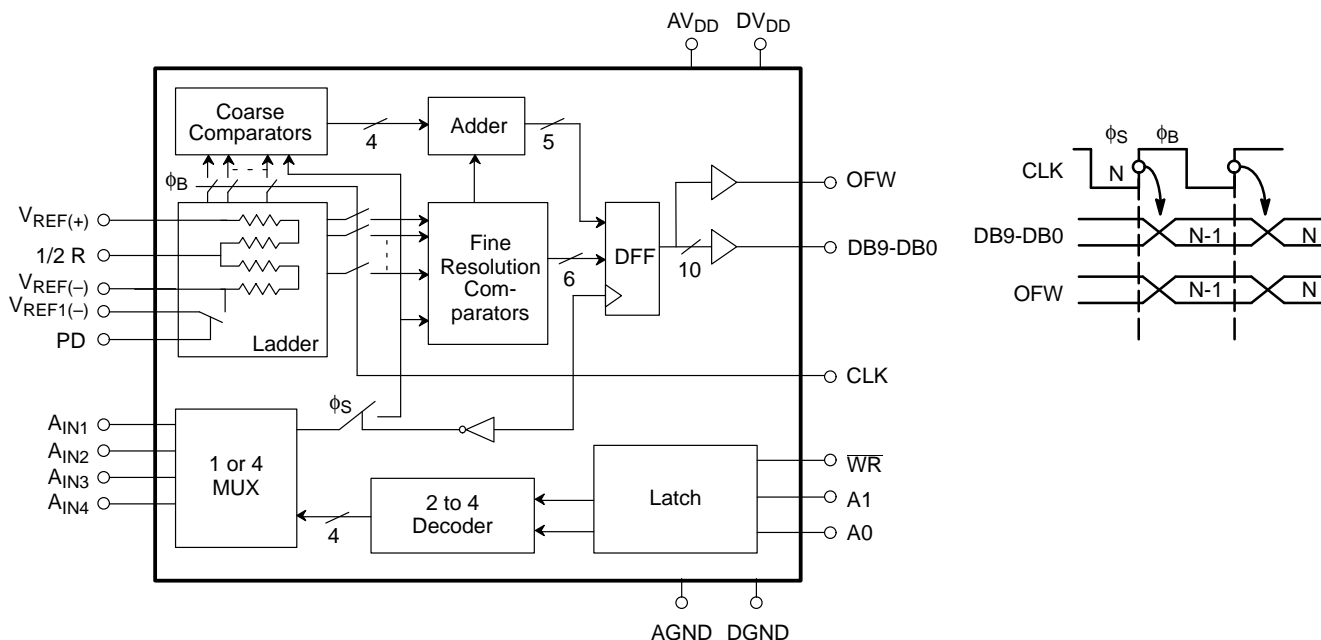
When the power down input is “high”, the data outputs DB9 to DB0 hold their current values and $V_{REF(-)}$ is disconnected from $V_{REF1(-)}$. The power consumption during the power down mode is approximately 3mW.

Specified for operation over the commercial / industrial (-40 to $+85^{\circ}\text{C}$) temperature range, the MP87098 is available in Plastic dual-in-line (PDIP) and Surface Mount (SOIC), and Shrink Small Outline (SSOP) packages.

ORDERING INFORMATION

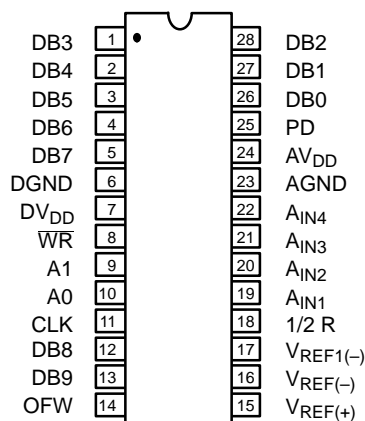
| Package Type | Temperature Range | Part No. | DNL (LSB) | INL (LSB) |
|--------------|--------------------------------|-----------|-----------|-----------|
| SOIC | -40 to $+85^{\circ}\text{C}$ | MP87098AS | ± 1 | 2 |
| PDIP | -40 to $+85^{\circ}\text{C}$ | MP87098AN | ± 1 | 2 |
| SSOP | -40 to $+85^{\circ}\text{C}$ | MP87098AQ | ± 1 | 2 |

SIMPLIFIED BLOCK AND TIMING DIAGRAM

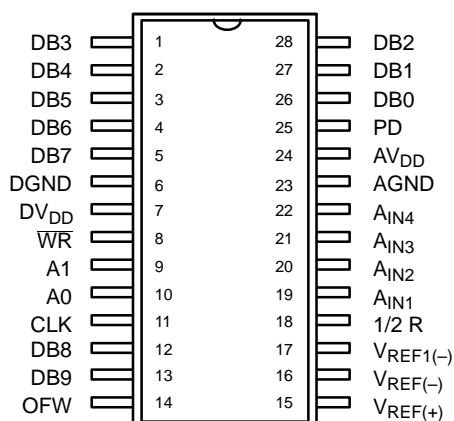


PIN CONFIGURATIONS

See Packaging Section for
Package Dimensions



28 Pin PDIP (0.300")
NN28



28 Pin SOIC (Jedec, 0.300") – S28
28 Pin SSOP – A28

PIN OUT DEFINITIONS

| PIN NO. | NAME | DESCRIPTION |
|---------|------------------|-------------------------|
| 1 | DB3 | Data Output Bit 3 |
| 2 | DB4 | Data Output Bit 4 |
| 3 | DB5 | Data Output Bit 5 |
| 4 | DB6 | Data Output Bit 6 |
| 5 | DB7 | Data Output Bit 7 |
| 6 | DGND | Digital Ground |
| 7 | DV _{DD} | Digital V _{DD} |
| 8 | WR | Write (Active Low) |
| 9 | A1 | Address 1 Input |
| 10 | A0 | Address 0 Input |
| 11 | CLK | Clock Input |
| 12 | DB8 | Data Output Bit 8 |
| 13 | DB9 | Data Output Bit 9 (MSB) |
| 14 | OFW | Overflow Output |

| PIN NO. | NAME | DESCRIPTION |
|---------|-----------------------|-------------------------|
| 15 | V _{REF} (+) | Upper Reference Voltage |
| 16 | V _{REF} (-) | Lower Reference Voltage |
| 17 | V _{REF1} (-) | Lower Reference Voltage |
| 18 | 1/2 R | Reference Ladder Tap |
| 19 | A _{IN1} | Analog Signal Input 1 |
| 20 | A _{IN2} | Analog Signal Input 2 |
| 21 | A _{IN3} | Analog Signal Input 3 |
| 22 | A _{IN4} | Analog Signal Input 4 |
| 23 | AGND | Analog Ground |
| 24 | AV _{DD} | Analog V _{DD} |
| 25 | PD | Power Down |
| 26 | DB0 | Data Output Bit 0 (LSB) |
| 27 | DB1 | Data Output Bit 1 |
| 28 | DB2 | Data Output Bit 2 |

TRUTH TABLE FOR INPUT CHANNEL SELECTION

| WR | A1 | A0 | SELECTED ANALOG INPUT |
|----|----|----|-----------------------|
| 0 | 0 | 0 | A _{IN1} |
| 0 | 0 | 1 | A _{IN2} |
| 0 | 1 | 0 | A _{IN3} |
| 0 | 1 | 1 | A _{IN4} |
| 1 | X | X | Previous selection |

Note: WR, A1, A0 are internally connected to GND through 500KΩ resistance.

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 5\text{ V}$, $F_S = 750\text{ kHz}$ (50% Duty Cycle),

$V_{REF(+)} = 4.6$, $V_{REF(-)} = AGND$, $T_A = 25^\circ\text{C}$

| Parameter | Symbol | Min | 25°C Typ | Max | Units | Test Conditions/Comments |
|--|---------------------------------|-----------------------|-------------|---------------------|--------|--|
| KEY FEATURES | | | | | | |
| Resolution | | 10 | | | Bits | |
| Sampling Rate | F _S | 1 | | 750 | kHz | For Rated Performance |
| ACCURACY² | | | | | | |
| Differential Non-Linearity | DNL | | ±3/4 | ±1 | LSB | Best Fit Line (Max INL – Min INL)/2 Reference from V _{REF(+)} to V _{REF(–)} |
| Integral Non-Linearity | INL | | | ±2 | LSB | |
| Zero Scale Error | EZS | | +0.50 | | LSB | |
| Full Scale Error | EFS | | –2.5 | | LSB | |
| REFERENCE VOLTAGES | | | | | | |
| Positive Ref. Voltage | V _{REF(+)} | | | AV _{DD} | V | |
| Negative Ref. Voltage | V _{REF(–)} | AGND | | | V | |
| Differential Ref. Voltage ⁵ | ΔV _{REF} | 0.5 | | AV _{DD} | V | |
| Ladder Resistance | R _L | 525 | 675 | 900 | Ω | |
| Ladder Temp. Coefficient | R _{TCO} | | 2000 | | ppm/°C | |
| Ladder Switch Resistance | | | 12 | | Ω | |
| Ladder Switch Off Leakage | I _{LKG-SW} | | 50 | | nA | |
| ANALOG INPUT¹ | | | | | | |
| Input Bandwidth | | | 100 | | kHz | |
| Input Voltage Range ⁷ | V _{IN} | V _{REF(–)} | | V _{REF(+)} | V | |
| Input Capacitance ³ | C _{IN} | | 60 | | pF | |
| Aperture Delay | t _{AP} | | 35 | 45 | ns | |
| DIGITAL INPUTS | | | | | | |
| Logical “1” Voltage | V _{IH} | 2.0 | | | V | V _{IN} =DGND to DV _{DD} |
| Logical “0” Voltage | V _{IL} | | | 0.8 | V | |
| Leakage Currents | I _{IN} | | | | μA | |
| CLK | | | | ±100 | μA | |
| PD, (Internal Res to GND) | | –5 | | 30 | μA | |
| Input Capacitance | | | 5 | | pF | |
| Clock Timing (<i>See Figure 1.</i>) ¹ | | | | | | |
| Clock Period | T _S | 1000 | | | ns | |
| Rise & Fall Time ⁴ | t _R , t _F | | | 10 | ns | |
| “High” Time ⁶ | t _B | 250 | | 500,000 | ns | |
| “Low” Time ⁶ | t _S | 150 | | 500,000 | ns | |
| DIGITAL OUTPUTS | | | | | | |
| Logical “1” Voltage | V _{OH} | DV _{DD} -0.5 | | | V | C _{OUT} =15 pF I _{LOAD} = 2 mA I _{LOAD} = 4 mA V _{OUT} = DGND to DV _{DD} |
| Logical “0” Voltage | V _{OL} | | | 0.4 | V | |
| Tristate Leakage | I _{OZ} | 0 | | ±5 | μA | |
| Data Hold Time (<i>See Figure 2.</i>) ¹ | t _{HLD} | | 30 | 35 | ns | |
| Data Valid Delay ¹ | t _{DL} | | 35 | 45 | ns | |

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

| Parameter | Symbol | Min | 25°C Typ | Max | Units | Test Conditions/Comments |
|--|---------------------|-----|-------------|-----|-------|--------------------------|
| DIGITAL OUTPUTS (CONT'D) | | | | | | C _{OUT} =15 pF |
| Write Pulse Width ¹ | t _{WR} | 40 | | | ns | |
| Multiplexer Address Setup Time ¹ | t _{AS} | 80 | | | ns | |
| Multiplexer Address Hold Time ¹ | t _{AH} | 0 | | | ns | |
| Delay from \overline{WR} to Multiplexer ¹ Enable | t _{MUXEN1} | | | 80 | ns | |
| Power Down Time ¹ | t _{PD} | | | 300 | ns | |
| Power Up Time ¹ | t _{PU} | | | 200 | ns | |
| POWER SUPPLIES ⁸ | | | | | | |
| Power Down (I _{DD}) | I _{PD-DD} | | 0.6 | 1.2 | mA | |
| Operating Voltage (AV _{DD} , DV _{DD}) | V _{DD} | 4 | 5 | 6.5 | V | |
| Current (AV _{DD} + DV _{DD}) | I _{DD} | | 6 | 10 | mA | V _{IN} = 2 V |

NOTES:

- ¹ Guaranteed. Not tested.
- ² Tester measures code transition voltages by dithering the voltage of the analog input (V_{IN}). The difference between the measured code width and the ideal value (V_{REF}/1024) is the DNL error (see Figure 4.). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (See Figure 6.).
- ³ See V_{IN} input equivalent circuit (see Figure 9.).
- ⁴ Clock specification to meet aperture specification (t_{AP}). Actual rise/fall time can be less stringent with no loss of accuracy.
- ⁵ Specified values guarantee functional device. Refer to other parameters for accuracy.
- ⁶ System can clock MP87098 with any duty cycle as long as all timing conditions are met.
- ⁷ Input range where input is converted correctly into binary code. Input voltage outside specified range converts to zero or full scale output.
- ⁸ DV_{DD} and AV_{DD} are connected through the silicon substrate. They should go to the same potential and be separately decoupled.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)^{1, 2, 3}

| | | | |
|---|------------------------------------|---|---------------|
| V _{DD} (to AGND, DGND) | +7 V | Storage Temperature | -65 to +150°C |
| V _{REF(+)} & V _{REF(-)} | GND -0.5 to V _{DD} +0.5 V | Lead Temperature (Soldering 10 seconds) | +300°C |
| V _{IN} | GND -0.5 to V _{DD} +0.5 V | Package Power Dissipation Rating to 75°C | |
| All Inputs | GND -0.5 to V _{DD} +0.5 V | SOIC, PDIP, SSOP | 1000mW |
| All Outputs | GND -0.5 to V _{DD} +0.5 V | Derates above 75°C | 14mW/°C |

NOTES:

- ¹ Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- ² Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100μs.
- ³ V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

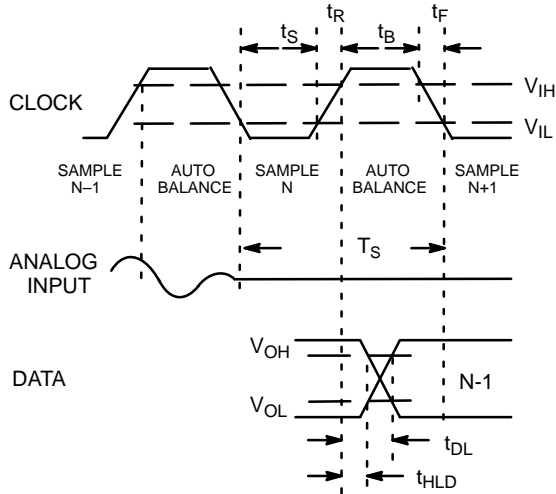


Figure 1. MP87098 Timing Diagram

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP87098 converts analog voltages into 1024 digital codes by encoding the outputs of 15 coarse and 67 fine comparators. Digital logic is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 2 clock periods.

The reference resistance ladder is a series of 1025 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$$R_{REF} = 1024 * R \quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 1024 * LSB$$

The clock signal generates the two internal phases, ϕ_B (CLK high) and ϕ_S (CLK low = sample) (See Figure 2.). The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant

when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The coarse comparators make the first pass conversion and selects a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next ϕ_B phase.

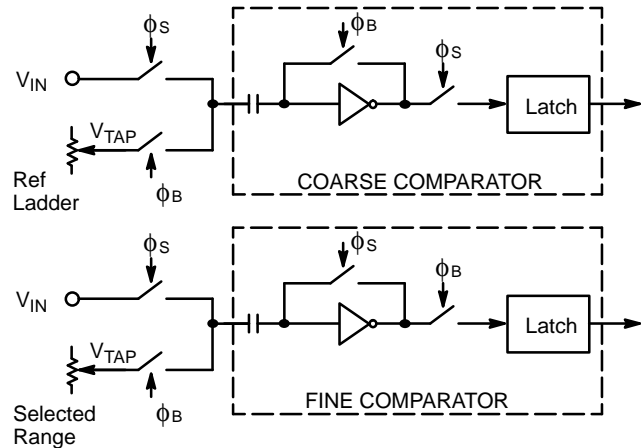


Figure 2. MP87098 Comparators

A_{IN} Sampling, Ladder Sampling, and Conversion Timing

Figure 3. shows this relationship as a timing chart. A_{IN} sampling, ladder sampling and output data relationships are shown for the general case where the levels which drive the ladder need to change for each sampled A_{IN} time point. The ladder is referenced for both last A_{IN} sample and next A_{IN} sample at the same time. If the ladder's levels change by more than 1 LSB, one of the samples must be discarded. Also note that the clock low period for the discarded A_{IN} can be reduced to the minimum t_S time of 150 ns.

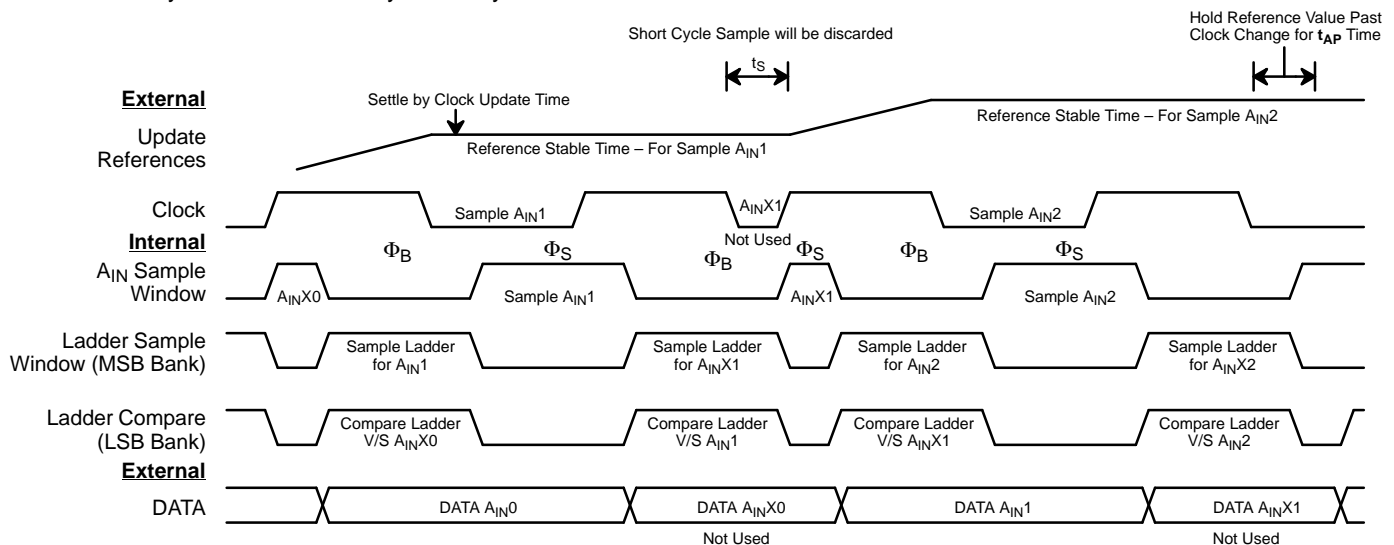


Figure 4. A_{IN} Sampling, Ladder Sampling & Conversion Timing

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in Figure 5.

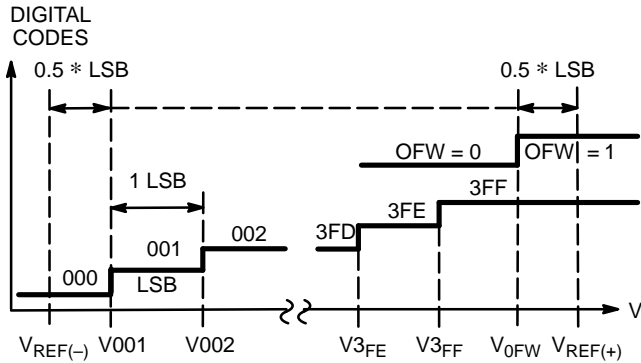


Figure 5. Ideal A/D Transfer Function

The overflow transition (V_{OFW}) takes place at:

$$V_{IN} = V_{OFW} = V_{REF(+)} - 0.5 * LSB$$

The first and the last transitions for the data bits take place at:

$$V_{IN} = V_{001} = V_{REF(-)} + 0.5 * LSB$$

$$V_{IN} = V_{3FF} = V_{REF(+)} - 1.5 * LSB$$

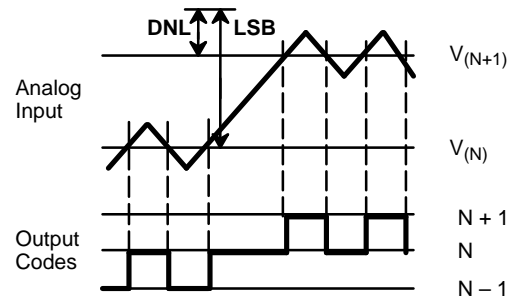
$$LSB = V_{REF} / 1024 = (V_{3FF} - V_{001}) / 1022$$

Note that the overflow transition is a flag and has no impact on the data bits.

In a "real" converter the code-to-code transitions don't fall exactly every $V_{REF}/1024$ volts.

A positive DNL (Differential Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSB's.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = ± 0.5 LSB means that all code widths are within 0.5 and 1.5 LSB. If $V_{REF} = 4.608$ V then 1 LSB = 4.5 mV and every code width is within 2.25 and 6.75 mV.



$$(N+1) \text{ Code Width} = V_{(N+1)} - V_{(N)}$$

$$LSB = [V_{REF(+)} - V_{REF(-)}] / 1024$$

$$DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - LSB$$

Figure 6. DNL Measurement On Production Tester

The formulas for Differential Non-Linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (E_{ZS} , E_{FS}) are:

$$DNL(001) = V_{002} - V_{001} - LSB$$

...

$$DNL(3FE) = V_{3FF} - V_{3FE} - LSB$$

$$E_{FS} \text{ (full scale error)} = V_{3FF} - [V_{REF(+)} - 1.5 * LSB]$$

$$E_{ZS} \text{ (zero scale error)} = V_{001} - [V_{REF(-)} + 0.5 * LSB]$$

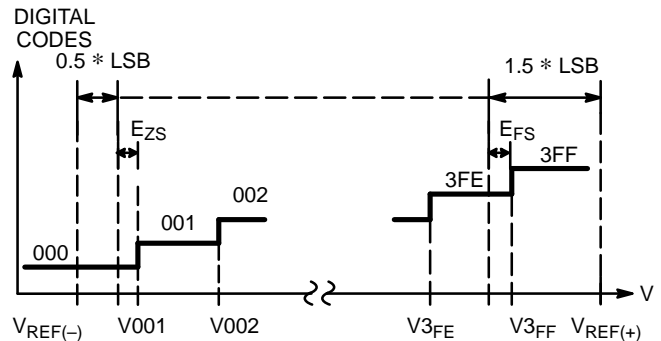


Figure 7. Real A/D Transfer Curve

Figure 7. shows the zero scale and full scale error terms.

Figure 8. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, the computer draws a line parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and the negative INL errors. For example, an INL error of -1 to $+2$ LSB's relative to the Ideal Line would be ± 1.5 LSB's relative to the Best Fit Line.

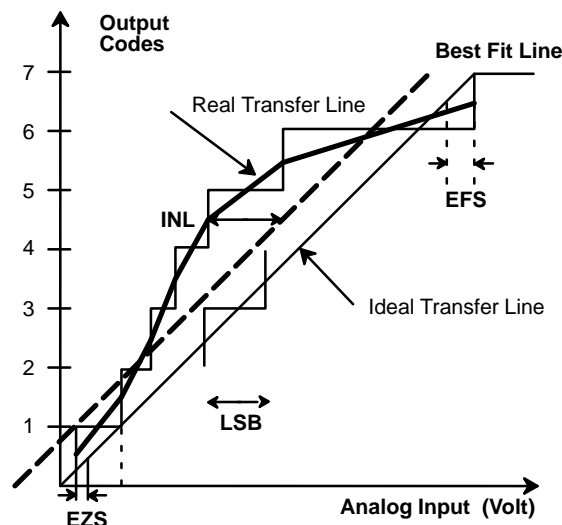


Figure 9. INL Error Calculation (Exaggerated for Visualization)

Clock and Conversion Timing

A system will clock the MP87098 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of Figure 8a shows normal operation, while the timing of Figure 8b keeps the MP87098 in balance and ready to sample the analog input.

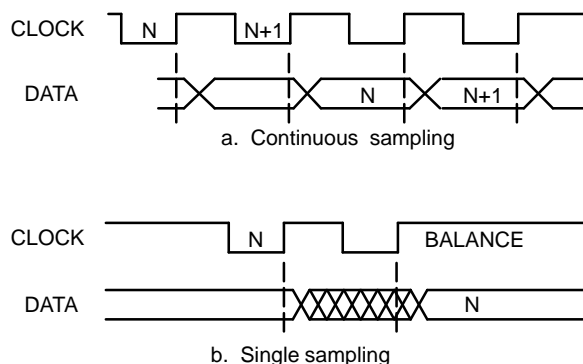


Figure 10. Relationship of Data to Clock

Analog Input

The MP87098 has very flexible input range characteristics. The user may set $V_{REF(+)}$ and $V_{REF(-)}$ to two fixed voltages and then vary the input DC and AC levels to match the V_{REF} range. Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP87098's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. Figure 11. shows the equivalent circuit for A_{IN} .

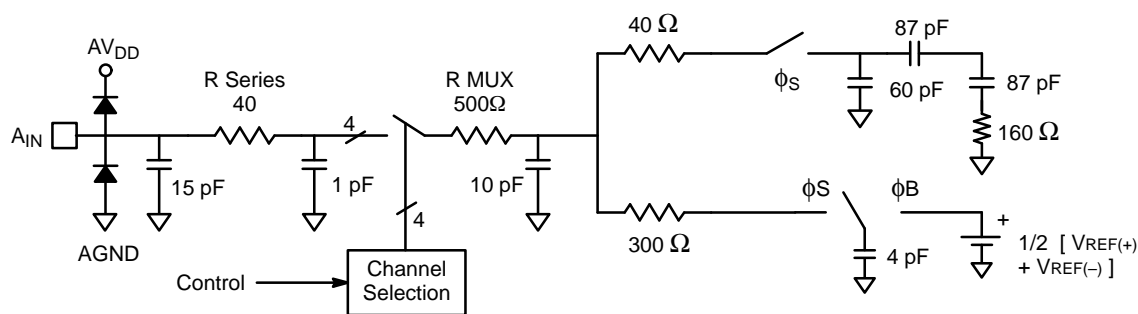


Figure 11. Analog Input Equivalent Circuit

Analog Input Multiplexer

The MP87098 includes a 4-channel analog input multiplexer. The relationship between the clock, the multiplexer address, the \overline{WR} and the output data is shown in *Figure 12*. and *Figure 13*.

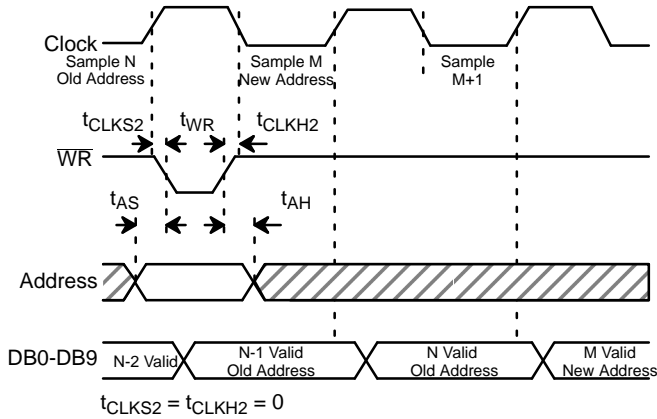


Figure 12. MUX Address Timing

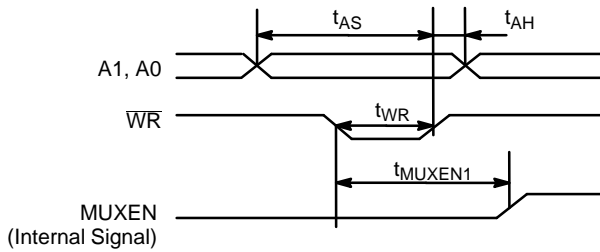


Figure 13. Analog MUX Timing

Reference Voltages

The input/output relationship is a function of V_{REF} :

$$\begin{aligned} A_{IN} &= V_{IN} - V_{REF(-)} \\ V_{REF} &= V_{REF(+)} - V_{REF(-)} \\ DATA &= 1023 * (A_{IN}/V_{REF}) \end{aligned}$$

A system can increase total gain by reducing V_{REF} .

Digital Interfaces

The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output.

The functional equivalent of the MP87098 (*Figure 14*.) is composed of:

- 1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
- 2) An ideal analog switch which samples V_{IN} .
- 3) An ideal A/D which tracks and converts V_{IN} with no delay.
- 4) A series of two DFF's with specified hold (t_{HLD}) and delay (t_{DL}) times.

t_{AP} , t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

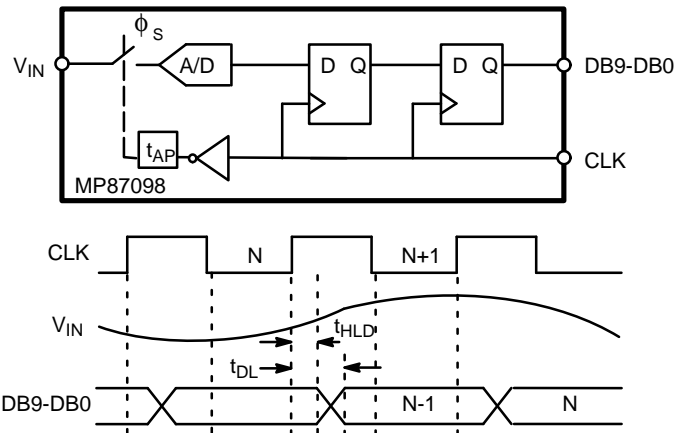


Figure 14. MP87098 Functional Equivalent Circuit and Interface Timing

Power Down

Figure 15. shows the relationship between the clock, sampled A_{IN} to output data relationship and the effect of power down.

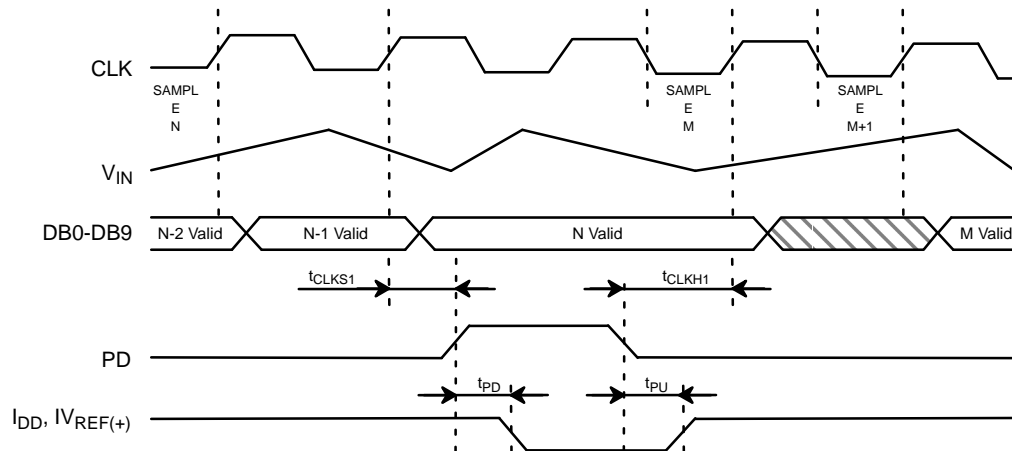


Figure 15. Power Down Timing Diagram

APPLICATION NOTES

$C_1 = 4.7$ or $10\mu\text{F}$ Tantalum
 $C_2 = 0.1\mu\text{F}$ Chip Cap or low inductance capacitor
 R_T = Clock Transmission Line Termination

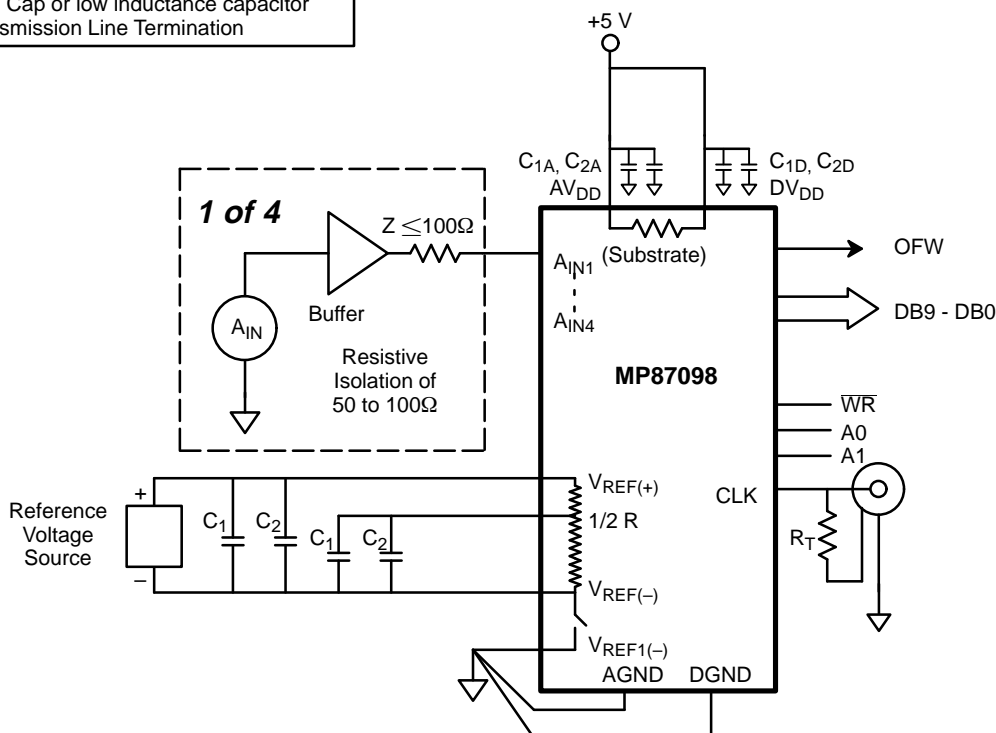


Figure 16. Typical Circuit Connections

The following information will be useful in maximizing the performance of the MP87098.

1. All signals should not exceed $AV_{DD} + 0.5\text{ V}$ or $AGND - 0.5\text{ V}$ or $DV_{DD} + 0.5\text{ V}$.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or $DV_{DD} + 0.5\text{ V}$ or $AGND - 0.5\text{ V}$) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP7684A inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP87098. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths. *DGND should not be shared with other digital circuitry.* If separate low impedance paths cannot be provided, DGND should be connected to AGND next to the MP87098.
7. *DVDD should not be shared with other digital circuitry* to avoid conversion errors caused by digital supply transients. DVDD for the MP87098 should be connected to AVDD next to the MP87098.
8. DVDD and AVDD are connected inside the MP87098 through the N – doped silicon substrate. Any DC voltage difference between DVDD and AVDD will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic ($0.1\mu\text{F}$) and a tantalum ($10\mu\text{F}$) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used. 100Ω resistors in series with the digital outputs in some applications reduces the digital output disruption of A_{IN} .

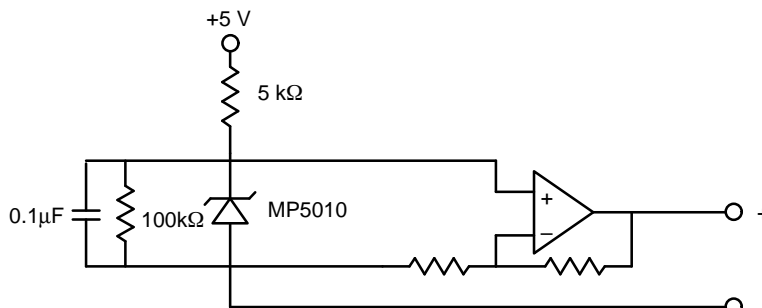
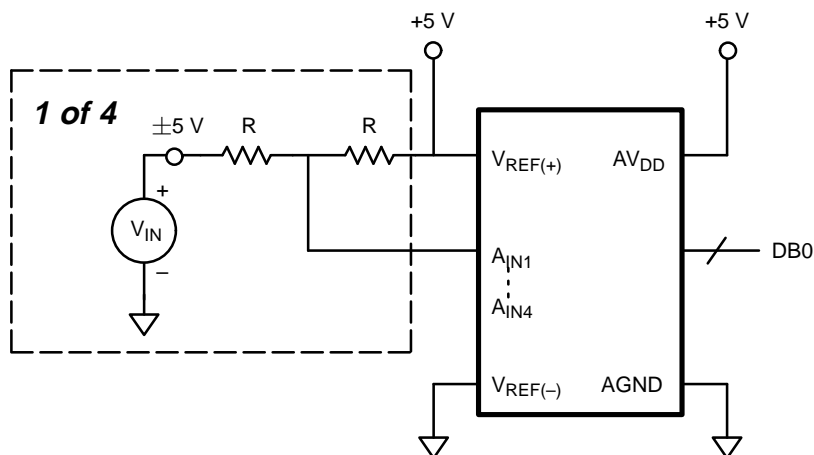


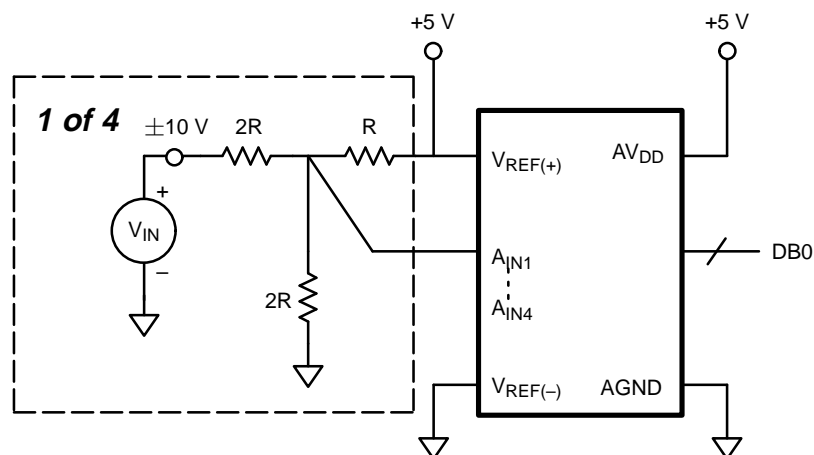
Figure 17. Example of a Reference Voltage Source



For $R = 5k$ use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the $(R * C_{IN})$ of ADC time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

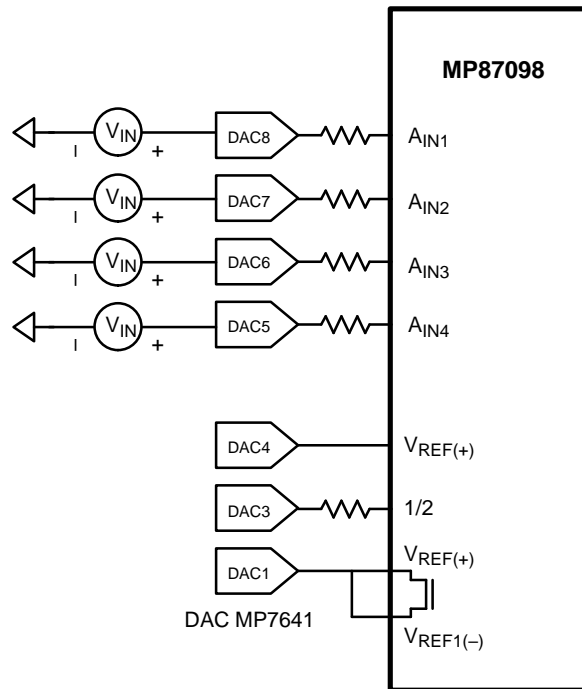
Figure 18. ± 5 V Analog Input



For $R = 5k$ use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the $(R * C_{IN})$ of ADC time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

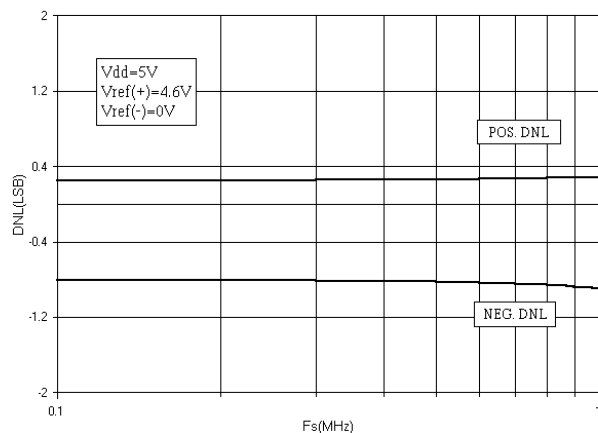
Figure 19. ± 10 V Analog Input



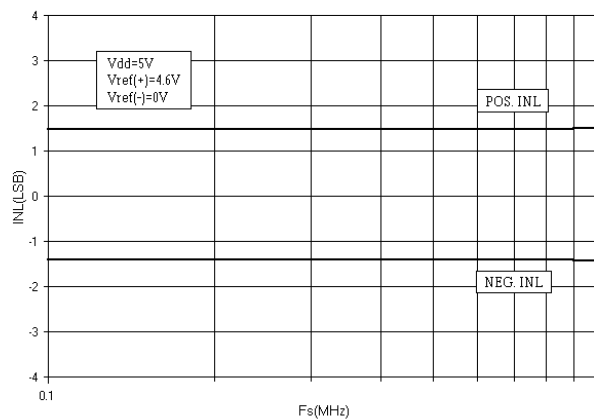
@ Power Down write values to DAC 3, 2, 1 = DAC 4 to minimize power consumption.
Only A_{IN} and Ladder detail shown.

**Figure 20. A/D Ladder and A_{IN} with Programmed Control
 (of V_{REF}(+), V_{REF}(-), 1/2 TAP.)**

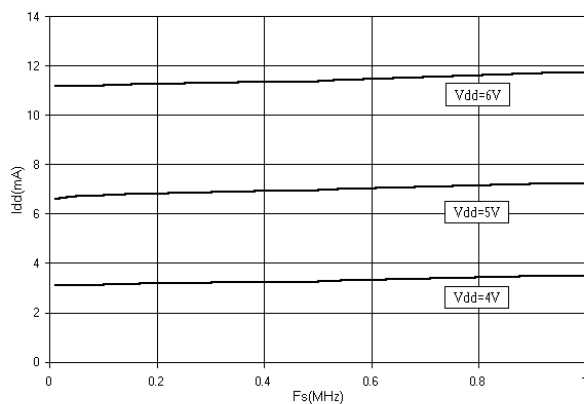
PERFORMANCE CHARACTERISTICS



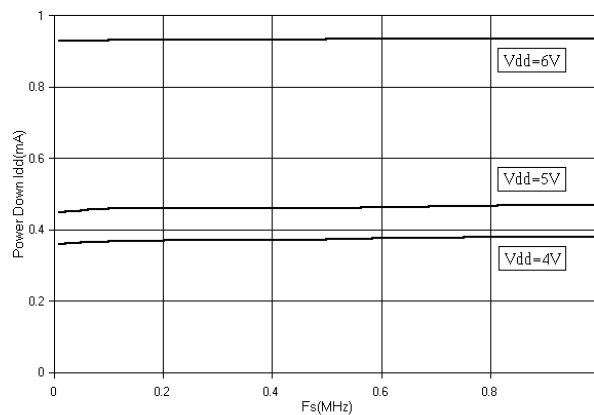
Graph 1. DNL vs. Sampling Frequency



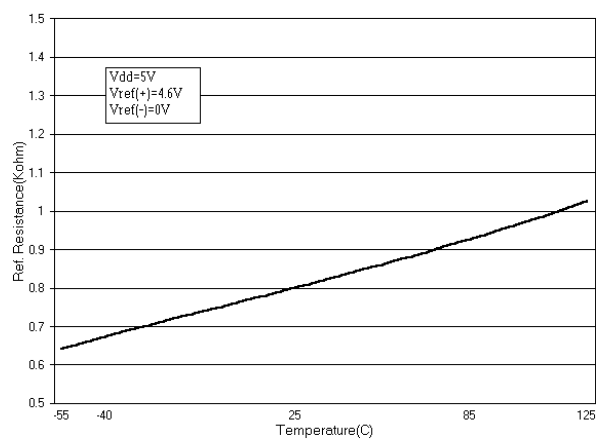
Graph 2. INL vs. Sampling Frequency



Graph 3. Supply Current vs. Sampling Frequency

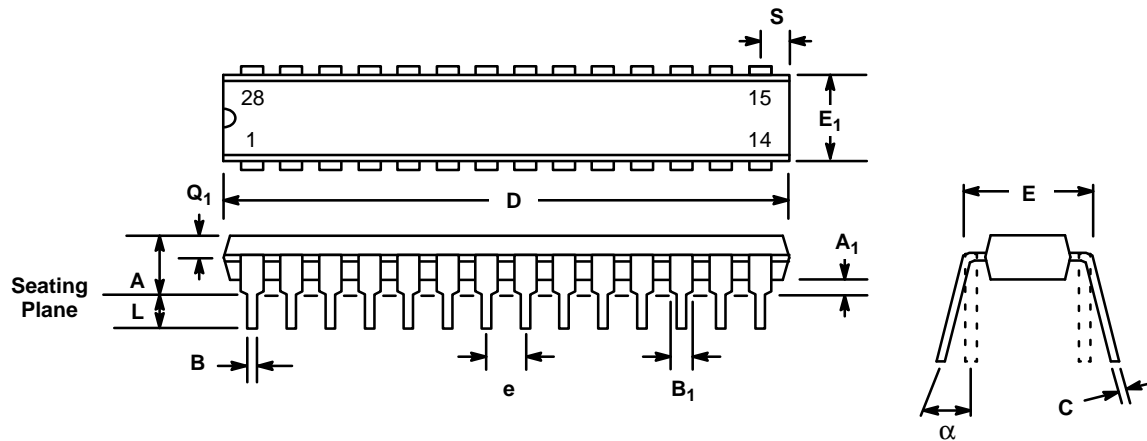


Graph 4. Power Down Current vs. Sampling Frequency



Graph 5. Reference Resistance vs. Temperature

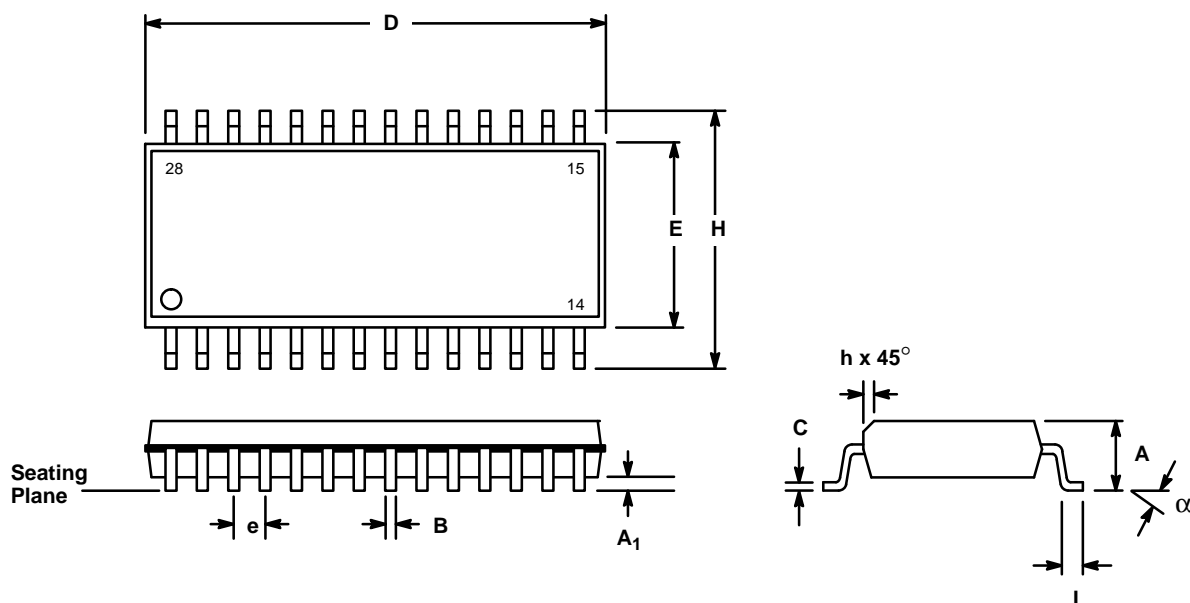
**28 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
NN28**



| SYMBOL | INCHES | | MILLIMETERS | |
|--------------------|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.130 | 0.230 | 3.30 | 5.84 |
| A ₁ | 0.015 | — | 0.381 | — |
| B | 0.014 | 0.023 | 0.356 | 0.584 |
| B ₁ (1) | 0.038 | 0.065 | 0.965 | 1.65 |
| C | 0.008 | 0.015 | 0.203 | 0.381 |
| D | 1.340 | 1.485 | 34.04 | 37.72 |
| E | 0.290 | 0.325 | 7.37 | 8.26 |
| E ₁ | 0.240 | 0.310 | 6.10 | 7.87 |
| e | 0.100 BSC | | 2.54 BSC | |
| L | 0.115 | 0.150 | 2.92 | 3.81 |
| α | 0° | 15° | 0° | 15° |
| Q ₁ | 0.055 | 0.070 | 1.40 | 1.78 |
| S | 0.020 | 0.100 | 0.508 | 2.54 |

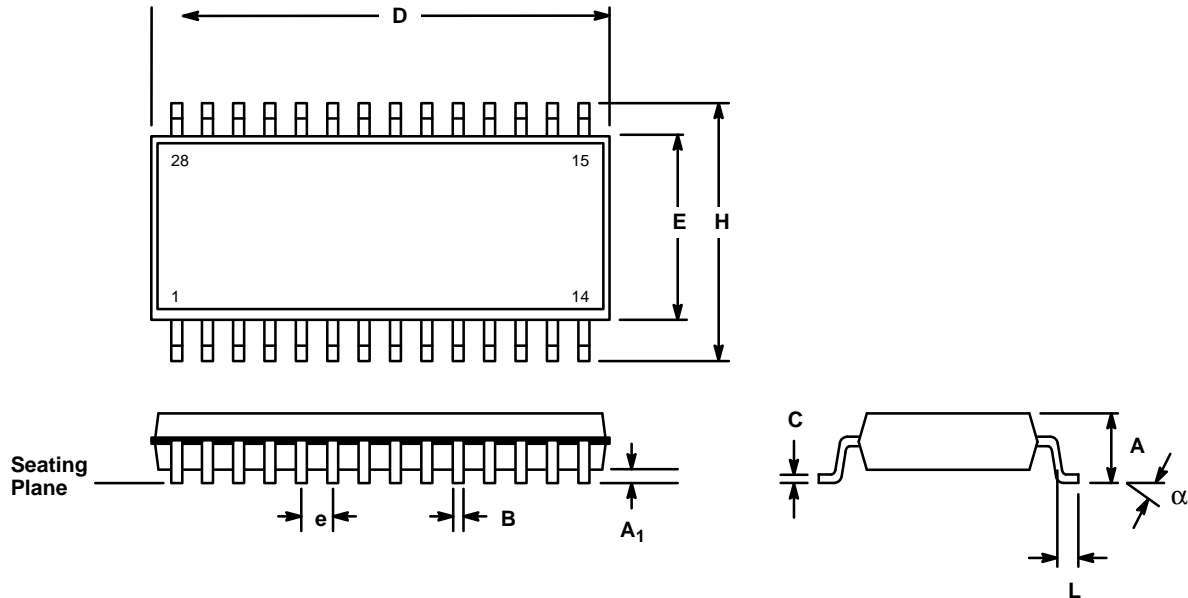
Note: (1) The minimum limit for dimensions B₁ may be 0.023" (0.58 mm) for all four corner leads only.

28 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC) S28



| SYMBOL | INCHES | | MILLIMETERS | |
|----------|-----------|--------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.097 | 0.104 | 2.464 | 2.642 |
| A1 | 0.0050 | 0.0115 | 0.127 | 0.292 |
| B | 0.014 | 0.019 | 0.356 | 0.483 |
| C | 0.0091 | 0.0125 | 0.231 | 0.318 |
| D | 0.701 | 0.711 | 17.81 | 18.06 |
| E | 0.292 | 0.299 | 7.42 | 7.59 |
| e | 0.050 BSC | | 1.27 BSC | |
| H | 0.400 | 0.410 | 10.16 | 10.41 |
| h | 0.010 | 0.016 | 0.254 | 0.406 |
| L | 0.016 | 0.035 | 0.406 | 0.889 |
| α | 0° | 8° | 0° | 8° |

**28 LEAD SHRINK SMALL OUTLINE PACKAGE
(SSOP)
A28**



| SYMBOL | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.73 | 2.05 | 0.068 | 0.081 |
| A ₁ | 0.05 | 0.21 | 0.002 | 0.008 |
| B | 0.20 | 0.40 | 0.008 | 0.016 |
| C | 0.13 | 0.25 | 0.005 | 0.010 |
| D | 10.07 | 10.40 | 0.397 | 0.409 |
| E | 5.20 | 5.38 | 0.205 | 0.212 |
| e | 0.65 BSC | | 0.0256 BSC | |
| H | 7.65 | 8.1 | 0.301 | 0.319 |
| L | 0.45 | 0.95 | 0.018 | 0.037 |
| α | 0° | 8° | 0° | 8° |

Notes

Notes

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Datasheet April 1995

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