

### FEATURES

- 10-Bit Resolution
- Sampling Rates from <1 kHz to 750 KSPS
- DNL better than 1/2 LSB up to 750 kHz
- Very Low Power CMOS - 30 mW (typ)
- Power Down; Lower Consumption – 3 mW (typ)
- Input Range between GND and  $V_{DD}$
- No S/H Required for Analog Signals less than 100 kHz
- No S/H Required for CCD Signals less than 750 kHz
- Single Power Supply (4 to 6.5 Volts)
- Latch-Up Free
- High ESD Protection: 4000 Volts Minimum
- 20 Pin Package: MP8796

### BENEFITS

- Reduced External Parts, No Sample/Hold Needed
- Suitable for Battery & Power Critical Applications
- Designer Can Adapt Input Range & Scaling

### APPLICATIONS

- $\mu$ P/DSP Interface and Control Applications
- Multiplexed Data Acquisition
- Radar Pulse Analysis
- Low Power A/D Applications

### GENERAL DESCRIPTION

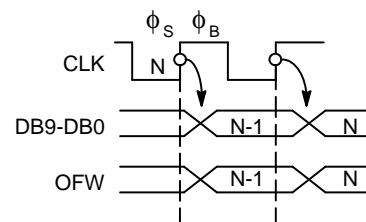
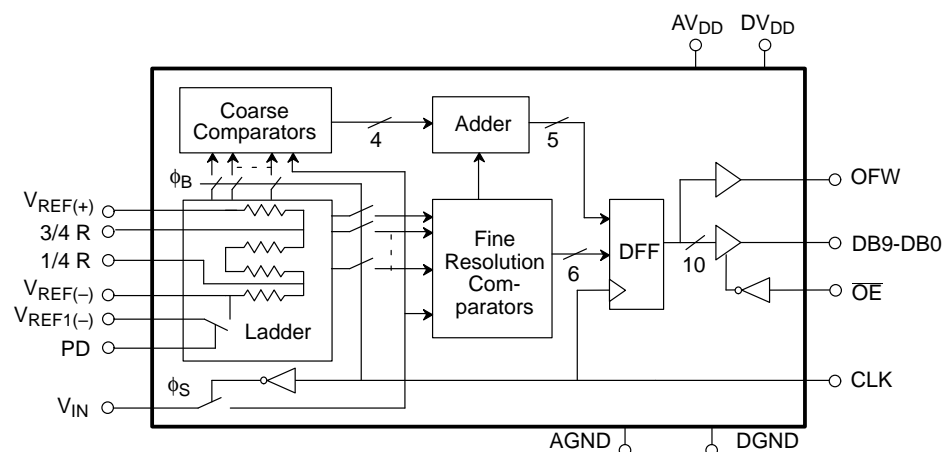
The MP87095 is a flexible, easy to use, precision 10-bit A/D Converter that operates over a wide range of input and sampling conditions. The MP87095 can operate with pulsed "on demand" conversion operation or continuous "pipeline" operation for sampling rates up to 750 kHz. The elimination of the S/H and small package size offer the designer a low cost solution. No sample and hold is required for charge couple device applications up to 750 kHz, or multiplexed input applications when the signal source bandwidth is limited to 100 kHz. The input architecture of the MP87095 allows direct interface to any analog input range between AGND and  $AV_{DD}$  (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets  $V_{REF(+)}$  and  $V_{REF(-)}$  to encompass the desired input range.

Scaled reference resistor taps 1/4 R and 3/4 R allow for customizing the transfer curve. Digital outputs offer tri-state operation and all digital pins are CMOS and TTL compatible.

The MP87095 uses a subranging technique. The first segment converts the 4 MSBs and consists of 15 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

When the power down input is "high", the data outputs DB9 to DB0 hold the current values and  $V_{REF(-)}$  is disconnected from  $V_{REF1(-)}$ . The power consumption during the power down mode is approximately 3mW.

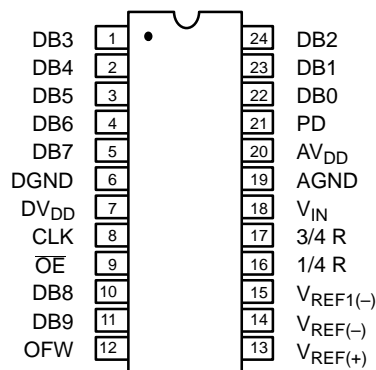
### SIMPLIFIED BLOCK AND TIMING DIAGRAM



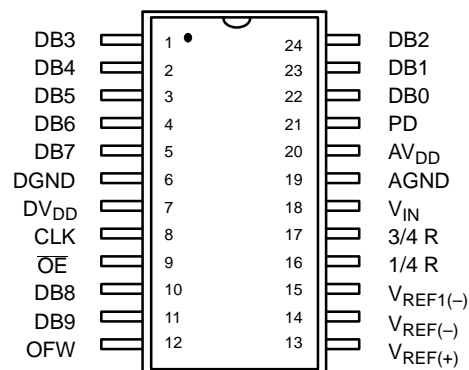
## ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	-40 to +85°C	MP87095AN	±1	2
SOIC	-40 to +85°C	MP87095AS	±1	2

## PIN CONFIGURATIONS



**24 Pin PDIP (0.300")  
NN24**



**24 Pin SOIC (Jedec, 0.300")  
S24**

## PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB3	Data Output Bit 3
2	DB4	Data Output Bit 4
3	DB5	Data Output Bit 5
4	DB6	Data Output Bit 6
5	DB7	Data Output Bit 7
6	DGND	Digital Ground
7	DVDD	Digital VDD
8	CLK	Clock Input
9	OE	Output Enable (Active Low)
10	DB8	Data Output Bit 8
11	DB9	Data Output Bit 9 (MSB)
12	OFW	Overflow Output

PIN NO.	NAME	DESCRIPTION
13	VREF(+)	Upper Reference Voltage
14	VREF(-)	Lower Reference Voltage
15	VREF1(-)	Lower Reference Voltage
16	1/4 R	Reference Ladder Tap @ 1/4 FS
17	3/4 R	Reference Ladder Tap @ 3/4 FS
18	VIN	Analog Signal Input
19	AGND	Analog Ground
20	AVDD	Analog VDD
21	PD	Power Down
22	DB0	Data Output Bit 0 (LSB)
23	DB1	Data Output Bit 1
24	DB2	Data Output Bit 2

## ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified:  $AV_{DD} = DV_{DD} = 5\text{ V}$ ,  $F_S = 0.75\text{ MHz}$  (50% Duty Cycle),

$V_{REF(+)} = 4.6$ ,  $V_{REF(-)} = AGND$ ,  $T_A = 25^\circ\text{C}$

Parameter	Symbol	Min	25°C Typ	Max	Units	Test Conditions/Comments
<b>KEY FEATURES</b>						
Resolution		10			Bits	For Rated Performance
Sampling Rate	F <sub>S</sub>	.001		0.75	MHz	
<b>ACCURACY<sup>2</sup></b>						
Differential Non-Linearity	DNL			±1	LSB	Best Fit Line (Max INL – Min INL)/2 Reference from V <sub>REF(+)</sub> to V <sub>REF(–)</sub>
Integral Non-Linearity	INL			±2	LSB	
Zero Scale Error	EZS		+1.00		LSB	
Full Scale Error	EFS		–2.5		LSB	
<b>REFERENCE VOLTAGES</b>						
Positive Ref. Voltage	V <sub>REF(+)</sub>			AV <sub>DD</sub>	V	
Negative Ref. Voltage	V <sub>REF(–)</sub>	AGND			V	
Differential Ref. Voltage <sup>5</sup>	V <sub>REF</sub>	0.5		AV <sub>DD</sub>	V	
Ladder Resistance	R <sub>L</sub>	525	675	900	Ω	
Ladder Temp. Coefficient <sup>1</sup>	R <sub>TCO</sub>		2000		ppm/°C	
Ladder Switch Resistance			12		Ω	
Ladder Switch Off Leakage	I <sub>ILKG-SW</sub>		50		nA	
<b>ANALOG INPUT<sup>1</sup></b>						
Input Bandwidth			100		kHz	1 LSB Error
Input Voltage Range <sup>7</sup>	V <sub>IN</sub>	V <sub>REF(–)</sub>		V <sub>REF(+)</sub>	V	
Input Capacitance <sup>3</sup>	C <sub>IN</sub>		60		pF	
Aperture Delay	t <sub>AP</sub>		35	45	ns	
<b>DIGITAL INPUTS</b>						
Logical “1” Voltage	V <sub>IH</sub>	2.0			V	V <sub>IN</sub> =DGND to DV <sub>DD</sub>
Logical “0” Voltage	V <sub>IL</sub>			0.8	V	
Leakage Currents	I <sub>IN</sub>			±100	μA	
CLK				30	μA	
PD, $\overline{OE}$ (Internal Res to GND)		–5			μA	
Input Capacitance			5		pF	
Clock Timing ( <i>See Figure 1.</i> ) <sup>1</sup>						
Clock Period	T <sub>S</sub>	500			ns	
Rise & Fall Time <sup>4</sup>	t <sub>R</sub> , t <sub>F</sub>			10	ns	Functional
“High” Time <sup>6</sup>	t <sub>B</sub>	250		500,000	ns	
“Low” Time <sup>6</sup>	t <sub>S</sub>	150		500,000	ns	
<b>DIGITAL OUTPUTS</b>						
Logical “1” Voltage	V <sub>OH</sub>	DV <sub>DD</sub> –0.5			V	C <sub>OUT</sub> =15 pF  I <sub>LOAD</sub> = 2 mA I <sub>LOAD</sub> = 4 mA V <sub>OUT</sub> = DGND to DV <sub>DD</sub>
Logical “0” Voltage	V <sub>OL</sub>			0.4	V	
Tristate Leakage	I <sub>OZ</sub>	0		±5	μA	
Data Hold Time ( <i>See Figure 1.</i> ) <sup>1</sup>	t <sub>HLD</sub>		30	35	ns	
Data Valid Delay <sup>1</sup>	t <sub>DL</sub>		35	45	ns	

## ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	Min	25°C Typ	Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS (CONT'D)						C <sub>OUT</sub> =15 pF
Data Enable Delay <sup>1</sup>	t <sub>DEN</sub>		25	30	ns	
Data Tristate Delay <sup>1</sup>	t <sub>DHZ</sub>		15	30	ns	
Clock to PD Set-up Time <sup>1</sup>	t <sub>CLKS1</sub>			400	ns	
Clock to PD Hold Time <sup>1</sup>	t <sub>CLKH1</sub>			600	ns	
Power Down Delay <sup>1</sup>	t <sub>PD</sub>			300	ns	
Power Up Delay <sup>1</sup>	t <sub>PU</sub>			200	ns	
POWER SUPPLIES <sup>8</sup>						V <sub>IN</sub> = 2 V
Power Down (I <sub>DD</sub> )	I <sub>DDDOWN</sub>		0.6	1.2	mA	
Operating Voltage (AV <sub>DD</sub> , DV <sub>DD</sub> )	V <sub>DD</sub>	4	5	6.5	V	
Current (AV <sub>DD</sub> + DV <sub>DD</sub> )	I <sub>DD</sub>		6	10	mA	

## NOTES:

- <sup>1</sup> Guaranteed. Not tested.
- <sup>2</sup> Tester measures code transition voltages by dithering the voltage of the analog input (V<sub>IN</sub>). The difference between the measured code width and the ideal value (V<sub>REF</sub>/1024) is the DNL error (see Figure 5.). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (See Figure 7.).
- <sup>3</sup> See V<sub>IN</sub> input equivalent circuit (see Figure 9.).
- <sup>4</sup> Clock specification to meet aperture specification (t<sub>AP</sub>). Actual rise/fall time can be less stringent with no loss of accuracy.
- <sup>5</sup> Specified values guarantee functional device. Refer to other parameters for accuracy.
- <sup>6</sup> System can clock MP87095 with any duty cycle as long as all timing conditions are met.
- <sup>7</sup> Input range where input is converted correctly into binary code. Input voltage outside specified range converts to zero or full scale output.
- <sup>8</sup> DV<sub>DD</sub> and AV<sub>DD</sub> are connected through the silicon substrate. Connect together at the package.

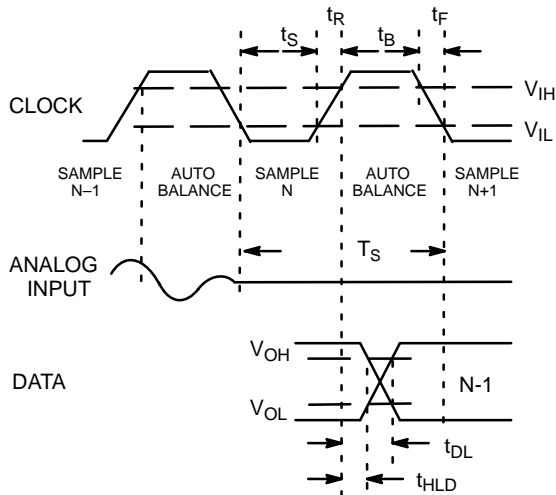
Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)<sup>1, 2, 3</sup>

V <sub>DD</sub> (to GND) .....	+7 V	Storage Temperature .....	-65 to +150°C
V <sub>REF(+)</sub> & V <sub>REF(-)</sub> .....	GND -0.5 to V <sub>DD</sub> +0.5 V	Lead Temperature (Soldering 10 seconds) .....	+300°C
V <sub>IN</sub> .....	GND -0.5 to V <sub>DD</sub> +0.5 V	Package Power Dissipation Rating to 75°C	
All Inputs .....	GND -0.5 to V <sub>DD</sub> +0.5 V	PDIP, SOIC .....	1000mW
All Outputs .....	GND -0.5 to V <sub>DD</sub> +0.5 V	Derates above 75°C .....	14mW/°C

## NOTES:

- <sup>1</sup> Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- <sup>2</sup> Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100μs.
- <sup>3</sup> V<sub>DD</sub> refers to AV<sub>DD</sub> and DV<sub>DD</sub>. GND refers to AGND and DGND.



**Figure 1. MP87095 Timing Diagram**

## THEORY OF OPERATION

### Analog-to-Digital Conversion

The MP87095 converts analog voltages into 1024 digital codes by encoding the outputs of 15 coarse and 67 fine comparators. Digital logic is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 2 clock periods.

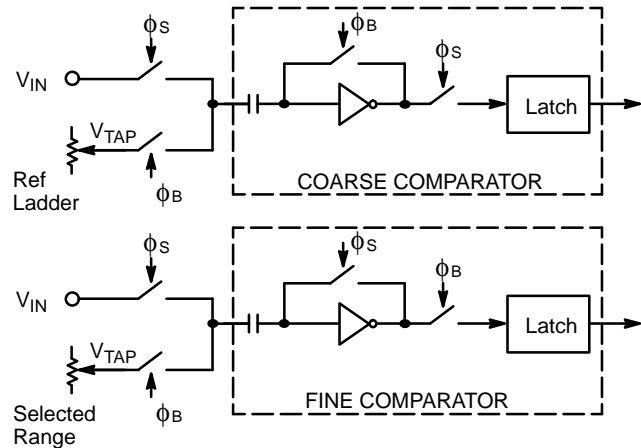
The reference resistance ladder is a series of 1025 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$$R_{REF} = 1024 * R \quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 1024 * LSB$$

The clock signal generates the two internal phases,  $\phi_B$  (CLK high) and  $\phi_S$  (CLK low = sample) (See Figure 2.). The rising edge of the CLK input marks the end of the sampling phase ( $\phi_S$ ). Internal delay of the clock circuitry will delay the actual instant

when  $\phi_S$  disconnects the latches from the comparators. This delay is called aperture delay ( $t_{AP}$ ).

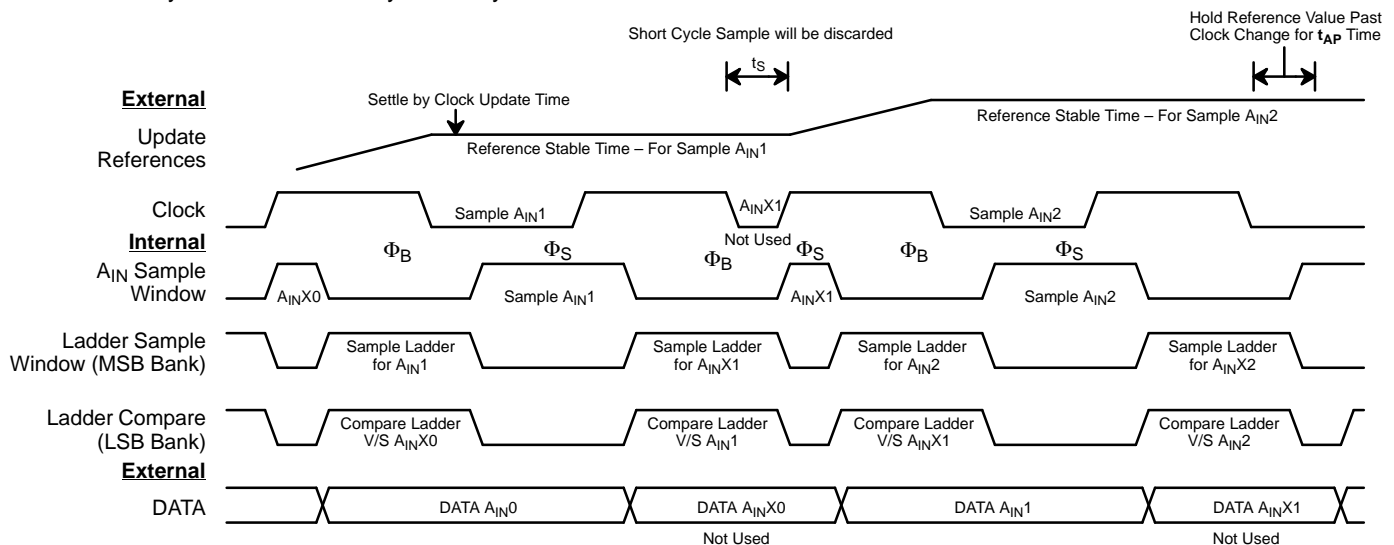
The coarse comparators make the first pass conversion and selects a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next  $\phi_B$  phase.



**Figure 2. MP87095 Comparators**

### $A_{IN}$ Sampling, Ladder Sampling, and Conversion Timing

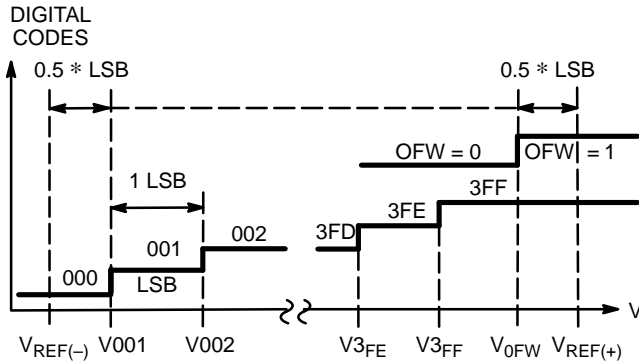
Figure 3. shows this relationship as a timing chart.  $A_{IN}$  sampling, ladder sampling and output data relationships are shown for the general case where the levels which drive the ladder need to change for each sampled  $A_{IN}$  time point. The ladder is referenced for both last  $A_{IN}$  sample and next  $A_{IN}$  sample at the same time. If the ladder's levels change by more than 1 LSB, one of the samples must be discarded. Also note that the clock low period for the discarded  $A_{IN}$  can be reduced to the minimum  $t_S$  time of 150 ns.



**Figure 3.  $A_{IN}$  Sampling, Ladder Sampling & Conversion Timing**

## Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in Figure 4.



**Figure 4. Ideal A/D Transfer Function**

The overflow transition ( $V_{OFW}$ ) takes place at:

$$V_{IN} = V_{OFW} = V_{REF(+)} - 0.5 * LSB$$

The first and the last transitions for the data bits take place at:

$$V_{IN} = V_{001} = V_{REF(-)} + 0.5 * LSB$$

$$V_{IN} = V_{3FF} = V_{REF(-)} - 1.5 * LSB$$

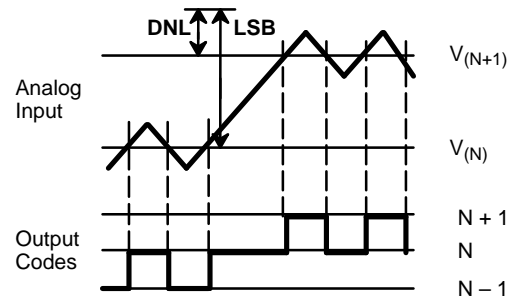
$$LSB = V_{REF} / 1024 = (V_{3FF} - V_{001}) / 1022$$

Note that the overflow transition is a flag and has no impact on the data bits.

In a "real" converter the code-to-code transitions don't fall exactly every  $V_{REF}/1024$  volts.

A positive DNL (Differential Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSB's.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL =  $\pm 0.5$  LSB means that all code widths are within 0.5 and 1.5 LSB. If  $V_{REF} = 4.608$  V then 1 LSB = 4.5 mV and every code width is within 2.25 and 6.75 mV.



$$(N+1) \text{ Code Width} = V_{(N+1)} - V_{(N)}$$

$$LSB = [V_{REF(+)} - V_{REF(-)}] / 1024$$

$$DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - LSB$$

**Figure 5. DNL Measurement On Production Tester**

The formulas for Differential Non-Linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors ( $E_{ZS}$ ,  $E_{FS}$ ) are:

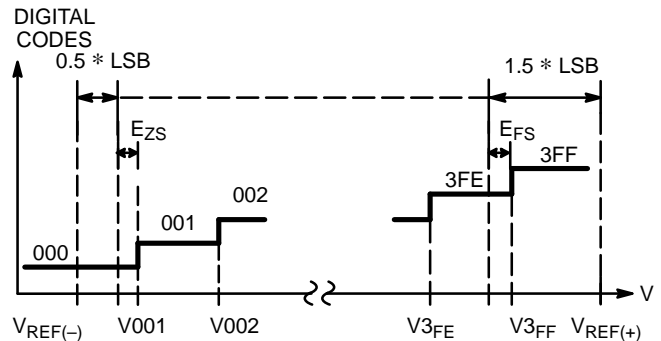
$$DNL(001) = V_{002} - V_{001} - LSB$$

...

$$DNL(3FE) = V_{3FF} - V_{3FE} - LSB$$

$$E_{FS} \text{ (full scale error)} = V_{3FF} - [V_{REF(+)} - 1.5 * LSB]$$

$$E_{ZS} \text{ (zero scale error)} = V_{001} - [V_{REF(-)} + 0.5 * LSB]$$

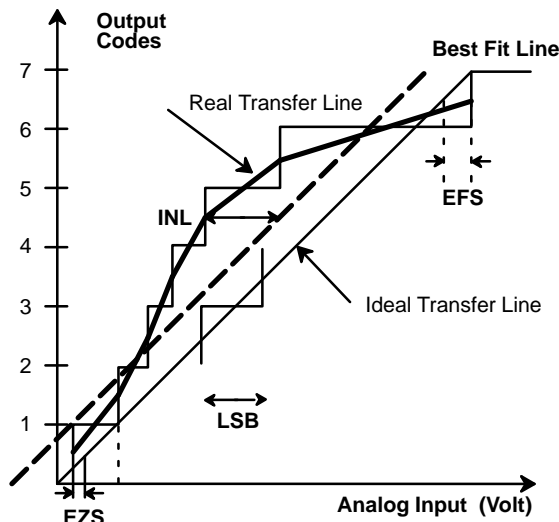


**Figure 6. Real A/D Transfer Curve**

Figure 6. shows the zero scale and full scale error terms.

Figure 7. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

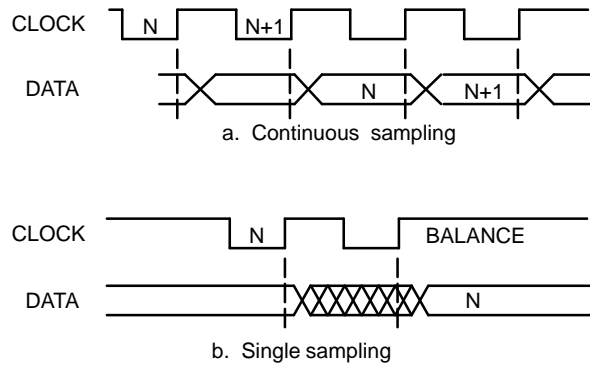
After a tester has measured all the transition voltages, the computer draws a line parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and the negative INL errors. For example, an INL error of  $-1$  to  $+2$  LSB's relative to the Ideal Line would be  $\pm 1.5$  LSB's relative to the Best Fit Line.



**Figure 7. INL Error Calculation**

## Clock and Conversion Timing

A system will clock the MP87095 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of Figure 8a shows normal operation, while the timing of Figure 8b keeps the MP87095 in balance and ready to sample the analog input.

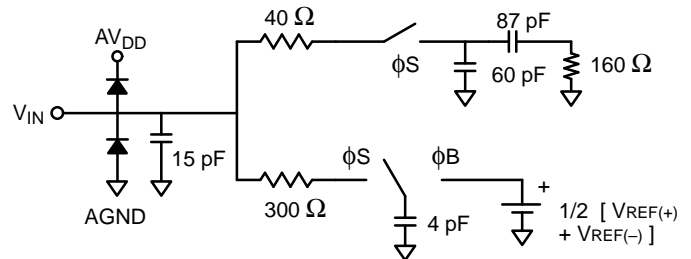


**Figure 8. Relationship of Data to Clock**

## Analog Input

The MP87095 has very flexible input range characteristics. The user may set  $V_{REF(+)}$  and  $V_{REF(-)}$  to two fixed voltages and then vary the input DC and AC levels to match the  $V_{REF}$  range. Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP87095's performance is optimized by using analog input circuitry that is capable of driving the  $A_{IN}$  input. Figure 9. shows the equivalent circuit for  $A_{IN}$ .



**Figure 9. Analog Input Equivalent Circuit**

## Reference Voltages

The input/output relationship is a function of  $V_{REF}$ :

$$\begin{aligned} A_{IN} &= V_{IN} - V_{REF(-)} \\ V_{REF} &= V_{REF(+)} - V_{REF(-)} \\ DATA &= 1023 * (A_{IN}/V_{REF}) \end{aligned}$$

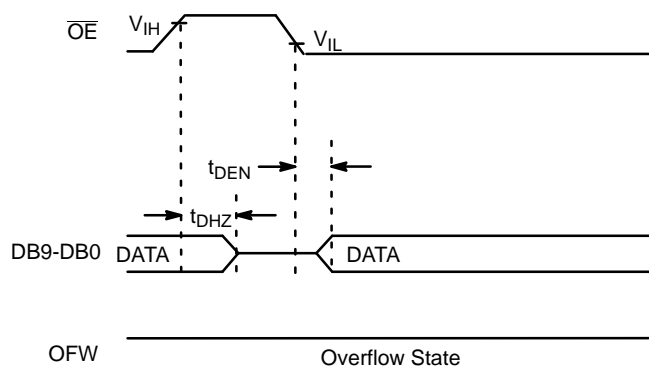
A system can increase total gain by reducing  $V_{REF}$ .

## Digital Interfaces

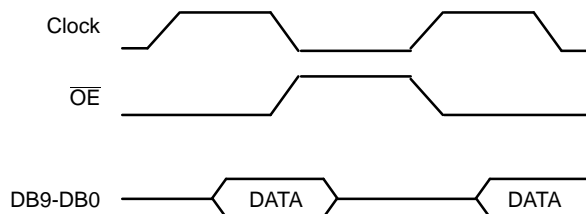
The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output. The input  $\overline{OE}$  controls the output buffers in an asynchronous mode.

$\overline{OE}$	OFW	DB9 – DB0
1	Valid	High Z
0	Valid	Valid

**Table 1. Output Enable Logic**



**Figure 10. Output Enable/Disable Timing Diagram**



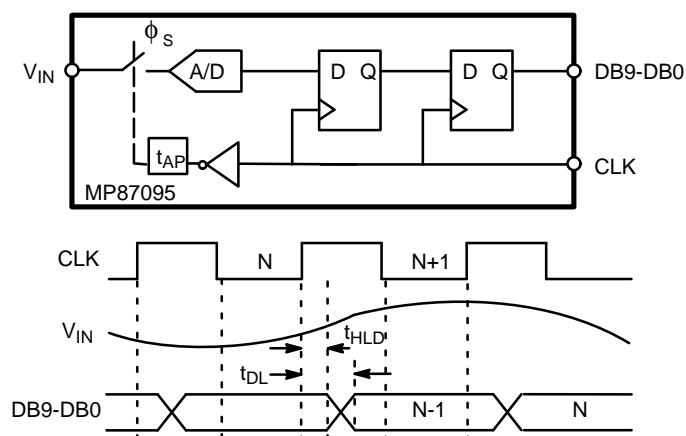
**Figure 11. Preferred Output Control**

Figure 11. shows the preferred output control where  $\overline{OE}$  and clock are opposite phase. This provides a quiet time at the end of the  $A_{IN}$  sample phase.

The functional equivalent of the MP87095 (Figure 12.) is composed of:

- 1) Delay stage ( $t_{AP}$ ) from the clock to the sampling phase ( $\phi_S$ ).
- 2) An ideal analog switch which samples  $V_{IN}$ .
- 3) An ideal A/D which tracks and converts  $V_{IN}$  with no delay.
- 4) A series of two DFF's with specified hold ( $t_{HLD}$ ) and delay ( $t_{DL}$ ) times.

$t_{AP}$ ,  $t_{HLD}$  and  $t_{DL}$  are specified in the Electrical Characteristics table.



**Figure 12. MP87095 Functional Equivalent Circuit and Interface Timing**

## Power Down

Figure 13. shows the relationship between the clock, sampled  $A_{IN}$  to output data relationship and the effect of power down.



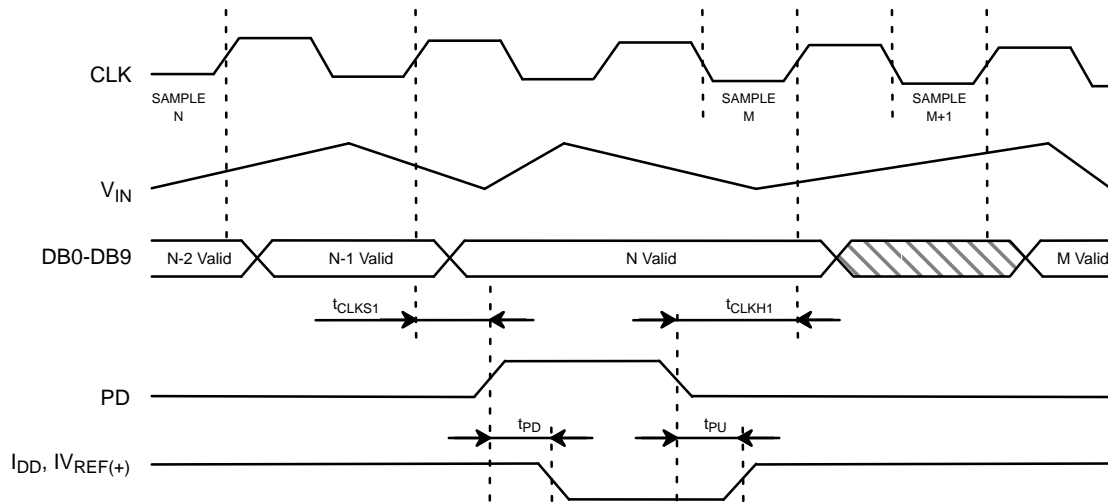
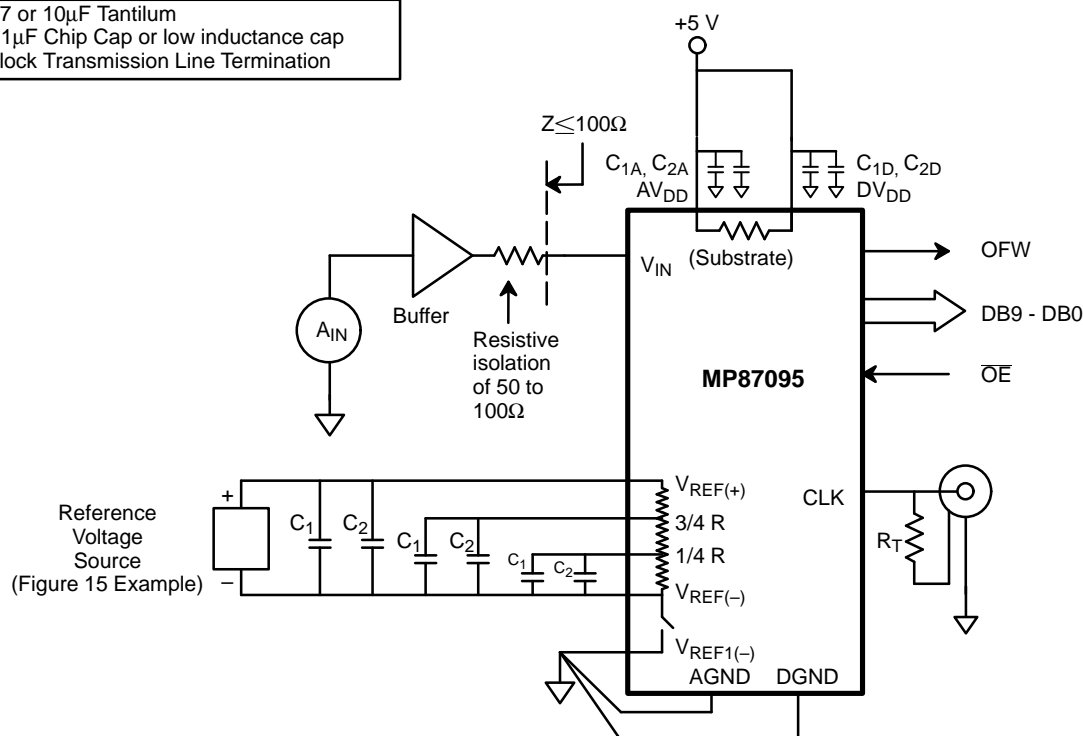


Figure 13. Power Down Timing Diagram

## APPLICATION NOTES

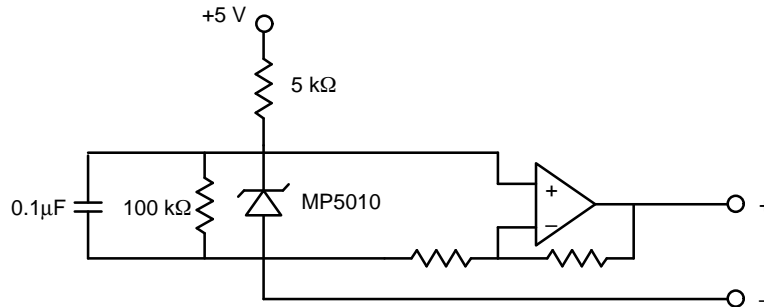
$C_1 = 4.7$  or  $10\mu\text{F}$  Tantalum  
 $C_2 = 0.1\mu\text{F}$  Chip Cap or low inductance cap  
 $R_T$  = Clock Transmission Line Termination



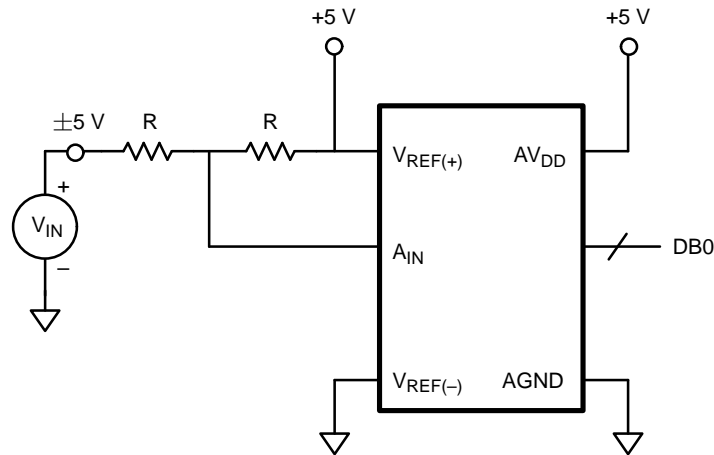
**Figure 14. Typical Circuit Connections**

The following information will be useful in maximizing the performance of the MP87095.

1. All signals should not exceed  $AV_{DD} + 0.5\text{ V}$  or  $AGND - 0.5\text{ V}$  or  $DV_{DD} + 0.5\text{ V}$ .
2. Any input pin which can see a value outside the absolute maximum ratings ( $AV_{DD}$  or  $DV_{DD} + 0.5\text{ V}$  or  $AGND - 0.5\text{ V}$ ) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP7684A inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP87095. Use of wire wrap is not recommended.
4. The analog input signal ( $V_{IN}$ ) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than  $50\Omega$ ).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths. *DGND should not be shared with other digital circuitry.* If separate low impedance paths cannot be provided, DGND should be connected to AGND next to the MP87095.
7. *DVDD should not be shared with other digital circuitry* to avoid conversion errors caused by digital supply transients.  $DV_{DD}$  for the MP87095 should be connected to  $AV_{DD}$  next to the MP87095.
8.  $DV_{DD}$  and  $AV_{DD}$  are connected inside the MP87095 through the N – doped silicon substrate. Any DC voltage difference between  $DV_{DD}$  and  $AV_{DD}$  will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic ( $0.1\mu\text{F}$ ) and a tantalum ( $10\mu\text{F}$ ) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used.  $100\Omega$  resistors in series with the digital outputs in some applications reduces the digital output disruption of  $A_{IN}$ .



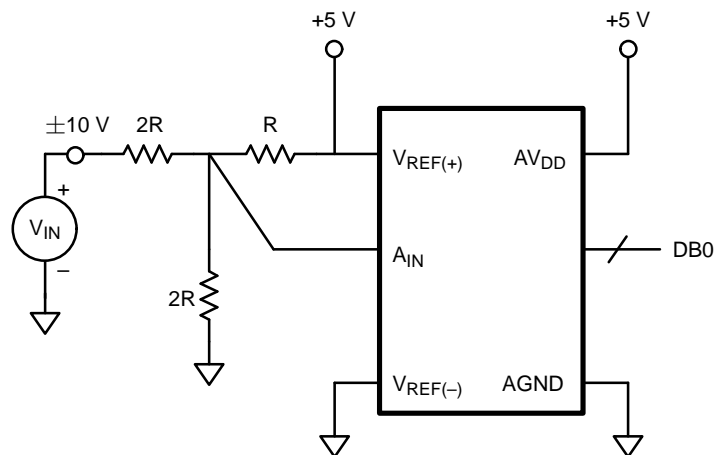
**Figure 15. Example of a Reference Voltage Source**



For  $R = 5k$  use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High  $R$  values affect the input BW of ADC due to the  $(R * C_{IN})$  of ADC time constant. Therefore, for different applications the  $R$  value needs to be selected as a tradeoff between  $A_{IN}$  settling time and power dissipation.

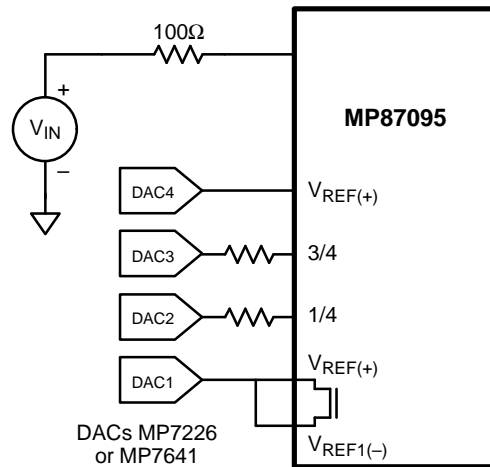
**Figure 16.  $\pm 5$  V Analog Input**



For  $R = 5k$  use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High  $R$  values affect the input BW of ADC due to the  $(R * C_{IN})$  of ADC time constant. Therefore, for different applications the  $R$  value needs to be selected as a tradeoff between  $A_{IN}$  settling time and power dissipation.

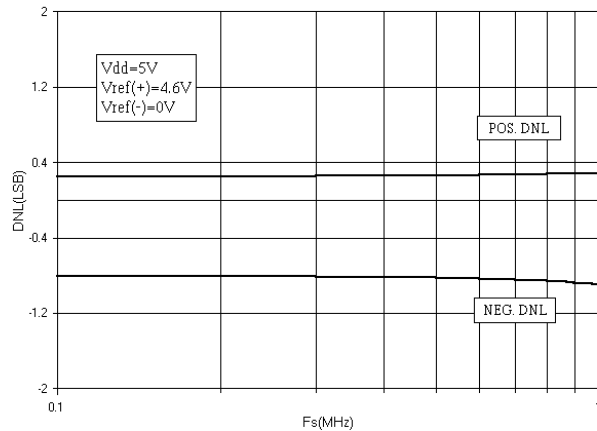
**Figure 17.  $\pm 10$  V Analog Input**



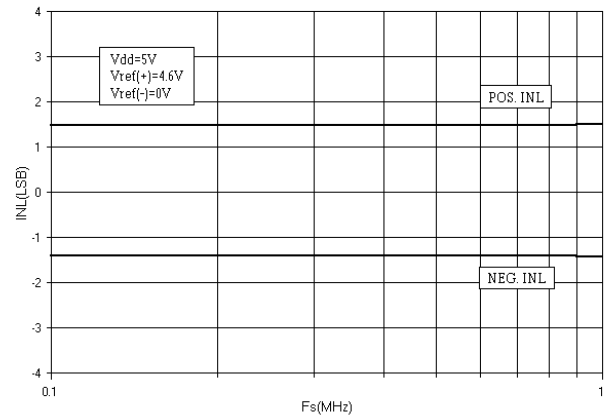
@ Power Down write values to DAC 3, 2, 1 = DAC 4 to minimize power consumption.  
Only  $A_{IN}$  and Ladder detail shown.

**Figure 18. A/D Ladder with Programmed Control  
(of  $V_{REF(+)}$ ,  $V_{REF(-)}$ , 1/4 and 3/4 TAP.)**

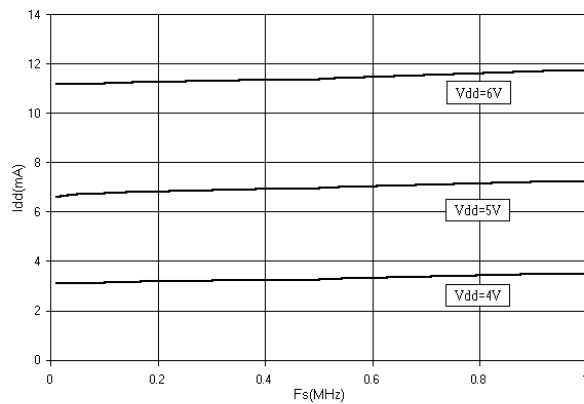
**PERFORMANCE CHARACTERISTICS**



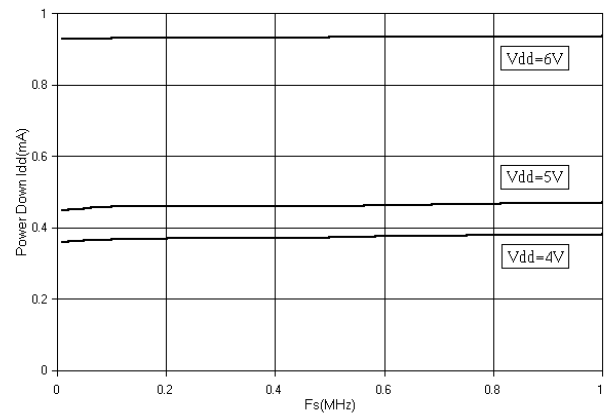
**Graph 1. DNL vs. Sampling Frequency**



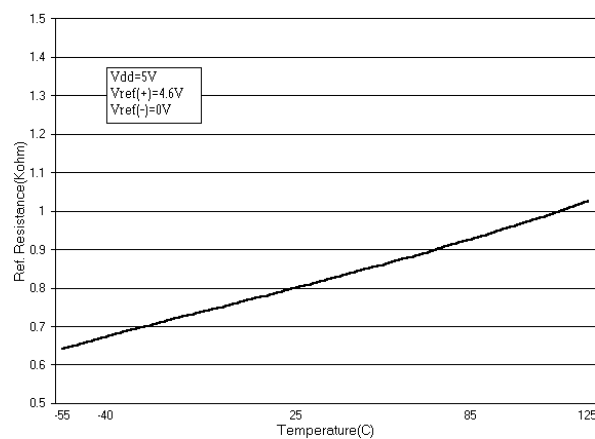
**Graph 2. INL vs. Sampling Frequency**



**Graph 3. Supply Current vs. Sampling Frequency**

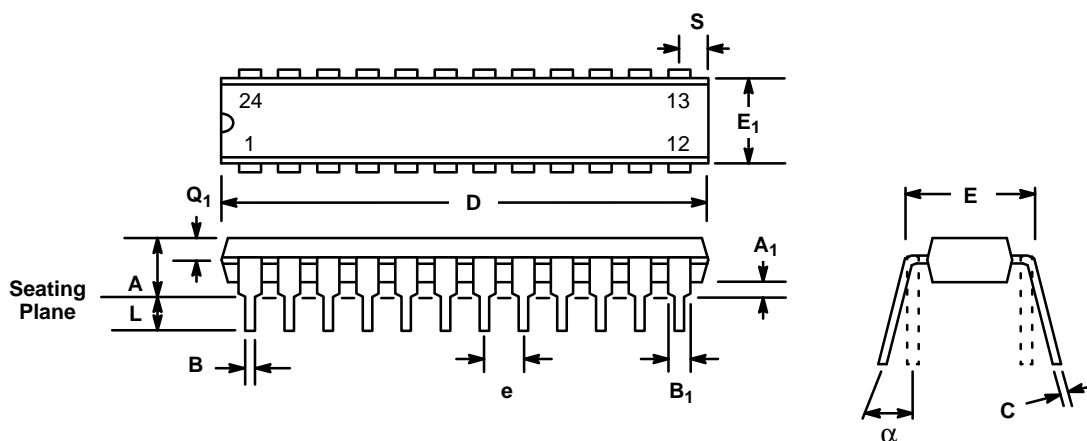


**Graph 4. Power Down Current vs. Sampling Frequency**



**Graph 5. Reference Resistance vs. Temperature**

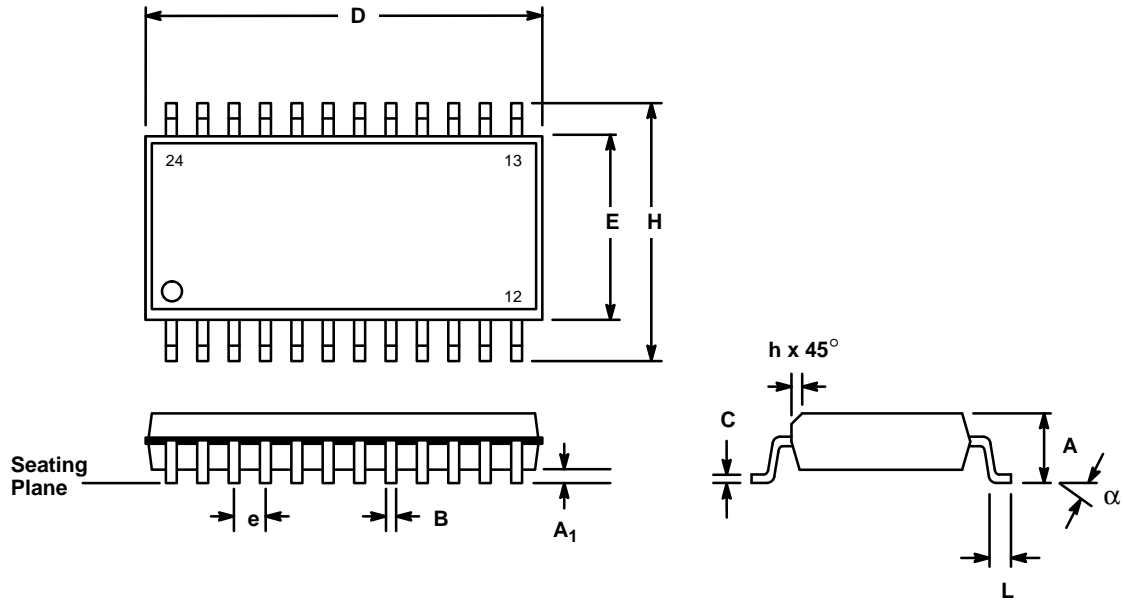
## 24 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP) NN24



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A <sub>1</sub>	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B <sub>1</sub> (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.16	1.280	29.46	32.51
E	0.295	0.325	7.49	8.26
E <sub>1</sub>	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q <sub>1</sub>	0.055	0.070	1.40	1.78
S	0.028	0.098	0.711	2.49

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

**24 LEAD SMALL OUTLINE  
(300 MIL JEDEC SOIC)  
S24**



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.642
A1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.602	0.612	15.29	15.54
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
$\alpha$	0°	8°	0°	8°

## NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contains here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Copyright 1993 EXAR Corporation

Datasheet April 1995

Reproduction, in part or whole, without the prior written consent of EXAR Corporation is prohibited.