MP87092

CMOS 750 KSPS, 12-Bit
Analog-to-Digital Converter
with Serial Logic Interface Port

FEATURES

- **12-Bit Monotonic ADC with DNL = ±1 LSB, INL = ±2 LSB**
- **SNR > 66 dB**
- **Sampling Frequency ≤ 750 kHz**
- **Internal Track and Hold**
- **Single 5 V Supply**
- **Rail-to-Rail Input Range**
- **V_{REF} Range: 1.5 V to V_{DD}**
- **CMOS Low Power: 175 mW (typ)**
- **Binary and Two's Complement Digital Output Mode**
- **Serial Port**
- **Underflow Outputs**
- **Precision Aperture Output**
- **6 Reference Resistor Taps**
- **Latch-Up Free**

APPLICATIONS

- **Control Systems**
- **Instrumentation**
- **DAS**
- **Sonar**

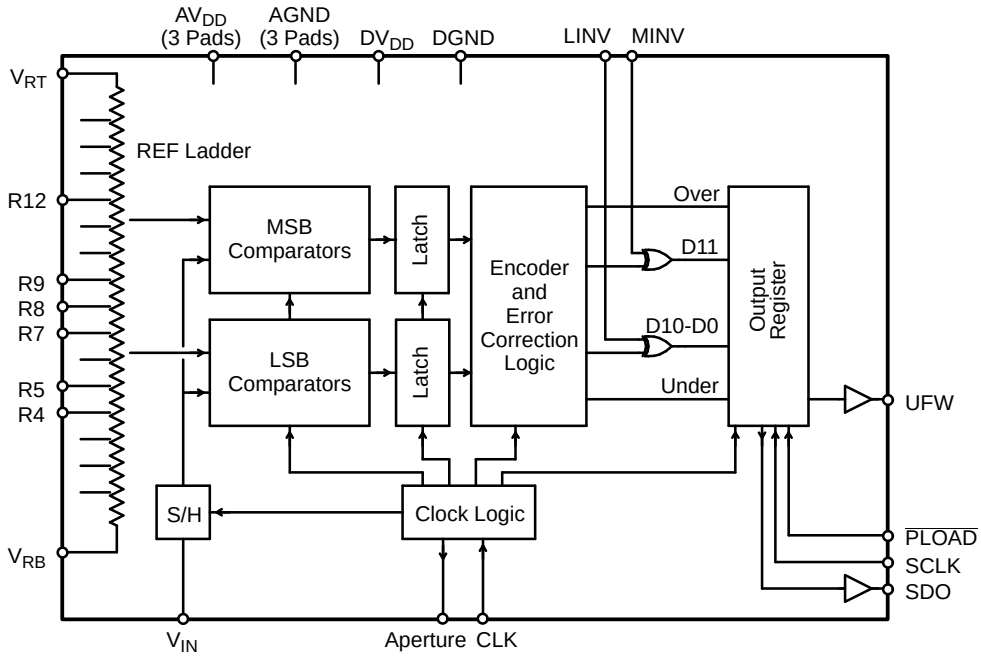
GENERAL DESCRIPTION

The MP87092 is a 12-bit 750 kHz subranging Analog-to-Digital Converter with an internal track and hold.

The MP87092 operates with a single supply ranging from +3 V to +5 V while consuming less than 175 mW of power (typical). Separate pins for V_{RT} and V_{RB} allow flexibility for analog input (V_{IN}) and the reference voltage range (ΔV_{REF}).

Data is presented at the output port every clock cycle after a 3 cycle pipeline delay. The digital output port is equipped with a serial data port. LINV and MINV enable binary and 2's complement data formatting. Access is provided to 6 ladder tap pins, providing for transfer function adjustment.

SIMPLIFIED BLOCK DIAGRAM

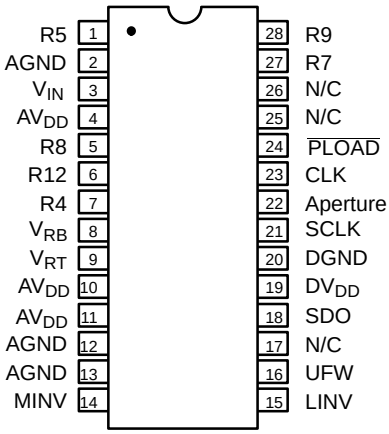


ORDERING INFORMATION

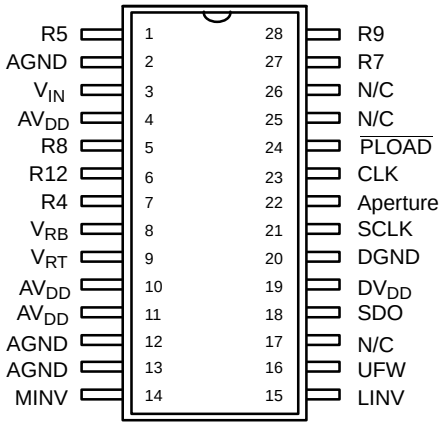
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PDIP	–40 to +85°C	MP87092AN	±1	2 1/2
SOIC	–40 to +85°C	MP87092AS	±1	2 1/2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP (0.600")
N28



28 Pin SOIC (EIAJ 0.335")
R28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	R5	Ref. Resistor Ladder Tap (5/16 V_{REF})
2	AGND	Analog Ground
3	V_{IN}	Analog Input
4	AV_{DD}	Analog Positive Supply
5	R8	Ref. Resistor Ladder Tap (1/2 V_{REF})
6	R12	Ref. Resistor Ladder Tap (3/4 V_{REF})
7	R4	Ref. Resistor Ladder Tap (1/4 V_{REF})
8	V_{RB}	Negative Reference
9	V_{RT}	Positive Reference
10	AV_{DD}	Analog Positive Supply
11	AV_{DD}	Analog Positive Supply
12	AGND	Analog Ground
13	AGND	Analog Ground
14	MINV	Invert MSB (Active High)

PIN NO.	NAME	DESCRIPTION
15	LINV	Invert LSB (Active High)
16	UFW	Underflow Bit
17	N/C	No Connection
18	SDO	Serial Data Out
19	DV_{DD}	Digital Positive Supply
20	DGND	Digital Ground
21	SCLK	Serial Clock
22	Aperture	Aperture Delay Sync
23	CLK	Clock
24	$\overline{PLOAD}$	Serial Shift Register Data Load
25	N/C	No Connection
26	N/C	No Connection
27	R7	Ref. Resistor Ladder Tap (7/16 V_{REF})
28	R9	Ref. Resistor Ladder Tap (9/16 V_{REF})

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, FS = 750 kHz (50% Duty Cycle), $V_{REF(+)}$ = 5.0 V, $V_{REF(-)}$ = AGND, TA = 25°C, V_{IN} Connected through 39Ω

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		12			Bits	
Sampling Rate	FS			750	kHz	
ACCURACY[1]						
Differential Non-Linearity	DNL		±1/2	±1	LSB	
Integral Non-Linearity (*See Graph 3.*)	INL		±2	±3	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+20		LSB	
Full Scale Error	EFS		–20		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	V_{RT}	1.5		AV_{DD}	V	
Negative Ref. Voltage	V_{RB}	AGND			V	
Differential Ref. Voltage[3]	V_{REF}	1.5		AV_{DD}	V	4.5 to 5 V is recommended for specified performance
Ladder Resistance	R_L		550		Ω	
ANALOG INPUT						
Input Bandwidth (–3 dB)[4]	BW		10		MHz	
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V p-p	
Input Capacitance Sample[5]	C_{IN}		50		pF	
Input Capacitance Convert[5]			8		pF	
Aperture Delay from Clock	t_{AP}		20		ns	
DIGITAL INPUTS						
Logical “1” Voltage	V_{IH}		2.4		V	
Logical “0” Voltage	V_{IL}		0.8		V	
Leakage Currents [6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK, MINV, LINV			10		µA	
Input Capacitance			5		pF	
Clock Timing						
Clock Period	t_S	1.33			µs	
Rise & Fall Time[7]	t_R, t_F		15		ns	
“High” Time	t_{PWH}	665			ns	
“Low” Time	t_{PWL}	665			ns	
Duty Cycle			50		%	
Serial Register Timing						
Shift Clock Period	t_{SC}	110			ns	
Shift Clock to Data Delay	t_{SD}		20		ns	
Minimum Pulse Width $\overline{PLOAD}$	t_S		50		ns	
Clock↑ to $\overline{PLOAD}$↓ For Valid D11	t_{CP}		0		ns	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical “1” Voltage	V_{OH}		DV_{DD}-0.5		V	I_{LOAD} = 4 mA
Logical “1” Source Current	I_{OH}		4		mA	V_{OH} = DV_{DD}-0.5
Logical “0” Voltage	V_{OL}		0.5		V	I_{LOAD} = 4 mA
Logical “0” Sink Current	I_{OL}		4		mA	V_{OL} = 0.5 V
Tristate Leakage	I_{OZ}		1		µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay[2]	t_{DL}		30		ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
POWER SUPPLIES[8]						
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}		5		V	
Current (AV_{DD} + DV_{DD})	I_{DD}		35	45	mA	
AC PARAMETERS						
Signal Noise Ratio	SNR	66			dB	V_{IN} = 5 Vp-p, 1 kHz

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/4096) is the DNL error. The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage. Accuracy is a function of the sampling rate (FS).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 –3 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.

5 A 39Ω resistor should be put in series with V_{IN} to dampen transients associated with inductive output impedance of typical op amps.

6 All inputs have diodes to DV_{DD} and DGND. Input(s) MINV and LINV have internal pull down(s). Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.

7 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.

8 AGND & DGND pins are internally connected through the silicon substrate.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 7 V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND –0.5 V
All Inputs ..... V_{DD} +0.5 to GND –0.5 V
Digital Outputs ..... V_{DD} +0.5 to GND –0.5 V
Storage Temperature ..... –65 to +150°C

Lead Temperature (Soldering 10 seconds) ..... +300°C

Package Power Dissipation Rating @ 75°C
PDIP. SOIC 1000mW
Derates above 75°C ..... 14mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

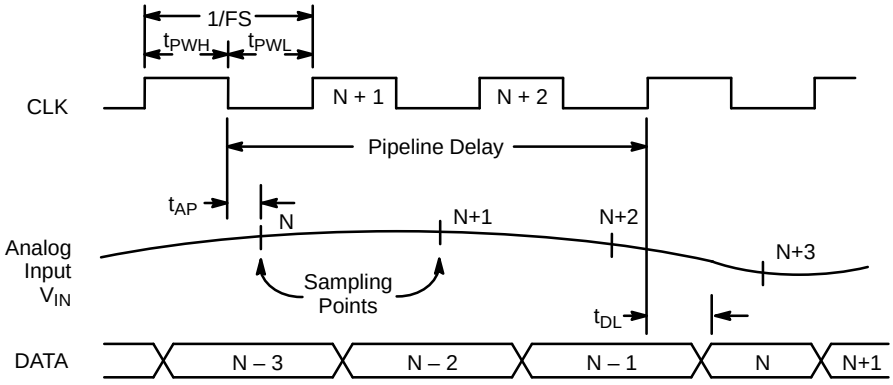
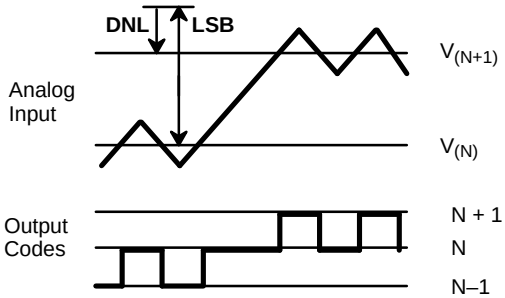


Figure 1. MP87092 Timing Diagram



Code Width (N) = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{RT} - V_{RB}$] / 4096

$DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - LSB$

Figure 2. DNL Measurement

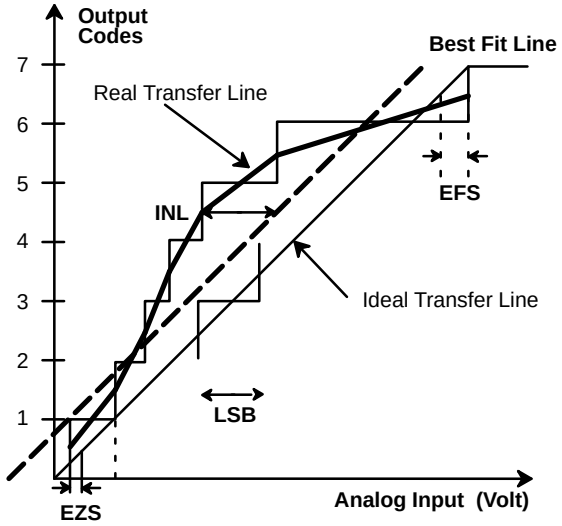


Figure 3. INL Error Calculation

UFW: Underflow (Output)

This signal indicates when the Analog Input (V_{IN}) goes outside the V_{RB} range, and is normally at a low logic level. When $V_{IN} < V_{RB}$, UFW will go high and the data bits will show negative full scale (i.e. all 0's if MINV & LINV are low).

SDO: Serial Data output

After the internal shift register is updated using the $\overline{\text{PLOAD}}$ signal, the SDO pin outputs the A/D result starting with the MSB (which appears just after the $\overline{\text{PLOAD}}$ strobe). Each bit is output on the rising edge of SCLK.

SCLK: Serial Data Port Clock

The SCLK controls the output of the serial port through SDO. SDO is updated on every rising edge of SCLK. The $\overline{\text{PLOAD}}$ signal will override the SCLK signal.

$\overline{\text{PLOAD}}$:

Serial data port shift register load: When $\overline{\text{PLOAD}}$ is low (i.e. level triggered not edge triggered) the current parallel data will be loaded into the shift register. $\overline{\text{PLOAD}}$ overrides SCLK. When $\overline{\text{PLOAD}}$ is high, the data can be shifted out through the SDO pin with SCLK.

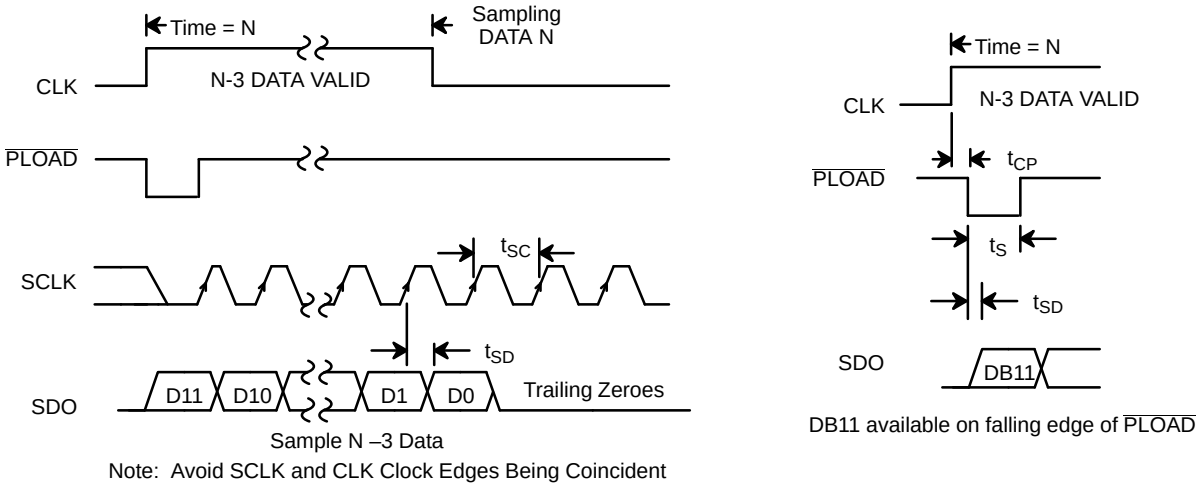


Figure 4. Serial Port Timing Chart

APERTURE: Aperture Delay Sync (output)

This signal is high when the internal sample/hold function is sampling V_{IN}, and goes low when it is in the hold mode (when the ADC is comparing the stored input value to the reference ladder). The value of V_{IN} at the high to low transition of APERTURE is the value that will be digitized. A system can monitor this signal and adjust the CLK to accurately synchronize the sampling point to an external event.

MINV LINV	0 0	0 1	1 0	1 1
V_{RT}	111 . . . 11 111 . . . 10	100 . . . 00 100 . . . 01	011 . . . 11 011 . . . 10	000 . . . 00 000 . . . 01
V_{IN} mid scale	100 . . . 01 100 . . . 00	111 . . . 10 111 . . . 11	000 . . . 01 000 . . . 00	011 . . . 10 011 . . . 11
	011 . . . 11	000 . . . 00	111 . . . 11	100 . . . 00
V_{RB}	000 . . . 01 000 . . . 00	011 . . . 10 011 . . . 11	100 . . . 01 100 . . . 00	111 . . . 10 111 . . . 11
	binary	inverted 2's complement	2's complement	inverted binary

Table 1. Output Data Format Truth Table

MINV & LINV: Digital Output Format (inputs)

These signals control the format of the digital output data bits DB0 – DB11. Normally both pins are held low so the data is in straight binary format (all 0's when V_{IN}=V_{RB}; all 1's when V_{IN}=V_{RT}). If MINV is pulled high then the MSB (DB11) will be inverted. If LINV is pulled high then the LSBs (DB0 – DB10) will be inverted. The OFW and UFW bits are not affected by these signals.

MINV & LINV are meant to be static digital signals. If they are to change during operation they should only change when the CLK is low (assuming PHASE is high, if PHASE is low then these signals should only change when CLK is high). Changing MINV and/or LINV on the wrong phase of the CLK will not hurt anything, but the effects on the digital outputs will not be seen until the output latch of the output register is enabled. MINV and LINV have internal pull down devices. Please see the simplified logic circuit *NO TAG*

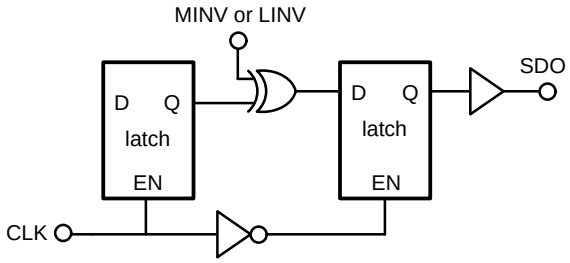


Figure 5. MINV, LINV Simplified Logic Circuit

V_{IN} Analog Input

This part has a switched capacitor type input circuit. This means that the input impedance changes with the phase of the input clock. V_{IN} is sampled at the high to low clock transition. The diagram *NO TAG* shows an equivalent input circuit.

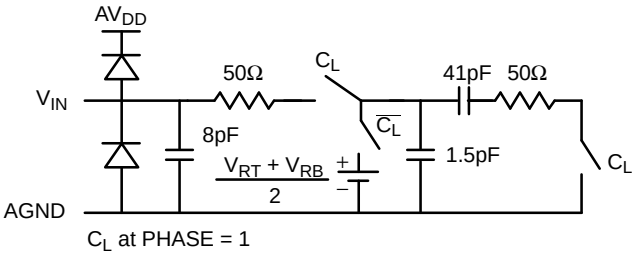


Figure 6. Equivalent Input Circuit

Reference Ladder Taps

These taps connect to every sixteenth point along the reference ladder; R4 is 4/16th up from V_{RB}, R7 is 7/16ths up from V_{RB}. These taps can be used to alter the transfer curve of the ADC. The internal interconnect resistance from the pin to the ladder is less than 3Ω for the even numbered taps, (i.e. R4,R6, etc.) and is approximately 10Ω for the odd numbered taps.

Altering the transfer curve may be desirable to enhance or minimize the probability of codes for a certain range of V_{IN}.

Sometimes this is referred to as probability density function shaping, or histogram shaping.

0.8 V maximum per tap is recommended for applications above 85°C. Up to 1.6 V is allowed for applications under 85°C.

APPLICATION NOTES

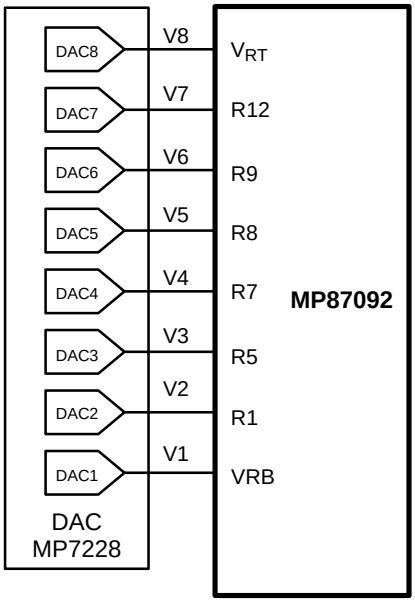
V_{IN} signals should not exceed AV_{DD} +0.5V or go below AGND –0.5V. All pins have internal protection diodes that will protect them from short transients (<100µs) outside the supply range.

AGND and DGND pins are connected internally through the P– substrate. DC voltage differences between any AGND or DGND pins will cause undesirable internal substrate currents.

The power supply (V_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to AGND, placed as close to the chip as possible.

The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

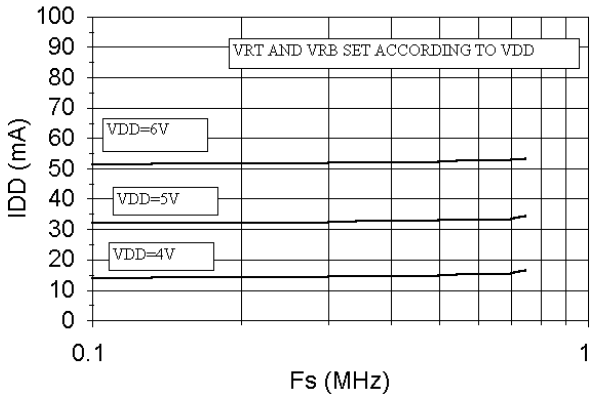
The reference tap pins (R1-R12) can be used to create piecewise-linear transfer functions. By forcing voltages on these pins, an 8 segment transfer function can be made. See *NO TAG*



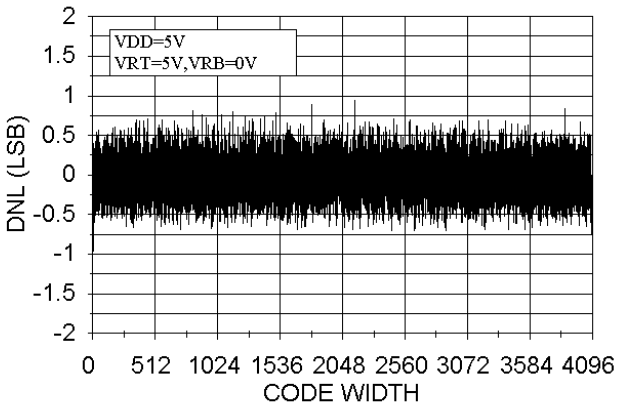
Only the Ladder detail shown.

Figure 7. A/D with Programmed Ladder Control for Creating a Piecewise Linear Transfer Function

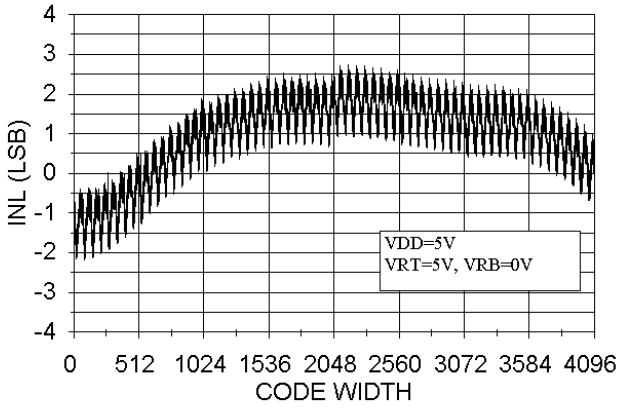
PERFORMANCE CHARACTERISTICS



Graph 1. I_{DD} vs. F_S

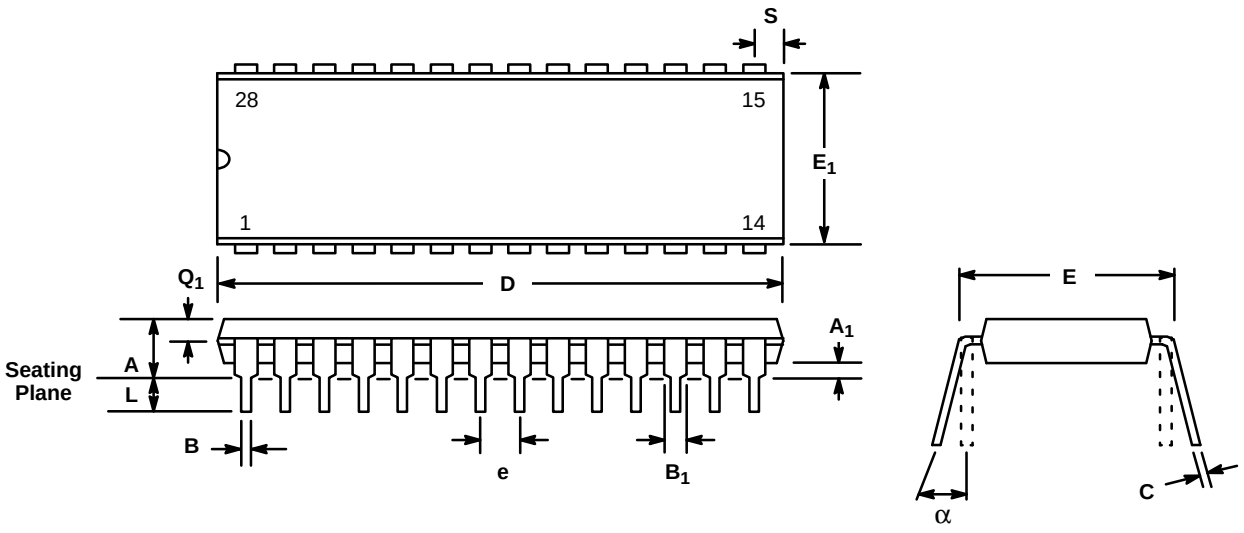


Graph 2. DNL Error Plot



Graph 3. INL Error Plot

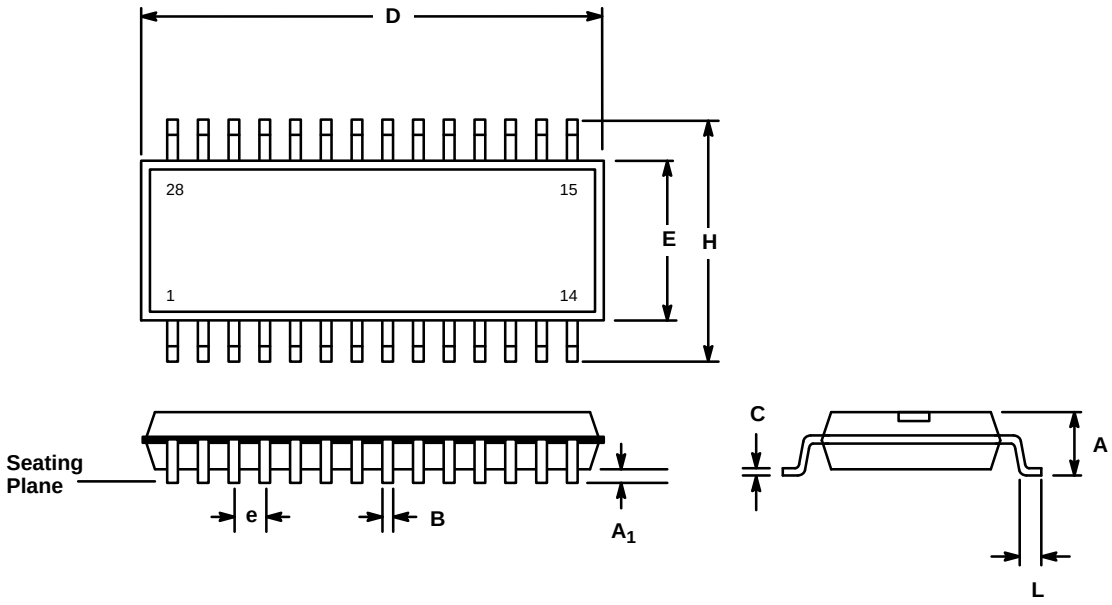
28 LEAD PLASTIC DUAL-IN-LINE
(600 MIL PDIP)
N28



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.232	—	5.893
A_1	0.015	—	0.381	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.380	1.490	35.05	37.85
E	0.585	0.625	14.86	15.88
E_1	0.500	0.610	12.70	15.49
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.020	0.100	1.508	2.54

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

28 LEAD SMALL OUTLINE
(335 MIL EIAJ SOIC)
R28



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.60	2.80	0.102	0.110
A_1	0.2 (typ.)		0.008 (typ.)	
B	0.3	0.5	0.012	0.020
C	0.10	0.20	0.004	0.008
D	17.6	18.0	0.693	0.709
E	8.3	8.5	0.327	0.335
e	1.27 (typ.)		0.050 (typ.)	
H	11.5	12.1	0.453	0.477
L	0.8	1.2	0.031	0.047

Notes

NOTICE

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