MP87091

CMOS 750 KSPS, 12-Bit
Analog-to-Digital Converter
with Parallel Logic Interface Port

FEATURES

- 12-Bit Monotonic ADC
- SNR > 66 dB
- Sampling Frequency $\leq$ 750 kHz
- Internal Track and Hold
- Single 5 V Supply
- Rail-to-Rail Input Range
- DNL = $\pm$1 LSB, INL = $\pm$2 LSB
- V_{REF} Range: 1.5 V to V_{DD}
- CMOS Low Power: 175 mW (typ)
- 1/4, 1/2 and 3/4 Scale Reference Resistor Taps
- Three-State Outputs
- Binary and Two's Complement Digital Output Mode
- Latch-Up Proof

APPLICATIONS

- Control Systems
- Instrumentation
- DAS
- Sonar

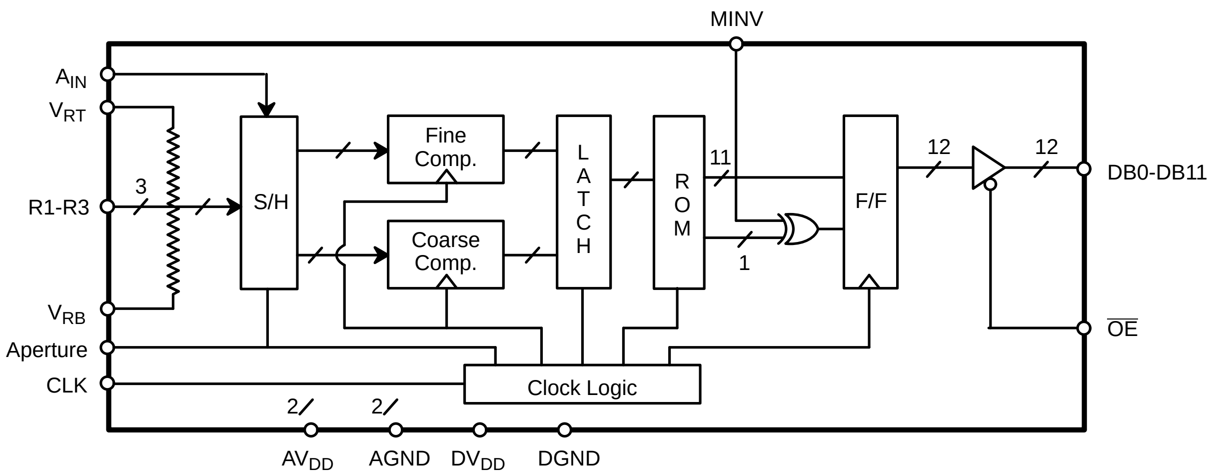
GENERAL DESCRIPTION

The MP87091 is a 750 kHz 12-bit subranging Analog-to-Digital Converter with an an internal track and hold.

The MP87091 operates with a single 5 V supply while consuming less than 175 mW of power (typical). Separate pins for V_{RT} and V_{RB} allow flexibility for various A_{IN} and ΔV_{REF}.

Data is presented at the parallel output port every clock cycle after a 2.5 cycle pipeline delay from sample edge. The digital output port is also equipped with a three-state function. MINV enables binary and 2's complement data formatting. Through pins R1-R3, transfer function adjustment, linearity, and speed enhancement can be accommodated.

SIMPLIFIED BLOCK DIAGRAM

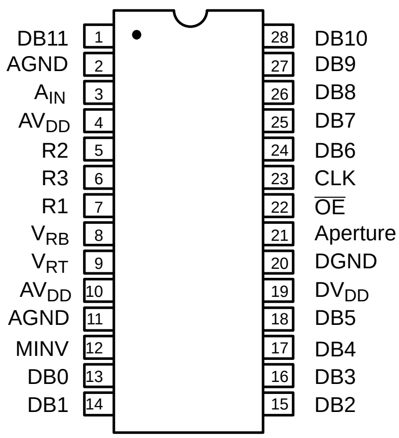


ORDERING INFORMATION

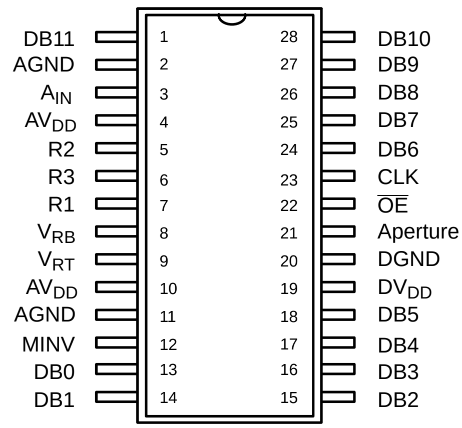
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PDIP	–40 to +85°C	MP87091AN	±1	2 1/2
SOIC	–40 to +85°C	MP87091AS	±1	2 1/2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP (0.600")
N28



28 Pin SOIC (EIAJ, 0.335")
R28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB11	Data Output Bit 11 (MSB)
2	AGND	Analog Ground
3	A_{IN}	Analog Input
4	AV_{DD}	Analog Power Supply
5	R2	Ref. Resistor Ladder Tap (1/2 V_{REF})
6	R3	Ref. Resistor Ladder Tap (3/4 V_{REF})
7	R1	Ref. Resistor Ladder Tap (1/4 V_{REF})
8	V_{RB}	Bottom Reference
9	V_{RT}	Top Reference
10	AV_{DD}	Analog Power Supply
11	AGND	Analog Ground
12	MINV	Invert MSB (Active High)
13	DB0	Data Output Bit 0 (LSB)
14	DB1	Data Output Bit 1

PIN NO.	NAME	DESCRIPTION
15	DB2	Data Output Bit 2
16	DB3	Data Output Bit 3
17	DB4	Data Output Bit 4
18	DB5	Data Output Bit 5
19	DV_{DD}	Digital Power Supply
20	DGND	Digital Ground
21	Aperture	Delayed Clock, indicates sample point
22	$\overline{OE}$	Output Enable (Active Low)
23	CLK	Clock
24	DB6	Data Output Bit 6
25	DB7	Data Output Bit 7
26	DB8	Data Output Bit 8
27	DB9	Data Output Bit 9
28	DB10	Data Output Bit 10

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD}$ = 5 V, FS = 750 kHz (50% Duty Cycle),
V_{RT} = 5.0 V, V_{RB} = AGND, TA = 25°C, A_{IN} Connected through 39Ω, Aperture Connected to $\overline{OE}$

Parameter	Symbol	25°C Min	Typ	Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		12			Bits	
Sampling Rate	FS			750	kHz	For rated accuracy
ACCURACY[1]						
Differential Non-Linearity	DNL			$\pm$1	LSB	
Integral Non-Linearity	INL			2 1/2	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+20		LSB	
Full Scale Error	EFS		–20		LSB	
REFERENCE VOLTAGES						
Top Ref. Voltage	V_{RT}	1.5		AV_{DD}	V	
Bottom Ref. Voltage	V_{RB}	AGND			V	
Differential Ref. Voltage[3]	V_{REF}	1.5		AV_{DD}	V	
Ladder Resistance	R_L		550		Ω	
ANALOG INPUT						
Input Bandwidth (–3 dB)[4]	BW		10		MHz	
Input Voltage Range	A_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V p-p	
Input Capacitance Sample[5]	C_{IN}		50		pF	
Input Capacitance Convert[5]			8		pF	
Aperture Delay from Clock	t_{AP}		35		ns	
Aperture Delay from Aperture Signal			0		ns	Aperture pin load 5 pF. Measured at 50% point.
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}		2.4		V	
Logical "0" Voltage	V_{IL}		0.8		V	
Leakage Currents [6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK, $\overline{OE}$, MINV			10		µA	
Input Capacitance			5		pF	
Clock Timing						
Clock Period	t_S	1000	1333		ns	Functional
Rise & Fall Time[7]	t_R, t_F		15		ns	
"High" Time	t_{PWH}	500	667		ns	
"Low" Time	t_{PWL}	500	667		ns	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}		DV_{DD}-0.5		V	I_{LOAD} = 4 mA
Logical "0" Voltage	V_{OL}			0.5	V	I_{LOAD} = 4 mA
Three-State Leakage	I_{OZ}		1		µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay	t_{DL}		30		ns	
Data Enable Delay	t_{DEN}		25		ns	
Data Three-State Delay	t_{DHZ}		25		ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	Min (25°C)	Typ (25°C)	Max (25°C)	Units	Test Conditions/Comments
POWER SUPPLIES[8] **(Tmin to Tmax)**						
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}		5		V	
Current (AV_{DD} + DV_{DD})	I_{DD}			45	mA	
AC PARAMETERS						
Signal Noise Ratio	SNR	66			dB	A_{IN} = 5 V p-p, 1 kHz

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/4096) is the DNL error. The INL error is the maximum distance (in LSB's) from the best fit line to any transition voltage. Accuracy is a function of the sampling rate (FS).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 –3 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.

5 A 39 Ω resistor should be put in series with A_{IN} to dampen transients with inductive output impedance of typical op amps.

6 All inputs have diodes to V_{DD} and GND. Input(s) $\overline{OE}$ and MINV have internal pull down(s). Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.

7 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.

8 AGND & DGND pins are connected through the silicon substrate.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND . . . . 7 V
V_{RT} & V_{RB} . . . . V_{DD} +0.5 to GND –0.5 V
A_{IN} . . . . V_{DD} +0.5 to GND –0.5 V
All Inputs . . . . V_{DD} +0.5 to GND –0.5 V
All Outputs . . . . V_{DD} +0.5 to GND –0.5 V

Storage Temperature . . . . –65 to +150°C
Lead Temperature (Soldering 10 seconds) . . . . +300°C
Package Power Dissipation Rating @ 75°C
PDIP, SOIC 450mW
Derates above 75°C . . . . 6mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

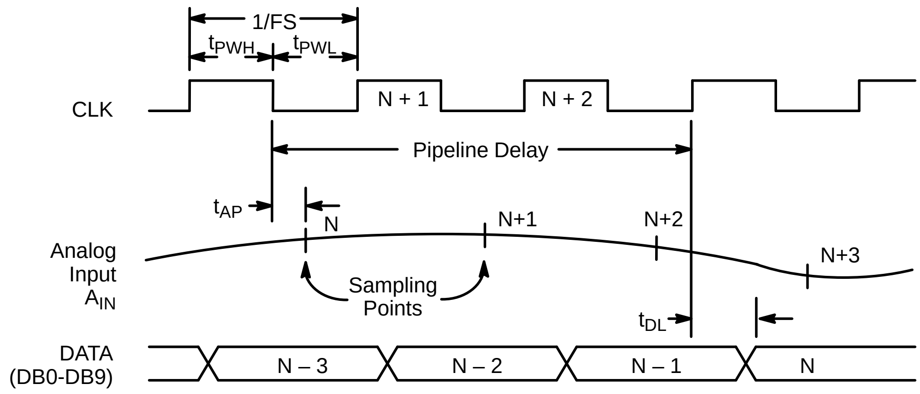


Figure 1. Timing Diagram

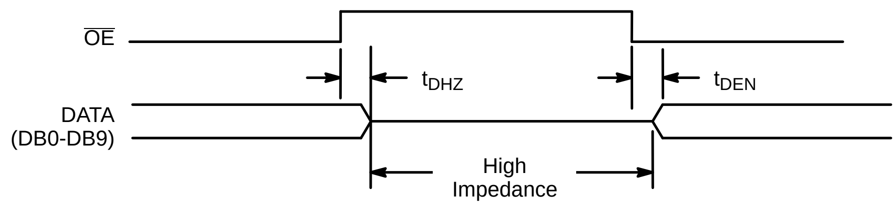


Figure 2. Three-State Timing Diagram

OVERVIEW OF THE MP87091 OPERATION

$\overline{OE}$: Output Enable (input)

This signal controls the 3-state drivers on the digital outputs DB0 - DB11. During normal operation $\overline{OE}$ should be held low so that all outputs are enabled (NOTE: an internal resistor will pull $\overline{OE}$ to this level if it is not connected). When $\overline{OE}$ is driven high DB0 - DB11 go into the high impedance mode. This control operates asynchronously to the clock and only controls the output drivers. The internal output register will get updated if the clock is running while the outputs are in 3-state mode. If possible, $\overline{OE}$ should be in three-state during Clock = 1 to reduce digital noise coupling into A_{IN} during the sample time. Aperture provides a convenient control for this purpose since it guarantees that the A_{IN} sample period is complete when the outputs are enabled.

APERTURE: Aperture Delay Sync (Output)

This signal is high when the internal sample/hold function is sampling V_{IN}, and goes low when it is in the hold mode (when the ADC is comparing the stored input value to the reference ladder). The value of V_{IN} at the high to low transition of APERTURE is the value that will be digitized. A system can monitor this signal and adjust the CLK to accurately synchronize the sampling point to an external event. The Aperture pin may also be used to control the $\overline{OE}$ (outputs between three-state and active mode). This will reduce the errors introduced by digital output coupling during the A_{IN} sample time. Specifications are based on this connection.

MINV: Digital Output Format (input).

This signal controls the format of the digital output data bits DB0 – DB11. Normally it is held low so the data is in straight binary format (all 0's when $V_{IN} = V_{RB}$; all 1's when $V_{IN} = V_{RT}$). If MINV is pulled high then the MSB (DB11) will be inverted.

MINV is meant to be a static digital signal. If it is to change during operation it should only change when the CLK is low. Changing MINV on the wrong phase of the CLK will not hurt anything, but the effects on the digital outputs will not be seen until the output latch of the output register is enabled. MINV has a internal pull down device.

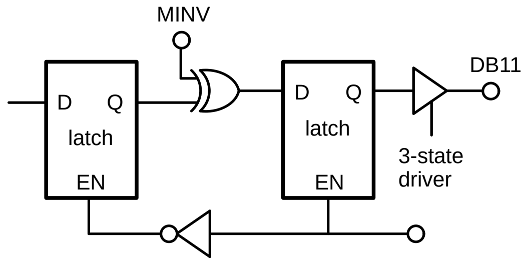


Figure 3. MINV Simplified Logic Circuit

A_{IN} Analog Input

A 50 to 75Ω resistor in series with this pin will minimize A_{IN} interaction with the signal source.

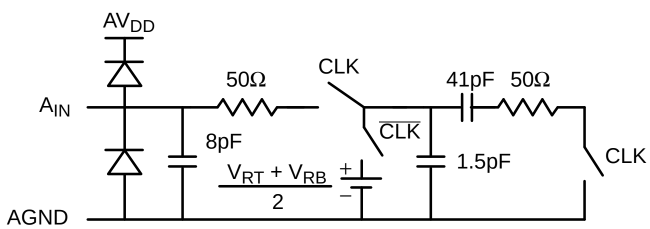


Figure 4. Equivalent Input Circuit

R1, R2, R3: Reference Ladder Taps.

These taps connect to every 1/4 point along the reference ladder; R1 is 1/4th up from V_{RB}, R3 is 3/4ths up from V_{RB} (or 1/4th down from V_{RT}). Normally these pins should have 0.1 microfarad capacitors to GND, this helps reduce the INL errors by stabilizing the reference ladder voltages.

These taps can also be used to alter the transfer curve of the ADC. A 4 segment, piecewise linear, custom transfer curve can be designed by connecting voltage sources to these pins.

This may be desirable to make the probability of codes for a certain range of V_{IN} be enhanced or minimized.

Sometimes this is referred to as probability density function shaping, or histogram shaping.

The internal interconnect resistance from each of the tAP pins to the ladder is less than 3Ω.

1.6V maximum per tap is recommended for applications above 85°C. Up to 3.2V is allowed for applications under 85°C.

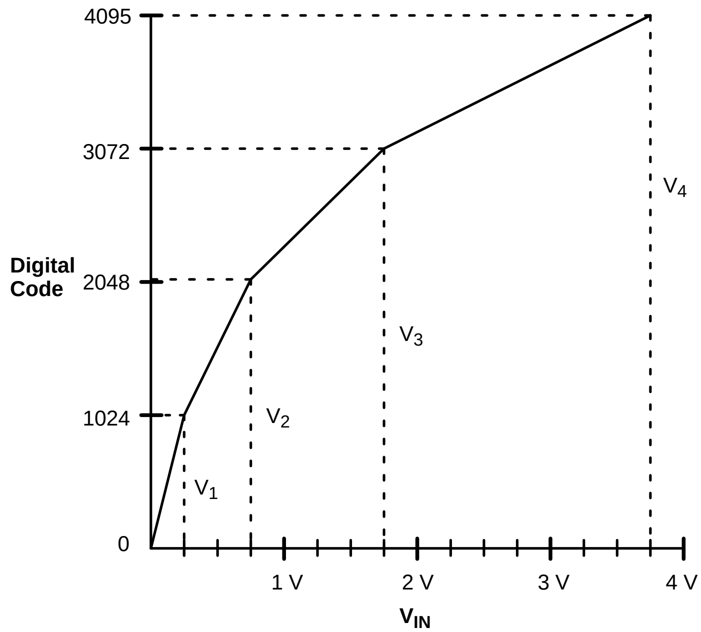
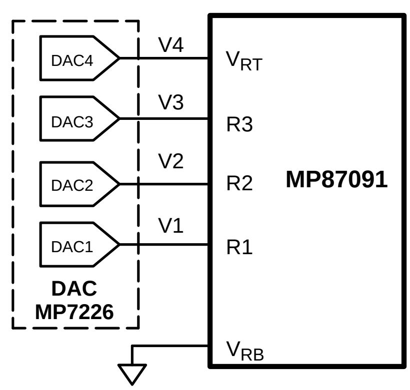


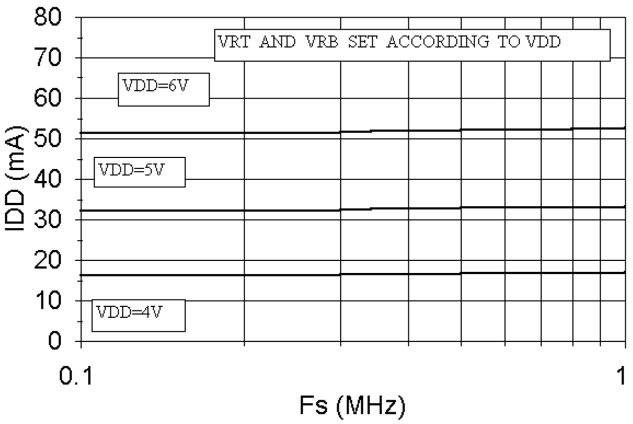
Figure 5. A Piecewise Linear Transfer Function



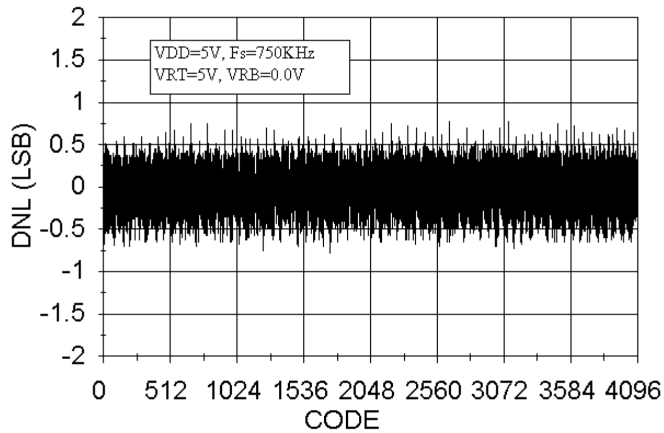
Only the Ladder detail shown.

Figure 6. A/D with Programmed Ladder Control for Creating a Piecewise Linear Transfer Function

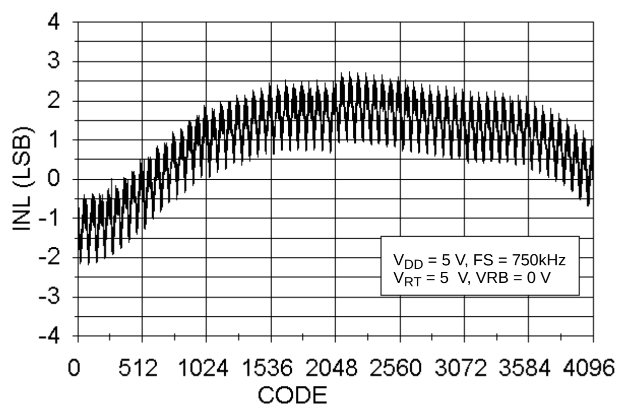
PERFORMANCE CHARACTERISTICS



Graph 1. I_{DD} vs. F_S

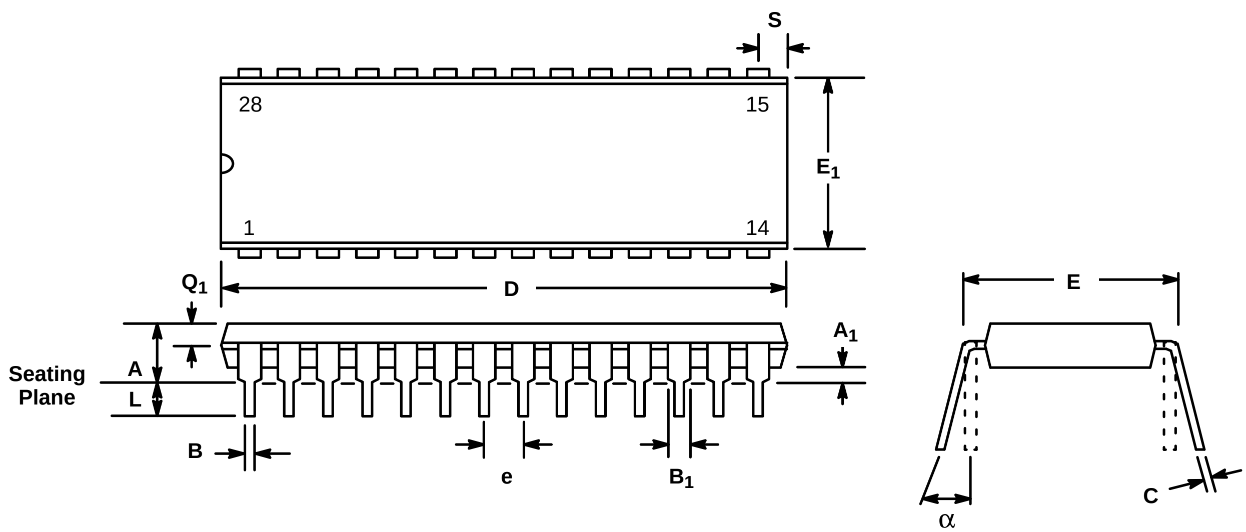


Graph 2. DNL Error Plot



Graph 3. INL Error Plot

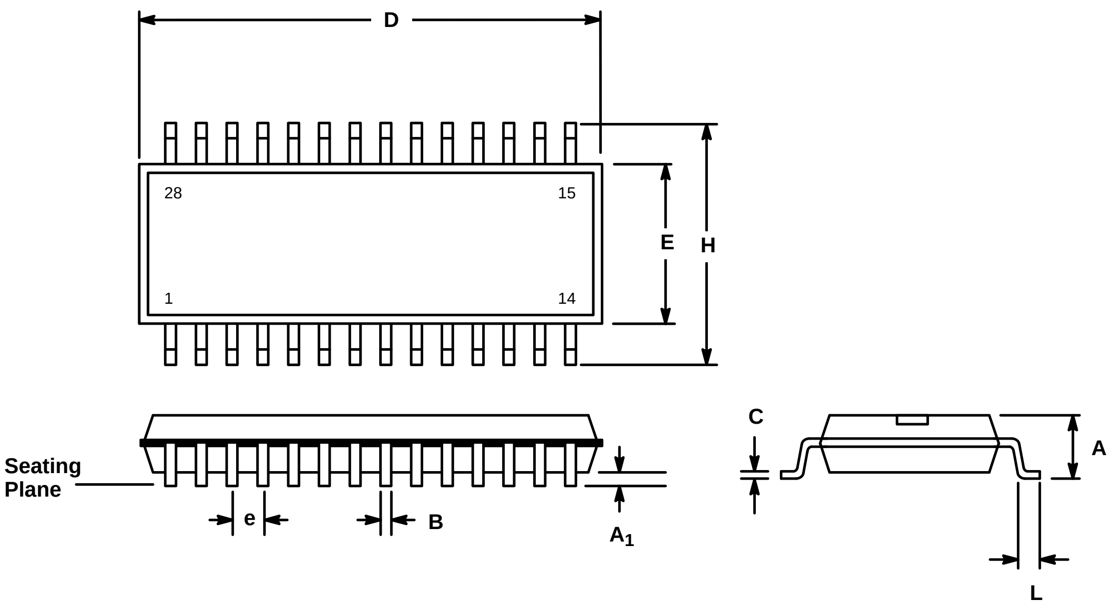
28 LEAD PLASTIC DUAL-IN-LINE
(600 MIL PDIP)
N28



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	—	0.232	—	5.893
A_1	0.015	—	0.381	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.380	1.490	35.05	37.85
E	0.585	0.625	14.86	15.88
E_1	0.500	0.610	12.70	15.49
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.020	0.100	1.508	2.54

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

28 LEAD SMALL OUTLINE
(335 MIL EIAJ SOIC)
R28



SYMBOL	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.60	2.80	0.102	0.110
A_1	0.2 (typ.)		0.008 (typ.)	
B	0.3	0.5	0.012	0.020
C	0.10	0.20	0.004	0.008
D	17.6	18.0	0.693	0.709
E	8.3	8.5	0.327	0.335
e	1.27 (typ.)		0.050 (typ.)	
H	11.5	12.1	0.453	0.477
L	0.8	1.2	0.031	0.047

Notes

Notes

NOTICE