MP7783

CMOS
Low Power 8-Bit
Analog-to-Digital Converter

FEATURES

- **Sampling Rates up to 3 MHz**
- **Requires NO SAMPLE AND HOLD for CCD Outputs or for Signals less than 100 kHz**
- **Single Supply Voltage**
- **Low Power Consumption (100 mW typ)**
- **Latch-Up Free**

APPLICATIONS

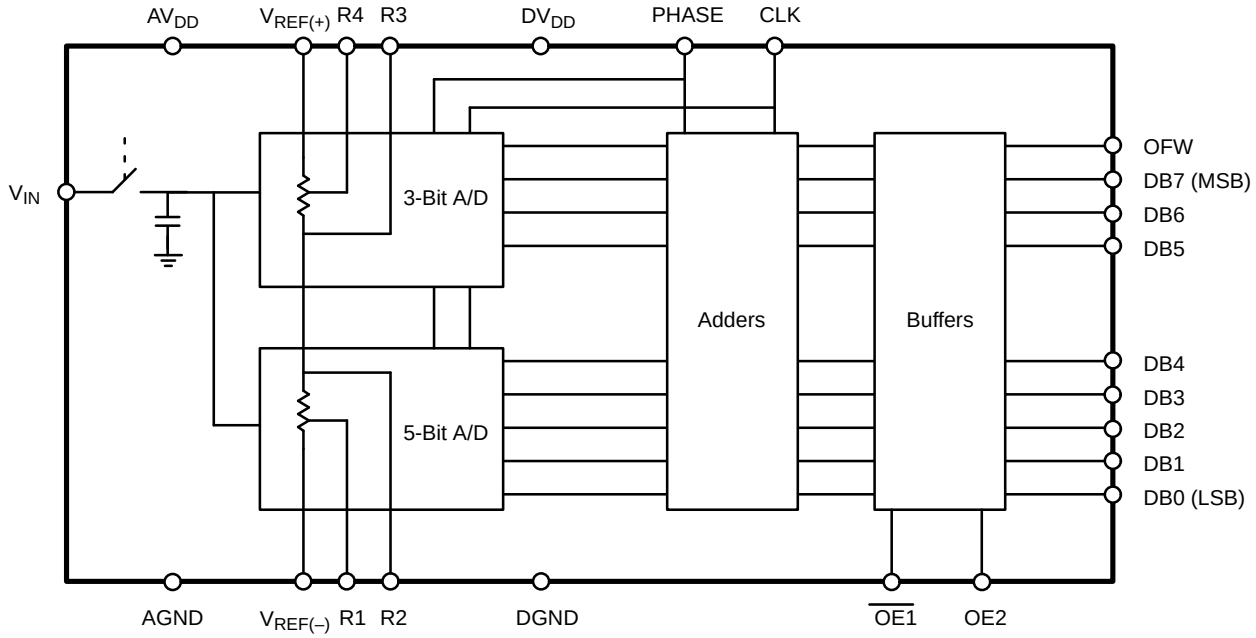
- **Data Acquisition Systems**
- **Computer Peripherals**
- **Scanners**
- **Process Control**

GENERAL DESCRIPTION

The MP7783 is a CMOS 8-Bit two step Analog-to-Digital Converter designed for precision applications requiring conversion times under a micro-second. Featuring a built in Track and Hold function, input signals to 100 kHz can be digitized with confidence. Integral and differential non-linearities are typically less than 1/4 LSB, with a clock frequency of 2 MHz and a supply of 5 volts.

Built on EXAR's proprietary CMOS technology, the conversion is done in two segments. The first segment converts the 3 MSBs while the second segment converts the five LSBs. An overflow bit is provided for applications requiring 9-bit resolution by using two devices in cascade.

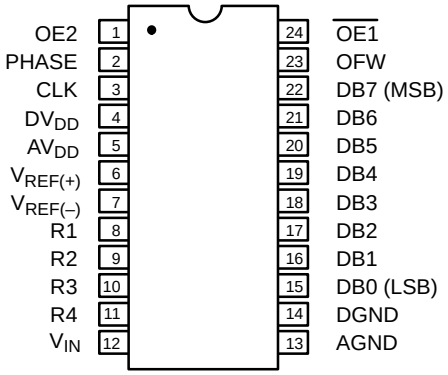
SIMPLIFIED BLOCK DIAGRAM



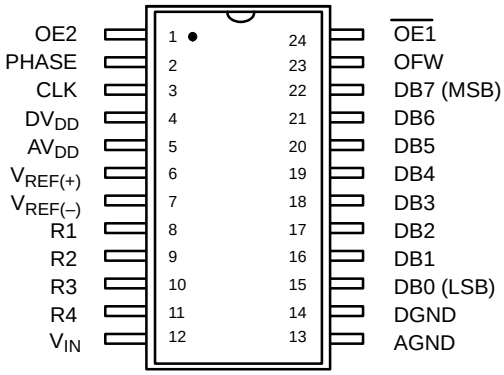
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP7783JN	±3/4	±3/4
SOIC	–40 to +85°C	MP7783JS	±3/4	±3/4

PIN CONFIGURATIONS



24 Pin PDIP (0.600")
N24



24 Pin SOIC (EIAJ, 0.335")
R24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	OE2	Output Enable Control 2
2	PHASE	Sampling Clock Phase Control
3	CLK	Clock Input
4	DV_{DD}	Power Supply for Digital Circuits
5	AV_{DD}	Power Supply for Analog Circuits
6	$V_{REF(+)}$	Reference Voltage (+) Input
7	$V_{REF(–)}$	Reference Voltage (–) Input
8	R1	1/16th Point of Ladder R Matrix
9	R2	5/16th Point of Ladder R Matrix
10	R3	9/16th Point of Ladder R Matrix
11	R4	13/16th Point of Ladder R Matrix
12	V_{IN}	Analog Input

PIN NO.	NAME	DESCRIPTION
13	AGND	Analog Ground
14	DGND	Digital Ground
15	DB0	Data Output Bit 0 (LSB)
16	DB1	Data Output Bit 1
17	DB2	Data Output Bit 2
18	DB3	Data Output Bit 3
19	DB4	Data Output Bit 4
20	DB5	Data Output Bit 5
21	DB6	Data Output Bit 6
22	DB7	Data Output Bit 7 (MSB)
23	OFW	Digital Output Overflow
24	$\overline{OE1}$	Output Enable Control 1

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, F_S = 2.5 MHz (50% Duty Cycle), $V_{REF(+)}$ = 4.1, $V_{REF(–)}$ = AGND, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		8			8		Bits	
Sampling Rate[1]	F_S	0.001		3.0	0.001	3.0	MHz	
ACCURACY (J Grade)[2]								
Differential Non-Linearity	DNL			±3/4		±3/4	LSB	
Integral Non-Linearity	INL			±3/4		±3/4	LSB	Best Fit Line
REFERENCE VOLTAGES								
Positive Ref. Voltage[3]	$V_{REF(+)}$			AV_{DD}		V_{DD}	V	
Negative Ref. Voltage	$V_{REF(–)}$	AGND			AGND		V	
Differential Ref. Voltage	V_{REF}		AV_{DD}-AGND			AV_{DD}-AGND	V	
Ladder Resistance	R_L	500		1500	300	1950	Ω	
Ladder Temp. Coefficient[4]	R_{TCO}					3000	ppm/°C	
ANALOG INPUT[4]								
Input Voltage Range	V_{IN}	$V_{REF(–)}$		$V_{REF(+)}$	$V_{REF(–)}$	$V_{REF(+)}$	V p-p	
Input Impedance	Z_{IN}		10				MΩ	
Input Capacitance Sample[6]	C_{IN}		50				pF	
Aperture Delay[7]	t_{AP}		55				ns	
Aperture Uncertainty (Jitter)[7]	t_{AJ}		200				ps	
DIGITAL INPUTS								
Logical “1” Voltage	V_{IH}	3.5			3.5		V	
Logical “0” Voltage	V_{IL}			0.4		0.4	V	
Leakage Currents[8]								V_{IN}=DGND to DV_{DD}
$\overline{CLK}$	I_{IN}			±50		±50	µA	
Input Capacitance[4]	C_{IN}		5				pF	
Clock Timing (*See Figure 1.*)								
Clock Period	t_S	400			400		ns	
“High” Time	t_H	200			200		ns	
“Low” Time	t_L	200			200		ns	
Duty Cycle			50				%	
DIGITAL OUTPUTS								C_{OUT}=5 pF
Logical “1” Voltage	V_{OH}	4.6			4.6		V	I_{LOAD} = –1.0 mA
Logical “0” Voltage	V_{OL}			0.4		0.4	V	I_{LOAD} = 2.0 mA
3-state Leakage	I_{OZ}			±50		±60	µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay[4]	t_{DL}		55				ns	
Data Enable Delay[4]	t_{DEN}		20				ns	
Data 3-state Delay[4]	t_{DHZ}		26				ns	
Digital Output Delay[4]	t_D			55			ns	
Output Capacitance[4]	C_{OL}		5				ns	

ELECTRICAL CHARACTERISTICS TABLE CONT'D

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLIES[9]								
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4.0	5.0	6.0		6.0	V	
Current (AV_{DD} + DV_{DD})	I_{DD}			20.0		36.0	mA	

NOTES

1 Maximum samplng frequency is the frequency which will still meet the non-linearity specification. However, the device is capable of higher frequency operation.

2 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (*Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 4.).* Accuracy is a function of the sampling rate (F_S).

3 For best results, it is recommended that the reference voltage be limited to AV_{DD} –0.5 V.

4 Guaranteed. Not tested.

5 Specified values guarantee functionality. Refer to other parameters for accuracy.

6 See V_{IN} input equivalent circuit (*Figure 5.*). Switched capacitor analog input requires driver with low output resistance.

7 All inputs have diodes to DGND. Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.

8 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.

9 DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package and to the analog supply. DGND should be tied to AGND at the package.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} (to GND) . . . . . +6.5 V

$V_{REF(+)}$ & $V_{REF(–)}$ . . . . . V_{DD} to GND

V_{IN} . . . . . GND –0.5 to V_{DD} +0.5 V

Digital Inputs . . . . . GND –0.5 to V_{DD} +0.5 V

Digital Outputs . . . . . GND –0.5 to V_{DD} +0.5 V

Operating Temperature . . . . . 0 to +70°C

Storage Temperature . . . . . –65°C to +150°C

Lead Temperature (Soldering 10 secs) . . . . . +300°C

Package Power Dissipation Rating to 75°C

PDIP, SOIC 1000mW

Derates above 75°C . . . . . 13mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

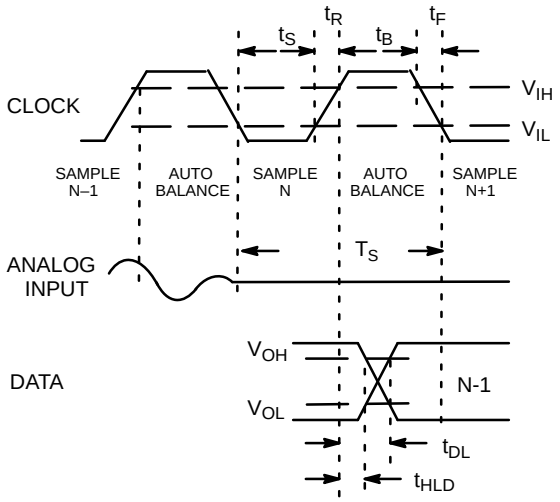


Figure 1. MP7783 Timing Diagram

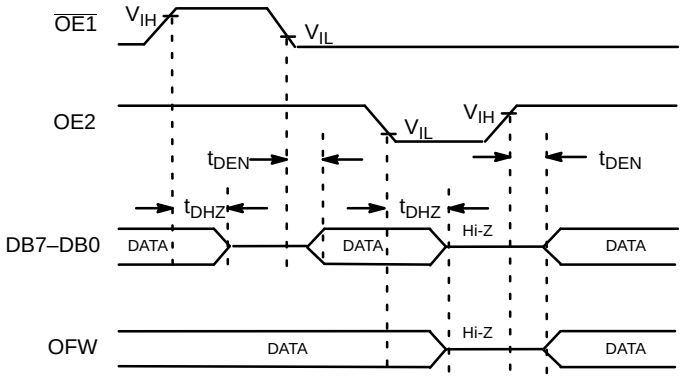
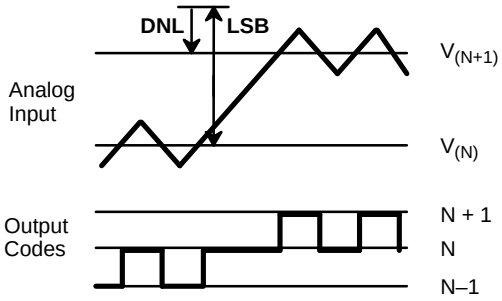


Figure 2. Output Enable/Disable Timing Diagram



(N) Code Width = $V_{(N+1)} – V_{(N)}$
LSB = [$V_{REF(+)} – V_{REF(–)}$] / 256

DNL(N) = [$V_{(N+1)} – V_{(N)}$] – LSB

Figure 3. DNL Measurement

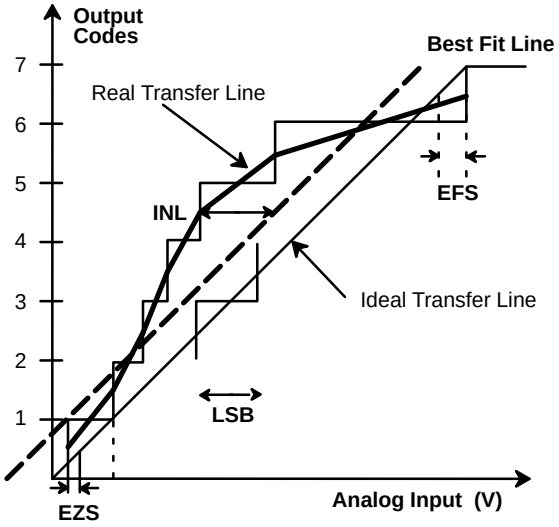


Figure 4. INL Error Calculation

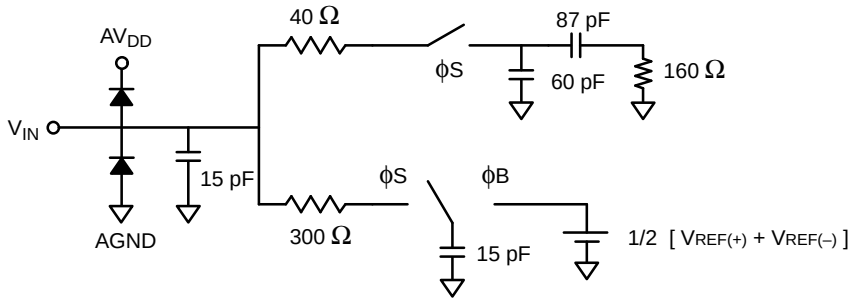


Figure 5. Analog Input Equivalent Circuit

DEVICE OPERATION

Figure 1. shows the timing information for the MP7783. A reference voltage is applied between the $V_{REF(+)}$ and $V_{REF(-)}$ which drives 256 resistors and switches with 4 voltage taps. These taps drive the inverting inputs of comparators. There are four control lines: Clock, $\overline{OE1}$, OE2 and phase. The phase line determines the polarity of the clock.

Figure 6. shows waveforms with the phase line high and low. With phase = 1, the "sample" occurs during the high period of the clock cycle, and the "auto-balance" occurs during the low period of the clock. The "sample" is queued and pipelined through a series of registers and latches. It appears at the output after 2 clock periods and time delay (Td). After the sample is acquired the data is valid for every clock period. The $\overline{OE1}$ will independently disable the 8 data bit buffers when it is in a high state. The truth table (*Table 1.*) summarizes this effect.

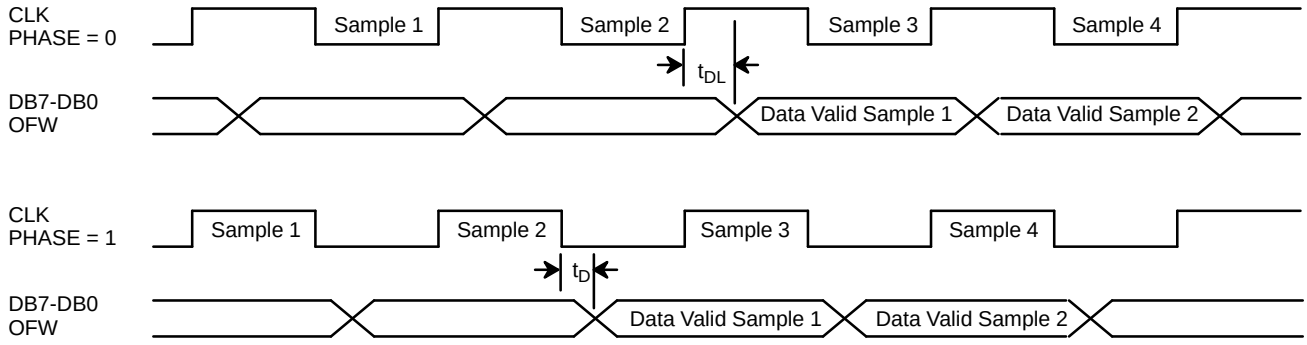


Figure 6. Timing Diagram

$\overline{OE1}$	OE2	DB7 - DB0	OFW
0	1	Valid	Valid
1	1	3-state	Valid
X	0	3-state	3-state

Table 1. Truth Table

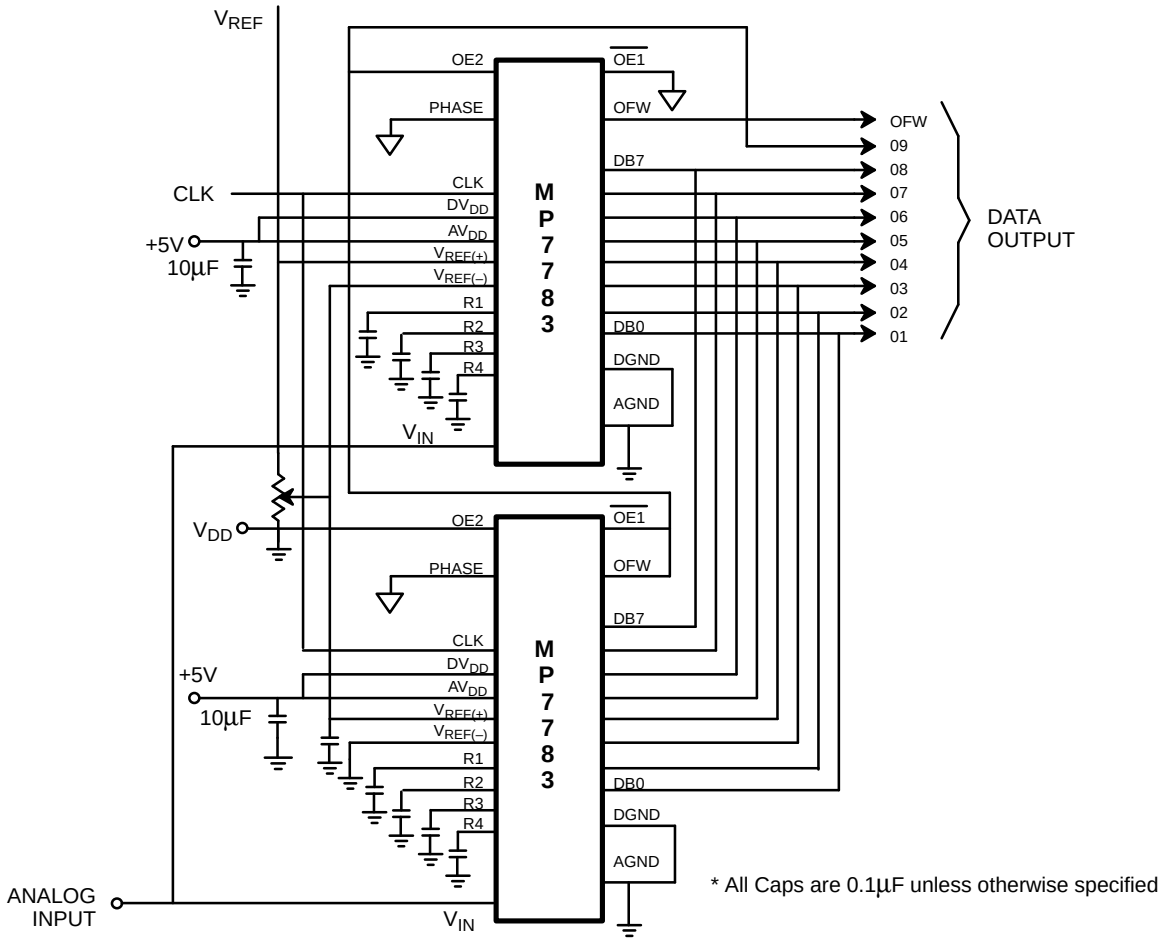


Figure 7. MP7783 9-Bit Resolution Configuration

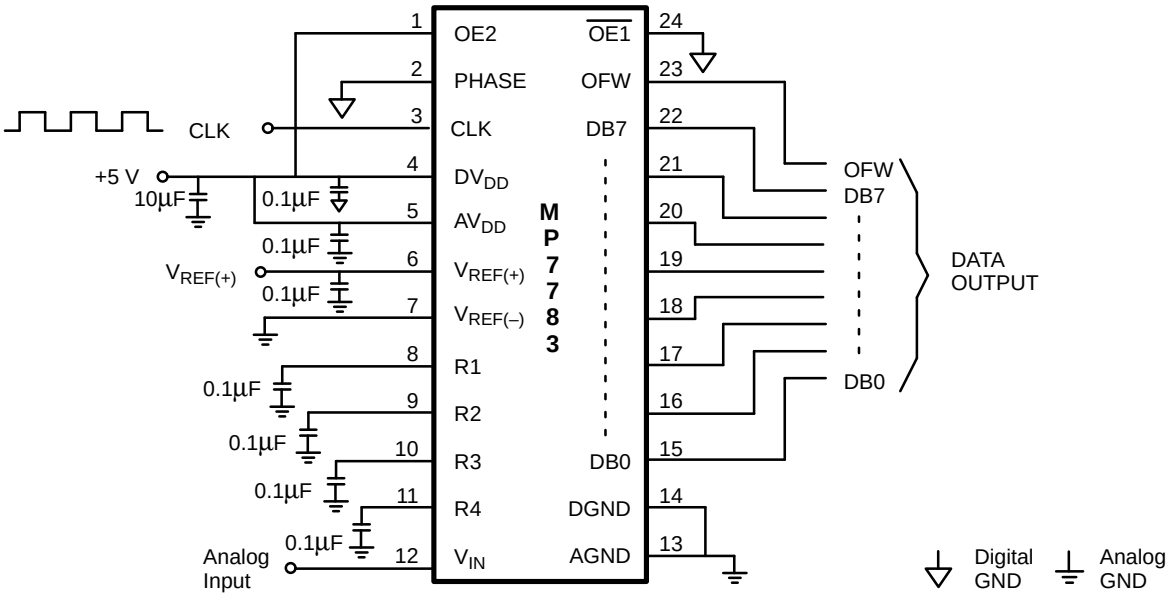


Figure 8. MP7783 Typical Connections

LINEARITY ADJUSTMENT

As noted in the specifications, integral non-linearity can be adjusted externally to enhance performance. While the setup may seem a little awkward, we have found that it can prove beneficial for high speed applications requiring 1/4 LSB at room temperature and 1/2 LSB over temperature.

Referring to *Figure 9.*, the reference resistor taps for 1/16th, 5/16ths, 9/16ths and 13/16ths of V_{REF} are brought out separately. In normal applications the user simply ties a 0.1 µF capacitor to ground at each of these nodes to provide a measure of filtering when the comparators are "zeroed" to their respective reference voltage points along the continuous ladder network. To compensate for comparator loading and other subtle errors associated with the distributed resistance of the ladder, the user can connect a "true" voltage source at each node and trim for optimized performance. As shown in *Figure 10.,* a series of op amps is used to set the proper voltage at each node. The value is best determined empirically by setting the nominal value for the node (e.g. 1/16th of V_{REF} at R1) and then fine tuning to significantly reduce the integral error.

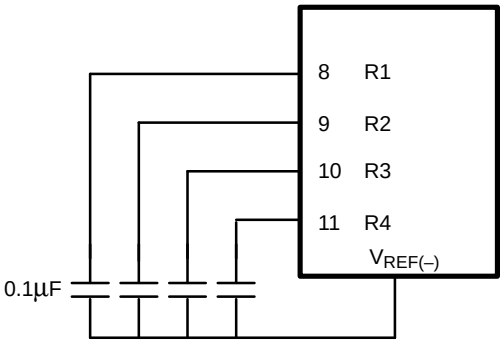


Figure 9.

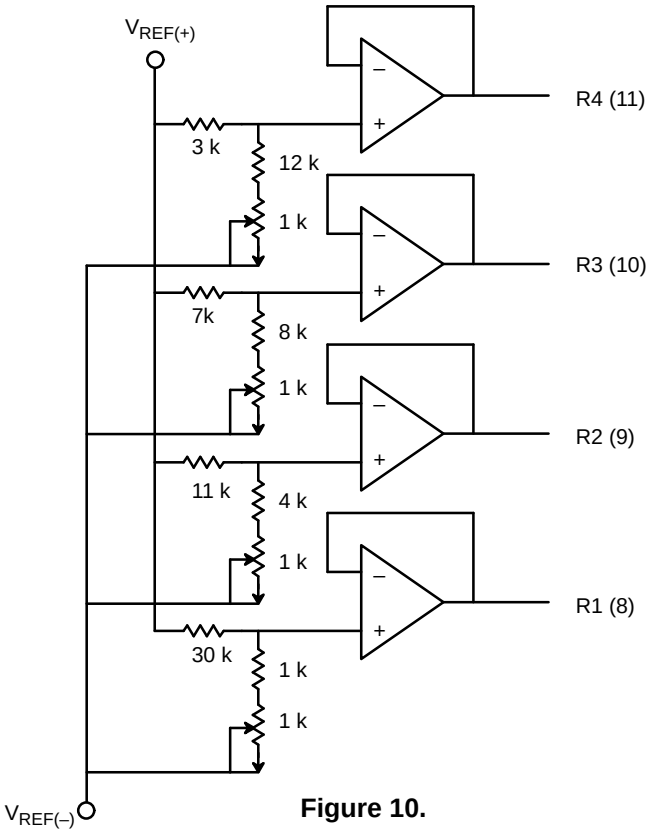
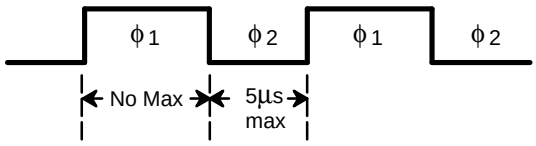


Figure 10.

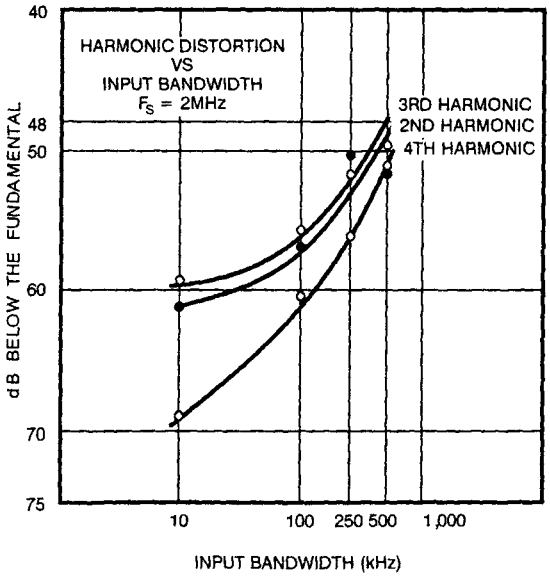
APPLICATION NOTES:

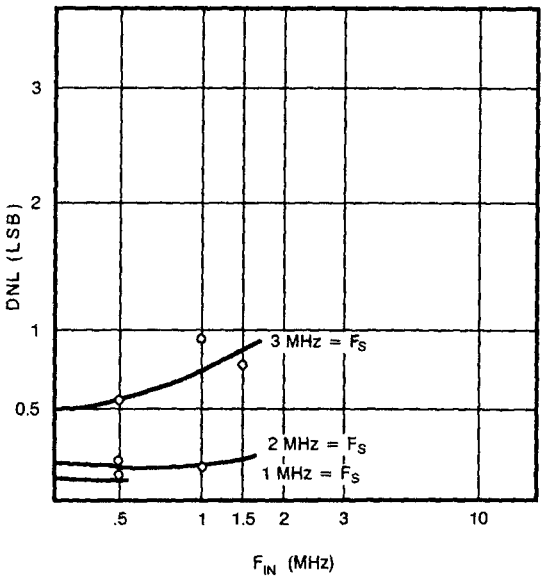
The following information will be useful in maximizing the performance of the MP7783.

1. This device may be susceptible to latch-up. All signals must not exceed DV_{DD} or DGND, or AV_{DD} or AGND at any time. Power should always be applied before any input signal is connected to avoid a latch-up condition.
2. The design of the PC layout and assembly will seriously affect the accuracy of the MP7783. Use of wire wrap is not recommended.
3. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
4. The analog input should be driven with a buffer Op Amp ($Z_{OUT} \leq 50\ \Omega$).
5. The use of a large shield plane is highly recommended, connected only at one point and connected to virtual ground.
6. The power supplies and reference voltages should be decoupled with ceramic (0.01 to 0.1µF) and tantalum (10µF) capacitors as close to the device as possible.
7. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used.

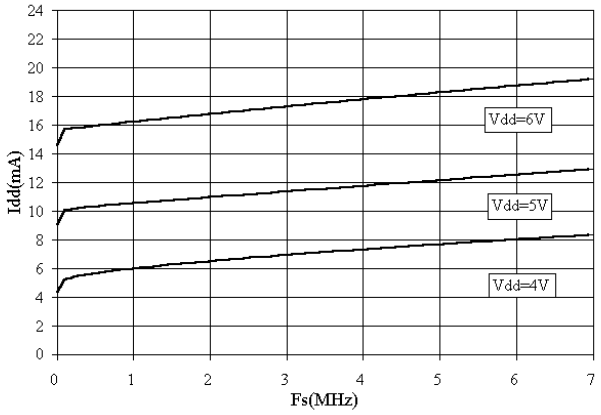


a. The minimum clock rate at 50% Duty Cycle is 10 kHz.
b. The minimum clock rate at non-50% Duty cycle may be DC as long as ϕ2 is kept to less than 5 µs.

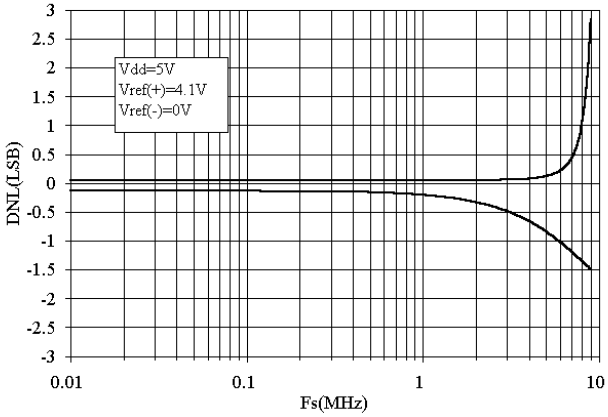




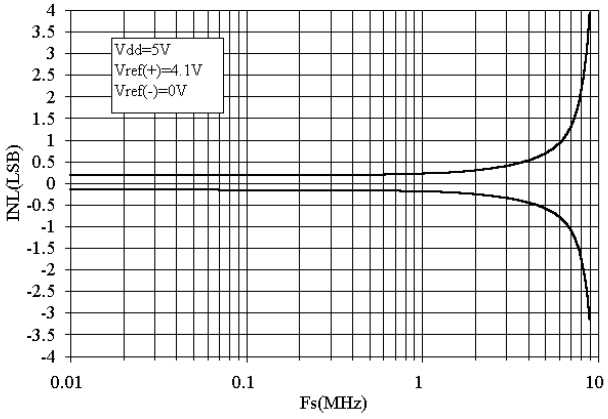
PERFORMANCE CHARACTERISTICS



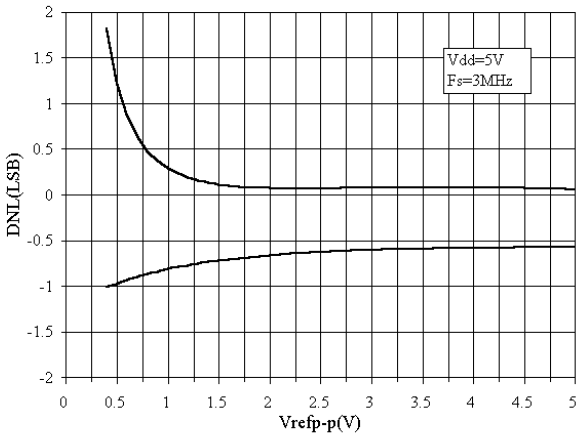
Graph 1. Supply Current vs. Sampling Frequency



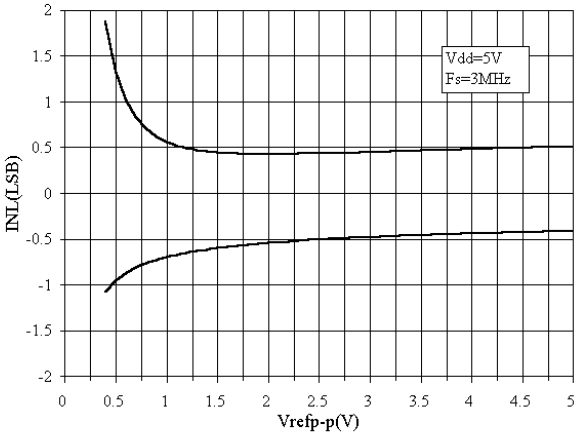
Graph 2. DNL vs. Sampling Frequency



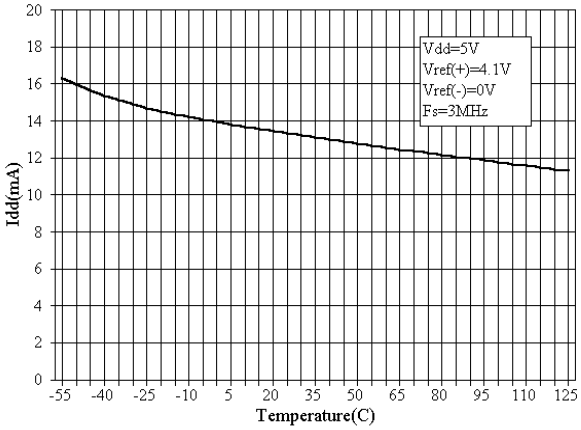
Graph 3. INL vs. Sampling Frequency



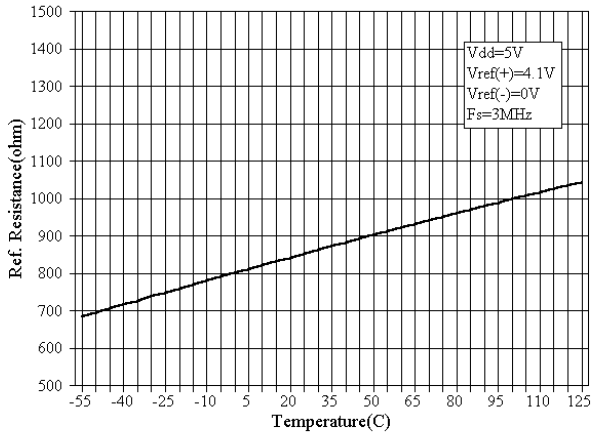
Graph 4. DNL vs. Reference Voltage



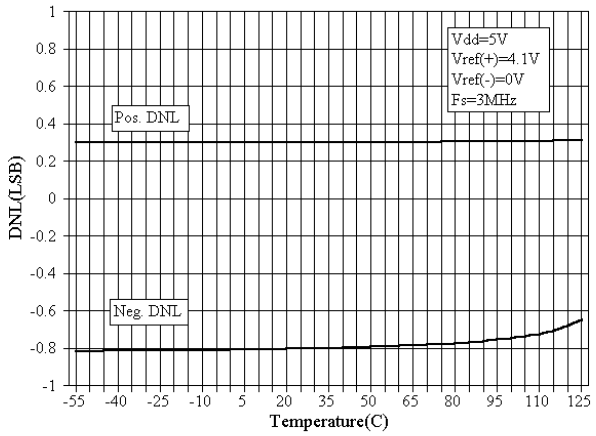
Graph 5. INL vs. Reference Voltage



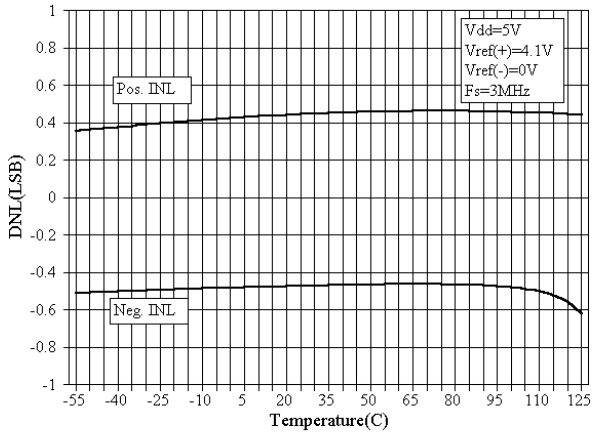
Graph 6. Supply Current vs. Temperature



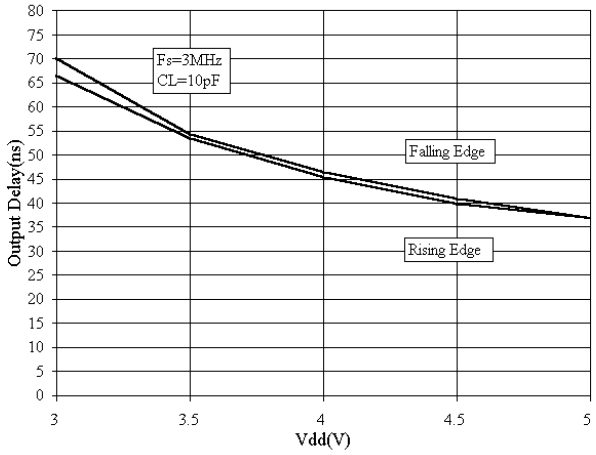
Graph 7. Reference Resistance vs. Temperature



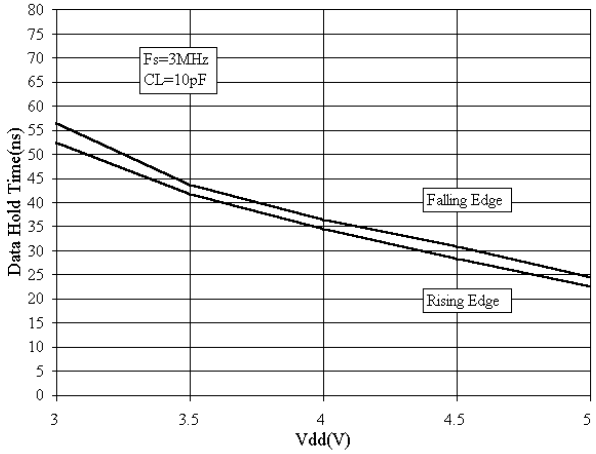
Graph 8. DNL vs. Temperature



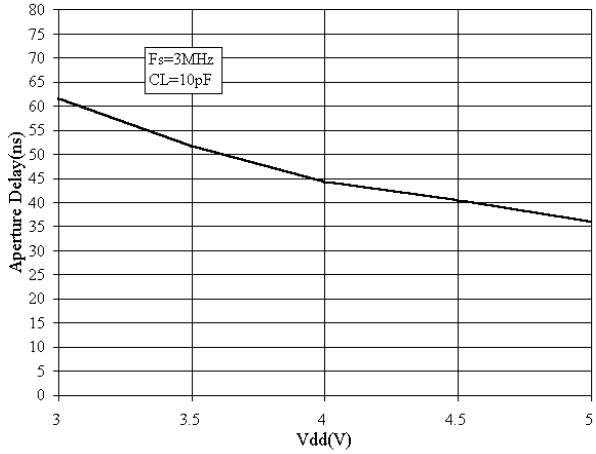
Graph 9. INL vs. Temperature



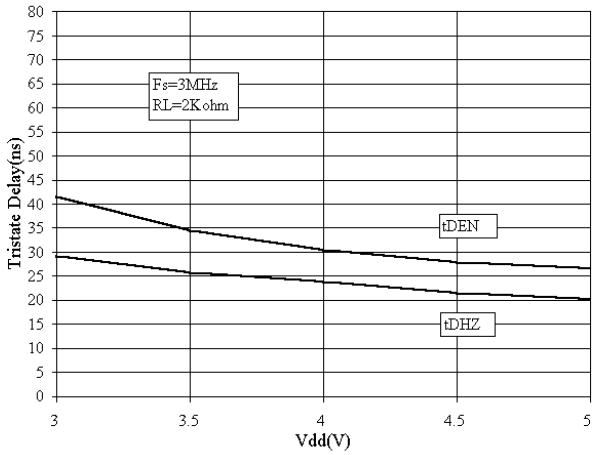
Graph 10. Output Delay vs. Supply Voltage



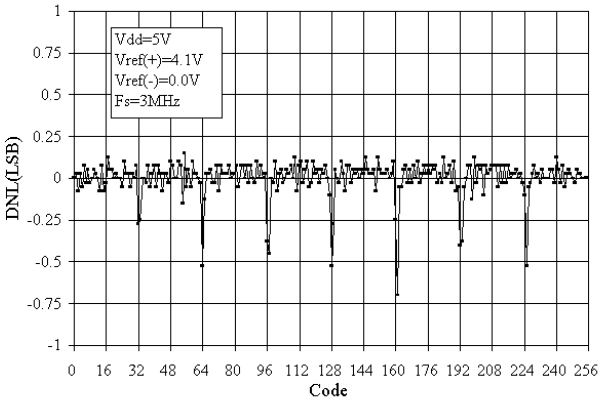
Graph 11. Data Hold Time vs. Supply Voltage



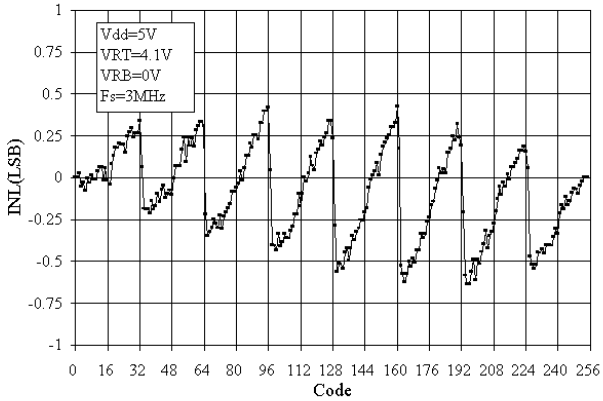
Graph 12. Aperture Delay vs. Supply Voltage



Graph 13. 3-state Enable Delay vs. Supply Voltage

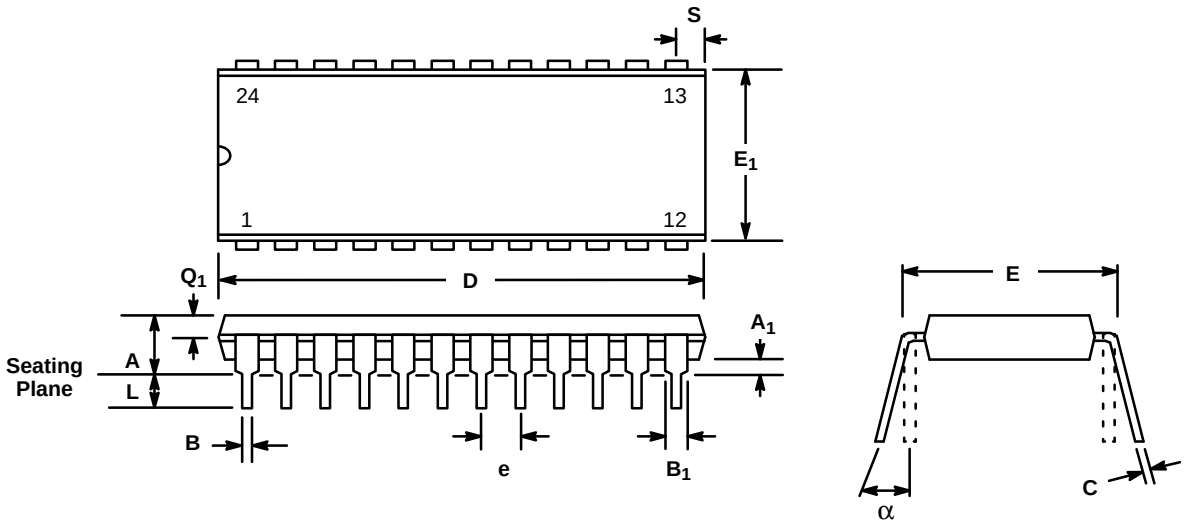


Graph 14. DNL Error Plot



Graph 15. INL Error Plot

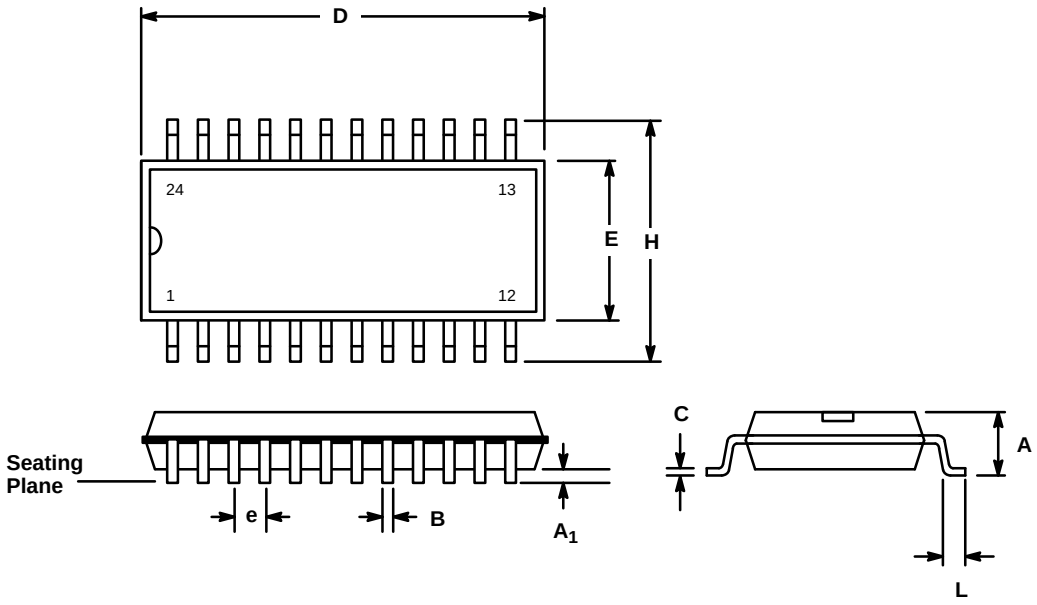
24 LEAD PLASTIC DUAL-IN-LINE
(600 MIL PDIP)
N24



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.225	—	5.72
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.160	1.290	29.46	32.77
E	0.585	0.625	14.86	15.88
E_1	0.500	0.610	12.70	15.49
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.098	1.02	2.49

Note: (1) The minimum limit for dimensions B1 may be 0.023” (0.58 mm) for all four corner leads only.

24 LEAD SMALL OUTLINE
(335 MIL EIAJ SOIC)
R24



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.60	2.80	0.102	0.110
A1	0.2 (typ.)		0.008 (typ.)	
B	0.3	0.50	.012	0.020
C	0.10	0.20	0.004	0.008
D	15.0	15.4	0.590	0.606
E	8.3	8.5	0.327	0.335
e	1.27 (typ.)		0.050 (typ.)	
H	11.5	12.1	0.453	0.477
L	0.8	1.2	0.031	0.047

Notes

NOTICE

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