MP76L90

Low Voltage CMOS
Programmable Input Range 8-Bit
High Speed Analog-to-Digital Converter

FEATURES

- **Sampling Rates from 1 kHz to 5 MHz**
- **Interface to any Input Range between GND and V_{DD}**
- **Input Op Amp Not Required**
- **Monotonic; No Missing Codes**
- **Single Power Supply (3.3 V)**
- **Low Power CMOS (45 mW)**
- **ESD Protection: 4000 Volts Minimum**
- **Latch-Up Free**

BENEFITS

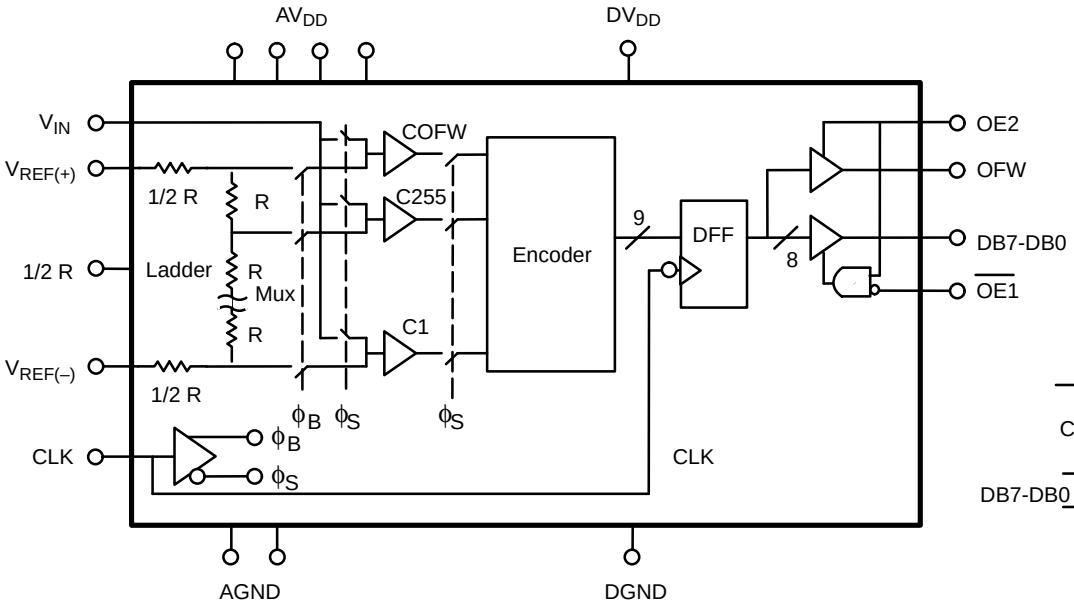
- **Reduced Board Space (small package)**
- **Excellent Accuracy Without High System Power**
- **Reduced External Parts, No Sample/Hold Needed**
- **Designer Can Adapt Input Range and Scaling**

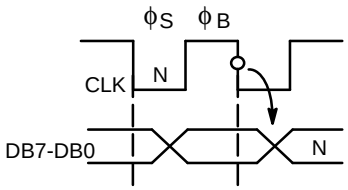
GENERAL DESCRIPTION

The MP76L90 is an 8-bit CMOS single step high speed Analog-to-Digital Converter designed for precision applications in video and data acquisition requiring conversion rates to 5 MHz with differential linearity error less than 1/2 LSB and low power consumption. The input architecture of the MP76L90 allows direct interface to any analog input range between AGND and AV_{DD} (50 mV to AV_{DD}). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

The MP76L90 includes 256 clocked comparators, encoders, 3-state output buffers, a reference ladder resistor and associated timing circuitry. An overflow bit (or flag) is provided.

SIMPLIFIED BLOCK AND TIMING DIAGRAM



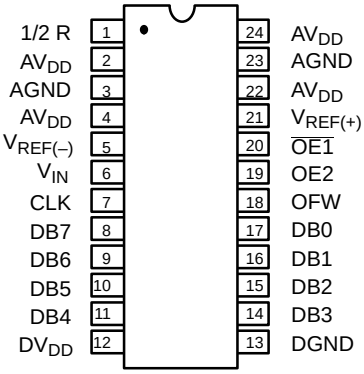


ORDERING INFORMATION

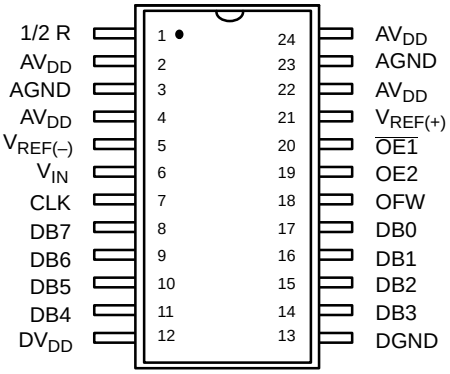
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP76L90AN	±1	1
SOIC	–40 to +85°C	MP76L90AS	±1	1

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin PDIP (0.300")
NN24



24 Pin SOIC (Jedec, 0.300")
S24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	1/2R	Center of Reference Ladder
2	AV_{DD}	Analog Power Supply Voltage
3	AGND	Analog Ground Return
4	AV_{DD}	Analog Power Supply Voltage
5	$V_{REF(–)}$	Lower Reference Voltage Input
6	V_{IN}	Analog Input Voltage
7	CLK	Sampling Clock Input
8	DB7	Data Output Bit 7 (MSB)
9	DB6	Data Output Bit 6
10	DB5	Data Output Bit 5
11	DB4	Data Output Bit 4
12	DV_{DD}	Digital Power Supply Voltage

PIN NO.	NAME	DESCRIPTION
13	DGND	Digital Ground Return
14	DB3	Data Output Bit 3
15	DB2	Data Output Bit 2
16	DB1	Data Output Bit 1
17	DB0	Data Output Bit 0 (LSB)
18	OFW	Overflow flag
19	OE2	Output Enable Control Pin
20	$\overline{OE1}$	Output Enable Control Pin
21	$V_{REF(+)}$	Upper Reference Voltage Input
22	AV_{DD}	Analog Power Supply Voltage
23	AGND	Analog Ground Return
24	AV_{DD}	Analog Power Supply Voltage

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 3$ V, $F_S =$ 5 MHz (50% Duty Cycle), $V_{REF(+)} = 3$, $V_{REF(-)}$ = AGND, $T_A = 25°C$

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		8			8		Bits	
Sampling Rate	F_S	0.001		5	0.001	5	MHz	For Specified Accuracy
ACCURACY (A Grades)[1]								
Differential Non-Linearity	DNL			±1		±1	LSB	
Integral Non-Linearity	INL			1		1	LSB	Best Fit Line (Min INL – Max INL)/2
REFERENCE VOLTAGES								
Positive Ref. Voltage	$V_{REF(+)}$	0.05		3			V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND					V	
Differential Ref. Voltage[3]	V_{REF}	50		AV_{DD}-AGND		AV_{DD}-AGND	mV	
Ladder Resistance	R_L	180		285	165	305	Ω	
Ladder Temp. Coefficient[2]	R_{TCO}					2000	ppm/°C	
ANALOG INPUT								
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V p-p	
Input Capacitance Sample[4]	C_{INA}		50				pF	
Aperture Delay	t_{AP}		25				ns	
Aperture Uncertainty (Jitter)	t_{AJ}		60				ps	
DIGITAL INPUTS								
Logical “1” Voltage	V_{IH}	2.5			2.5		V	
Logical “0” Voltage	V_{IL}			0.5		0.5	V	
Leakage Currents[5]								V_{IN}=DGND to DV_{DD}
CLK	I_{IN}	–100		100			µA	
DIGITAL OUTPUTS								
Logical “1” Voltage	V_{OH}	2.5			2.5		V	
Logical “0” Voltage	V_{OL}			0.5		0.5	V	
Tristate Leakage	I_{OZ}			±10		±15	µA	
POWER SUPPLIES[6]								
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	3	3.3	3.6		3.3	V	
Current (AV_{DD} + DV_{DD})	I_{DD}			15		20	mA	
AC PARAMETERS[2]								
Signal Noise Ratio[7]	SNR		40				dB	
Harmonic Distortion								100 mV F_S
Total Harmonic Distortion[8]	THD		–38				dB	F_S = 5 MHz, F_{IN} = 100 kHz
DYNAMIC ACCURACY								Histogram Test
Differential Non-Linearity[2]	DNL		0.3				LSB	F_{IN} = 0.1 MHz

ELECTRICAL CHARACTERISTICS TABLE CONT'D

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (VIN). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (*Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 4.*). Accuracy is a function of the sampling rate (F_S).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 See V_{IN} input equivalent circuit (*Figure 5.*). Switched capacitor analog input requires driver with low output resistance.

5 All inputs have diodes to DV_{DD} and DGND. Input(s) $\overline{OE1}$ has (have) internal pull down(s). Input(s) OE2 has(have) internal pull up(s). Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.

6 DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package and to the analog supply.

7 SNR: Ratio of RMS signal to RMS noise, up to 1/2 F_S in dB.

8 THD: Ratio of total RMS of harmonics (2nd to 5th) over RMS of signal, in dB.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +7 V

$V_{REF(+)}$ & $V_{REF(–)}$ ..... GND –0.5 to V_{DD} +0.5 V

V_{IN} ..... GND –0.5 to V_{DD} +0.5 V

All Inputs ..... GND –0.5 to V_{DD} +0.5 V

All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C

Lead Temperature (Soldering 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C

PDIP, SOIC 1000mW

Derates above 75°C ..... 13mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

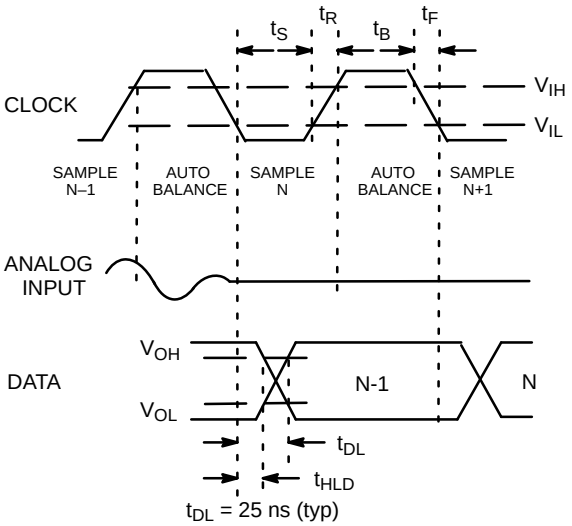


Figure 1. MP76L90 Timing Diagram

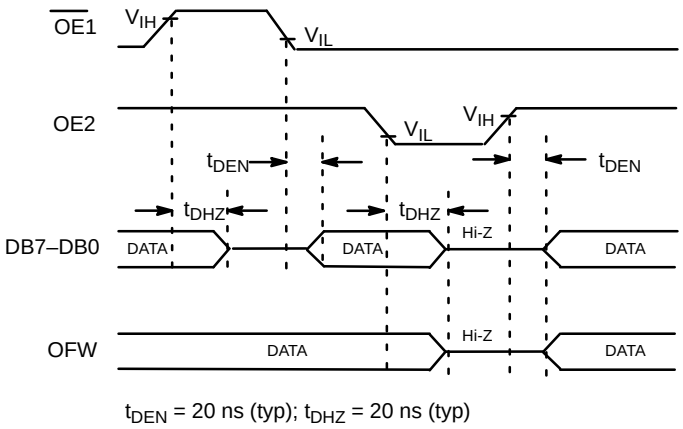
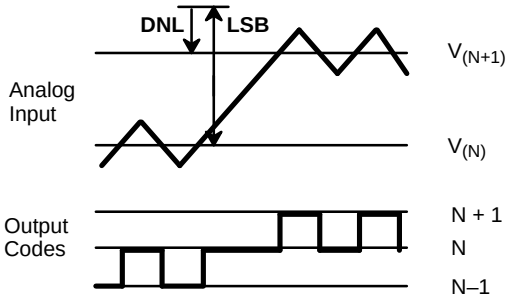


Figure 2. Output Enable/Disable Timing Diagram



(N) Code Width = $V_{(N+1)} – V_{(N)}$
LSB = [$V_{REF(+)} – V_{REF(–)}$] / 256

DNL(N) = [$V_{(N+1)} – V_{(N)}$] – LSB

Figure 3. DNL Measurement

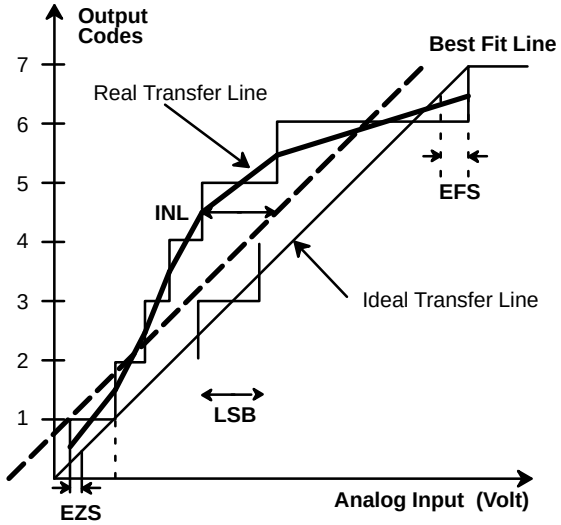


Figure 4. INL Error Calculation

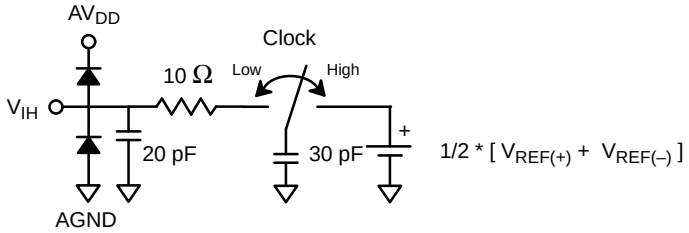


Figure 5. Analog Input Equivalent Circuit

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP76L90 converts analog voltages into 256 digital codes by encoding the outputs of 255 comparators. A 256th comparator is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 1.5 clock periods. Data is transferred from the comparator latches to the output registers each clock period and at the same time the input is sampled.

The clock signal generates the two internal phases, ϕ_B (CLK high = balance) and ϕ_S (CLK low = sample). ϕ_B connects the comparators to the reference tap points. ϕ_S connects the comparators to the analog input voltage.

The reference resistance ladder is a series of 257 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 256 * R$ $\quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 256 * LSB$

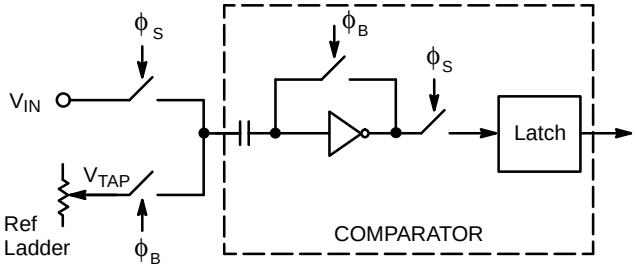


Figure 6. MP76L90 Comparator

The MP76L90 comparators use the balance phase (ϕ_B) to charge one plate of the capacitors to the reference ladder tap point (V_{TAP}) and the other to the inverter/comparator trigger point. During the sample phase (ϕ_S) one plate of the capacitors switches to V_{IN}. The change in voltage ($V_{IN} - V_{TAP}$) transfers across the capacitors and forces the inverters into one of the two possible logic states. Latches (connected to the comparators during ϕ_S) restores and propagates the digital level to the decode logic.

The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The aperture delay may vary from one cycle to the next. Internal thermal noise, power supply noise and slow input clock edges are major contributors to this variation. The aperture jitter (t_{AJ}) is the variation of the aperture delay distribution.

This uncertainty shows as digital code errors if the input slew rate multiplied by t_{AJ} is of the same order of magnitude as the LSB. That is if $(dv/dt) * t_{AJ} \approx V_{REF}/256$ an internal error of 1 LSB results.

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 7.*

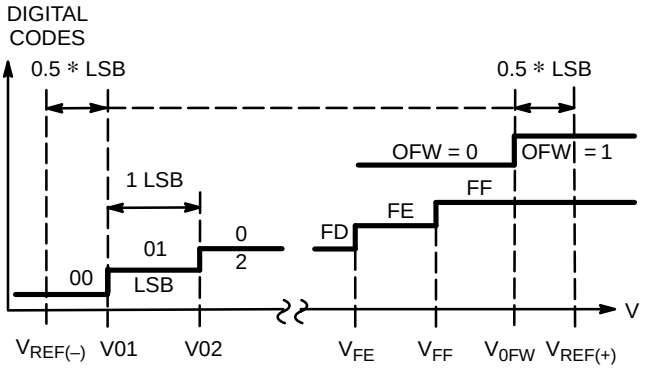


Figure 7. Ideal A/D Transfer Function

The overflow transition (V_{OFW}) takes place at:

$V_{IN} = V_{OFW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V01 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{FF} = V_{REF(+)} - 1.5 * LSB$

$LSB = (V_{REF(+)} - V_{REF(-)}) / 256 = (V_{FF} - V01) / 254$

Note that the overflow transition is a flag and has no impact on the data bits.

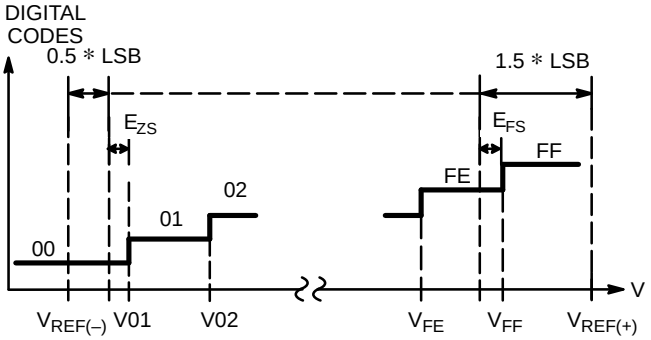


Figure 8. Real A/D Transfer Curve

In a "real" converter, the code-to-code transitions do not fall exactly every $(V_{REF(+)} - V_{REF(-)}) / 256$ volts.

A positive DNL (Differential Non Linearity) error means that the real width of a particular code is larger than or less than 1 LSB. This error is measured in fractions of LSB's.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = $\pm$ 0.5 LSB means that all codes are within 0.5 and 1.5 LSB. If V_{REF} = 4.096 V then 1 LSB = 16mV and every code width is within 8 and 24 mV.

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (EZS, EFS) are:

DNL (01) = V02 – V01 – LSB

: : :

DNL (FE) = $V_{FF} – V_{FE}$ – LSB

EFS (full scale error) = $V_{FF} – [V_{REF(+)} – 1.5 * LSB]$

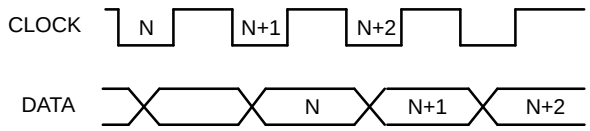
EZS (zero scale error) = $V_{01} – [V_{REF(–)} + 0.5 * LSB]$

Figure 8. shows the zero scale and full scale error terms.

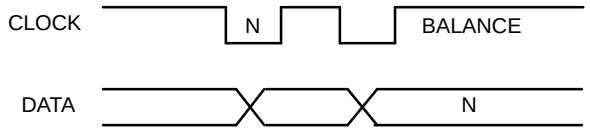
Systems that adjust the V_{REF} voltages to correct for EFS and EZS only increase the accuracy at the two extreme points. In the MP76L90, such adjustments have little impact at frequencies lower than 10 MHz and generally are not required. Refer to the characterization data for temperature and frequency dependence.

Figure 4. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

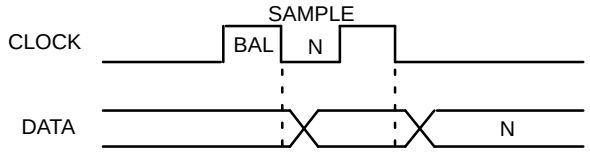
After a tester has measured all the transition voltages, a line is drawn parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and the negative INL errors. For example, an INL error of –1 to +2 LSB's relative to the Ideal Line would be ±1.5 LSB's relative to the Best Fit Line.



a. Continuous clock



b. Two negative clock pulses



c. Two positive clock pulses

Figure 9. Relationship of Data to Clock

Clock and Conversion Timing

A system will clock the MP76L90 continuously (*Figure 9a*) or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 9b* keeps the MP76L90 comparators in balance and ready to sample the analog input. This mode draws the most current from AV_{DD}. The timing of *Figure 9c* leaves the comparator inputs floating (and AC coupled to the V_{IN} input) and a balance phase is needed before a valid sampling phase. In this mode, I_{DD} varies because of the floating comparator inputs.

Analog Input

Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP76L90's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. These have an impact above 5 MHz and they are very important above 10 MHz. Use of Current Feedback Amplifiers is an easy and cost effective way to maximize performance.

Reference Voltages

If the input bandwidth is limited to the Nyquist region (F_{IN}) < (F_S) /2 then the two reference voltages can be set at any two values between the supplies. V_{REF} (their difference) can be reduced down to 1.5 volts with minor change in accuracy. If the input bandwidth exceeds (F_S) /2, then it is recommended that V_{REF} is lower than V_{DD}/2.

At V_{REF} = 1.5 V the LSB is reduced to 6mV. Further reductions show an increased error in terms of LSB (which is getting smaller) even if the error in terms of mV is about constant.

The input/output relationship as a function of V_{REF}:

$$A_{IN} = V_{IN} – V_{REF(–)}$$
$$V_{REF} = V_{REF(+)} – V_{REF(–)}$$
$$DATA = 256 * (A_{IN}/V_{REF})$$
$$0 \le V_{IN} \le V_{REF} – 1\ LSB,\ DATA = 255\ if\ V_{IN} = V_{REF}$$

a) **Gain adjustment.** A system can increase total gain by reducing V_{REF}.

b) **Increasing dynamic range**. A system can increase dynamic range by using DAC's to control V_{REF} and by "focusing" on input ranges of interest. In digitizing "static" information (an image in a scanner), a first digitization would point to the input range in which most of the output codes fall. The system then would adjust the DACs to generate $V_{REF(+)}$ and $V_{REF(–)}$ to include just the range of interest for the second and final pass.

c) **Subranging; increasing resolution**. Where practical, multiple passes at different V_{REF} ranges can increase resolution without changing hardware. A system needs to make four passes to increase the resolution to 10 bits. The merging of the data from the four passes can create DNL errors at the borders of the ranges. One solution is to "overlap" the ranges and to use software methods to properly merge the ranges.

Digital Interfaces

The logic encodes the 255 bits into a binary code and latches the data in a D-type flip-flop for output. The inputs $\overline{OE1}$ and OE2 control the output buffers in an asynchronous mode.

The functional equivalent of the MP76L90 (*Figure 10.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An A/D which tracks and converts V_{IN} with no delay.
3) A DFF with specified hold (t_{HLD}) and delay (t_{DL}) times.

$\overline{OE1}$	OE2	OFW	DB7 – DB0
X	0	High Z	High Z
1	1	Valid	High Z
0	1	Valid	Valid

Table 1. Output Enable Logic

If an external DFF is to follow the MP76L90, it is recommended that the system latches the data at the negative going edge of the clock. This will work at any frequency. If the system must latch with the positive going edge then care must be taken to avoid the overlay of the clock edge with the changing outputs.

If a latch follows the ADC, the positive half of the clock used as enable signal guarantees stable output at the end of the enable pulse.

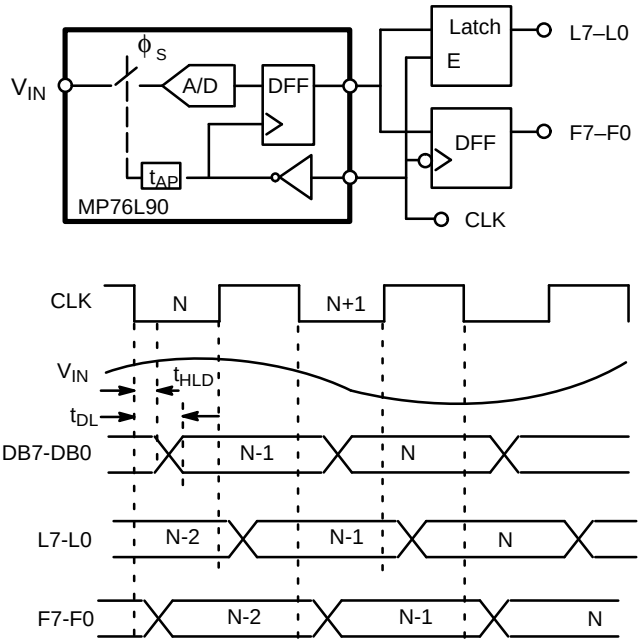
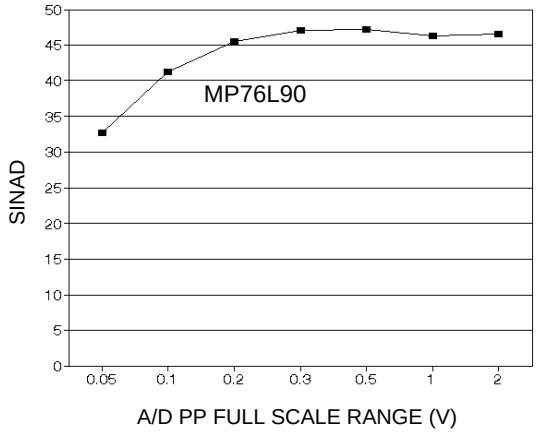


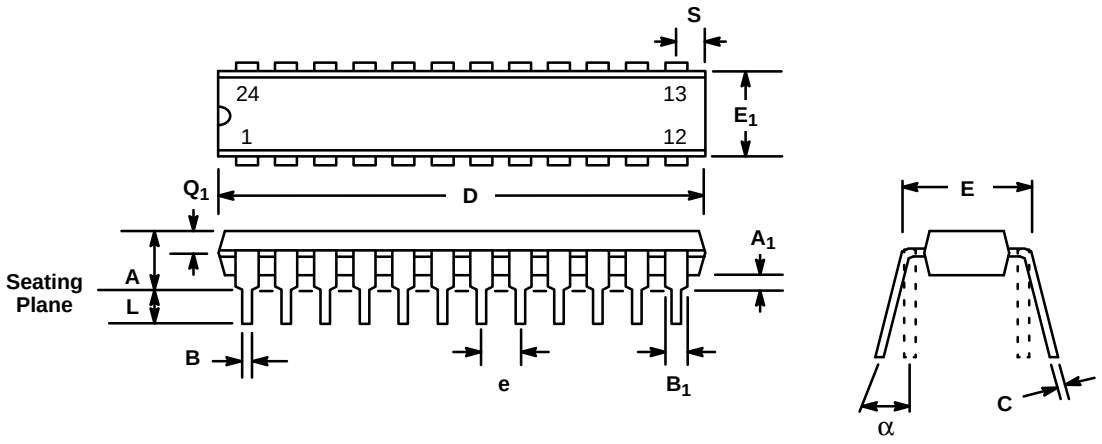
Figure 10. MP76L90 Functional Equivalent Circuit and Interface Timing

PERFORMANCE CHARACTERISTICS



Graph 1. 8-Bit Low Level Input Performance
$AV_{DD} = DV_{DD} = 3$ V, $F_S = 5$ MHz, $F_{IN} = 100$kHz

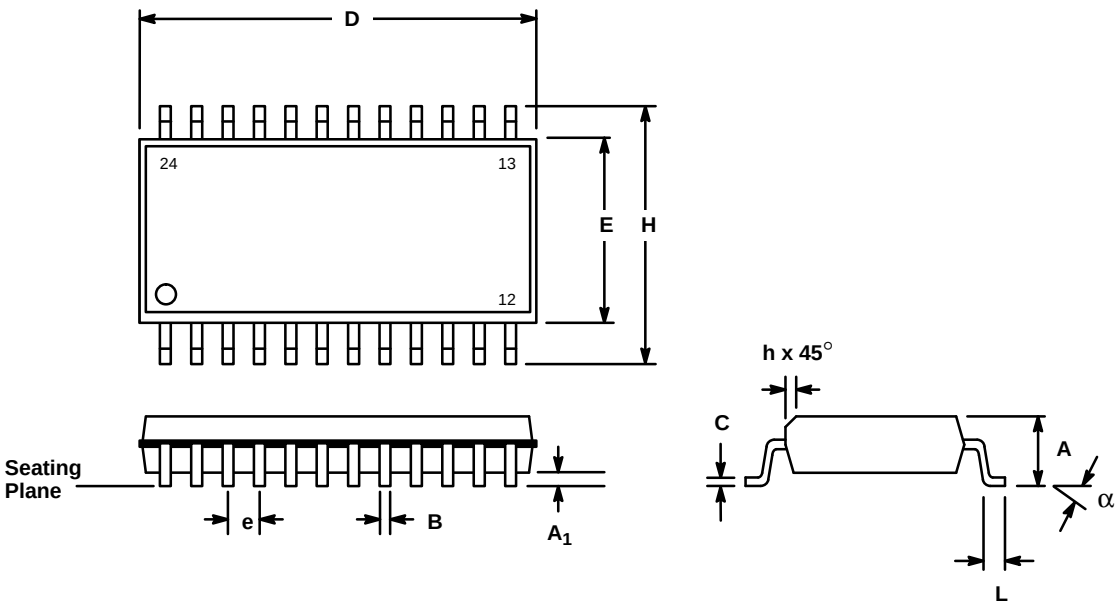
24 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
NN24



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.16	1.280	29.46	32.51
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.028	0.098	0.711	2.49

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

24 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S24



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.642
A1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.602	0.612	15.29	15.54
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

Notes

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