MP76L86

Low Voltage CMOS
Programmable Input Range 6-Bit
High Speed Analog-to-Digital Converter

FEATURES

- **Single Power Supply (3.3 Volt)**
- **Sampling Rates from 1 kHz to 6.0 MHz**
- **Interface to any Input Range between GND and V_{DD}**
- **Input Op Amp Not Required**
- **Monotonic; No Missing Codes**
- **Low Power CMOS (20 mW)**
- **ESD Protection: 4000 Volts Minimum**
- **Latch-Up Free**

BENEFITS

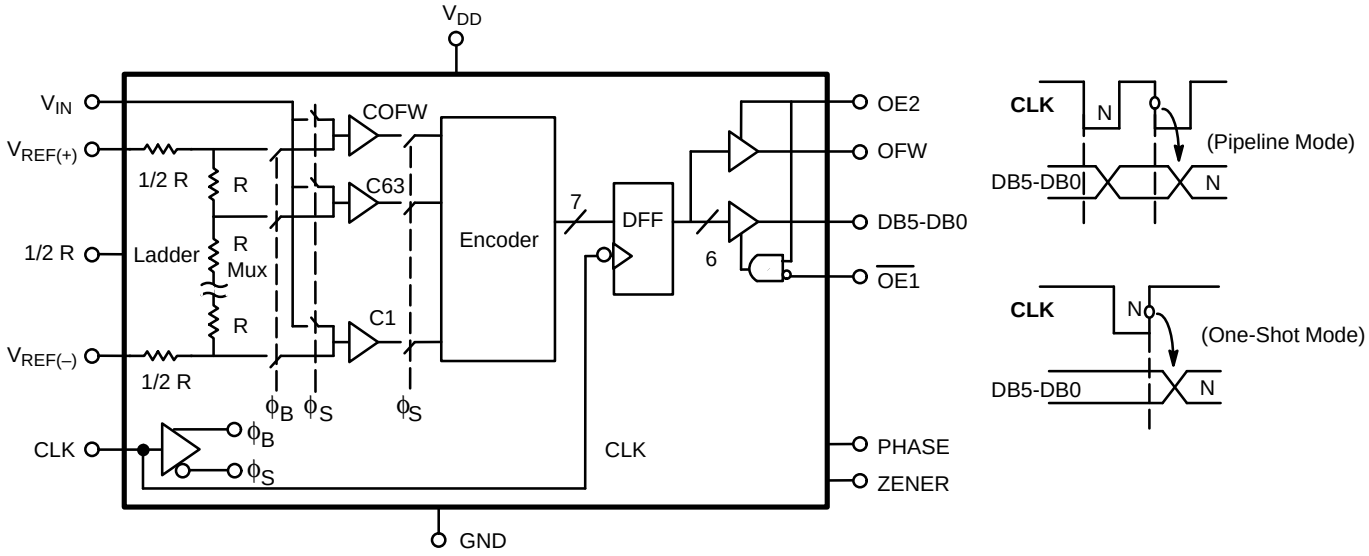
- **Reduced Board Space (small package)**
- **Excellent Accuracy Without High System Power**
- **Reduced External Parts, No Sample/Hold Needed**
- **Designer Can Adapt Input Range and Scaling**

GENERAL DESCRIPTION

The MP76L86 is a 6-bit CMOS single step high speed Analog-to-Digital Converter designed for precision applications in video and data acquisition requiring conversion rates to 6.0 MHz with differential linearity error less than 1/2 LSB and low power consumption. The input architecture of the MP76L86 allows direct interface to any analog input range between AGND and V_{DD} (of 50 mV to V_{DD}). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

The MP76L86 includes 64 clocked comparators, encoders, 3-state output buffers, a reference ladder resistor and associated timing circuitry. An overflow bit (or flag) is provided.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

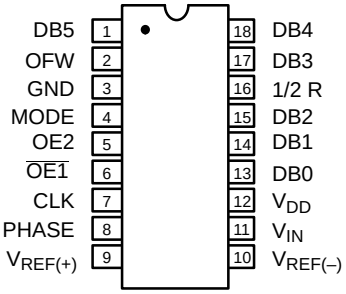


ORDERING INFORMATION

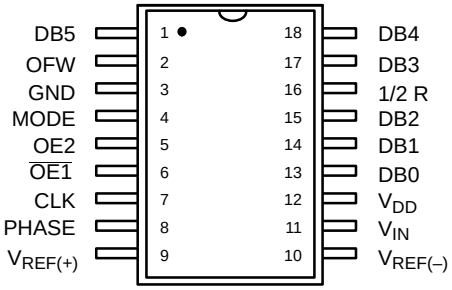
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP76L86AN	±1	1
SOIC	–40 to +85°C	MP76L86AS	±1	1

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



18 Pin PDIP (0.300")
N18



18 Pin SOIC (Jedec, 0.300")
S18

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB5	Data Output Bit 5 (MSB)
2	OFW	Digital Output Overflow
3	GND	Ground
4	MODE	Mode Select
5	OE2	Output Enable Control (See Truth Table)
6	$\overline{OE1}$	Output Enable Control (See Truth Table)
7	CLK	Clock Input
8	PHASE	Sampling Clock Phase Control
9	$V_{REF(+)}$	Positive Reference Voltage Pin

PIN NO.	NAME	DESCRIPTION
10	$V_{REF(–)}$	Negative Reference Voltage Pin
11	V_{IN}	Analog Input
12	V_{DD}	Power Supply
13	DB0	Data Output Bit 0 (LSB)
14	DB1	Data Output Bit 1
15	DB2	Data Output Bit 2
16	1/2 R	Center of Reference Ladder
17	DB3	Data Output Bit 3
18	DB4	Data Output Bit 4

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: V_{DD} = 3 V, F_S = 6.0 MHz (50% Duty Cycle), $V_{REF(+)}$ = 3, $V_{REF(-)}$ = GND, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		6			6		Bits	
Sampling Rate	F_S	0.001		6.0	0.001	6.0	MHz	
ACCURACY (A Grades)[1]								
Differential Non-Linearity	DNL			±1		±1	LSB	
Integral Non-Linearity	INL			±1		±1	LSB	Best Fit Line (Max INL – Min INL)/2
REFERENCE VOLTAGES								
Positive Ref. Voltage	$V_{REF(+)}$	0.05		3			V	
Negative Ref. Voltage	$V_{REF(-)}$	GND					V	
Differential Ref. Voltage[3]	V_{REF}	50		V_{DD}-GND		V_{DD}-GND	mV	
Ladder Resistance	R_L	180		285	160	320	Ω	
Ladder Temp. Coefficient[2]	R_{TCO}					3000	ppm/°C	
ANALOG INPUT								
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V p-p	
Input Impedance	Z_{IN}		10				MΩ	
Input Capacitance Sample[4]	C_{INA}		20				pF	
Aperture Delay	t_{AP}		25				ns	
Aperture Uncertainty (Jitter)	t_{AJ}		60				ps	
DIGITAL INPUTS								
Logical “1” Voltage	V_{IH}	2.5			2.5		V	
Logical “0” Voltage	V_{IL}			0.5		0.5	V	
Leakage Currents[5]								V_{IN}=GND to V_{DD}
CLK	I_{IN}			±100			µA	
DIGITAL OUTPUTS								
Logical “1” Voltage	V_{OH}	2.5			2.5		V	
Logical “0” Voltage	V_{OL}			0.5		0.5	V	
3-state Leakage	I_{OZ}		±1				µA	
POWER SUPPLIES[6]								
Operating Voltage	V_{DD}	3	3.3	3.6		3	V	
Current	I_{DD}			7		10	mA	
AC PARAMETERS[2]								100 mV F_S
Signal Noise Ratio[6]	SNR		32				dB	F_S = 5 MHz, F_{IN} = 100 kHz
DYNAMIC ACCURACY								Histogram Test
Differential Non-Linearity[2]	DNL		0.3				LSB	F_{IN} = 0.1 MHz

ELECTRICAL CHARACTERISTICS TABLE CONT'D

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/64) is the DNL error (*Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 4.*). Accuracy is a function of the sampling rate (F_S).

2 Guaranteed. Not tested.

3 Specified values guarantee functionality. Refer to other parameters for accuracy.

4 See V_{IN} input equivalent circuit (*Figure 5.*). Switched capacitor analog input requires driver with low output resistance.

5 All inputs have diodes to V_{DD} and GND. Input(s) $\overline{OE1}$ has (have) internal pull down(s). Input(s) OE2 has(have) internal pull up(s). Input DC currents will not exceed specified limits for any input voltage between GND and V_{DD}.

6 SNR: Ratio of RMS signal to RMS noise, up to 1/2 F_S in dB.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... +5.5 V

$V_{REF(+)}$ & $V_{REF(–)}$ ..... GND –0.5 to V_{DD} +0.5 V

V_{IN} ..... GND –0.5 to V_{DD} +0.5 V

All Inputs ..... GND –0.5 to V_{DD} +0.5 V

All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C

Lead Temperature (Soldering 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C

PDIP, SOIC 850mW

Derates above 75°C ..... 11mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

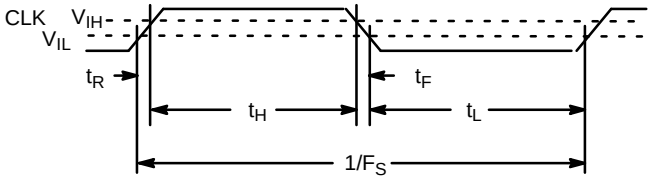


Figure 1. Clock Timing Specification

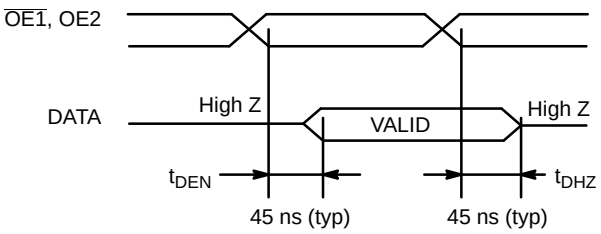


Figure 2. Data Line Enable Delay

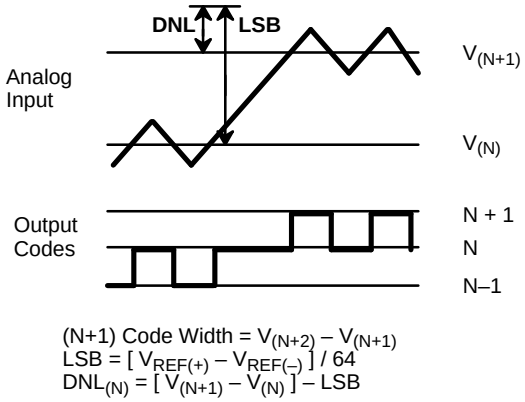


Figure 3. DNL Measurement

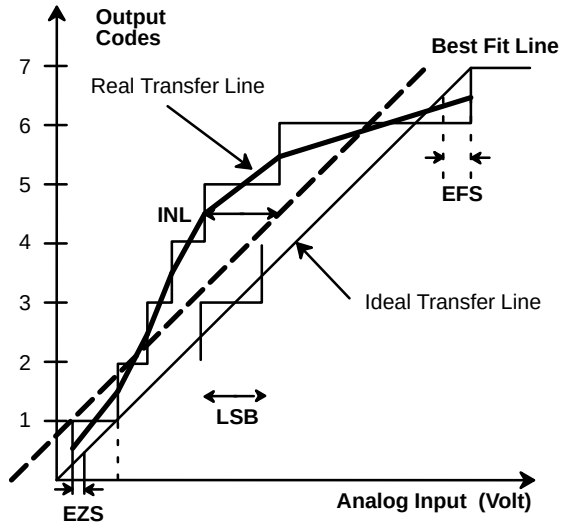


Figure 4. INL Error Calculation

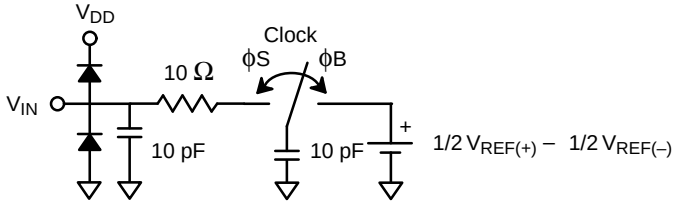


Figure 5. Analog Input Equivalent Circuit

THEORY OF OPERATION

The MP76L86 has three operating modes. It has two pipelined modes (MP7682 compatible), and a one shot mode. The voltages applied to the Phase and Mode pins determine the operating mode. *Figures 1, 2, 6 and 7* show the timing specifications. Timing parameters are measured to and from valid logic levels (i.e. t_{DH} is the time from CLK = 0.8 V to DATA = 0.4 or 2.4V).

Pipeline Modes (Mode = High)

In this configuration, the MP76L86 works in a continuous fashion (MP7682 compatible). *Figure 6.* shows the timing with the Phase pin high and low. When Phase is low, "sampling" occurs during the low period of the clock, and "balancing" during the high period. When Phase is high, operation is reversed (see *Figure 7.*), "sampling" occurs during the high period and "balancing" during the low period. The actual time when the internal comparators are connected to V_{IN} is called the Acquisition Time. This time is equal to the sample phase of the external clock delayed by t_{AD} and t_{AP}.

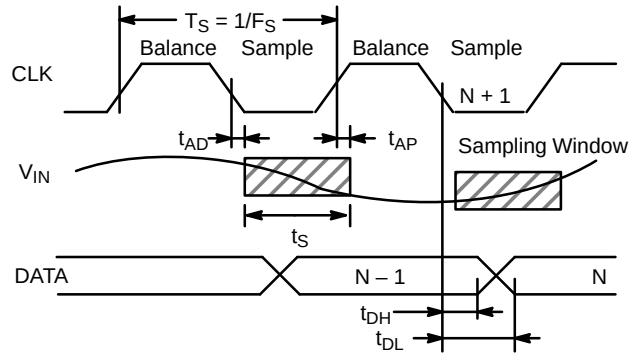


Figure 6. Pipeline Mode Timing (7682 compatible)
(Phase = 0, Mode = 1)

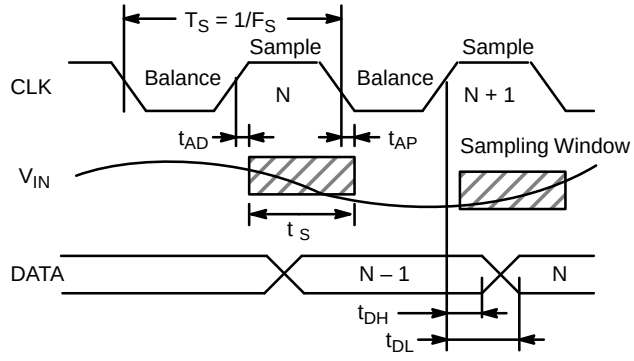


Figure 7. Pipeline Mode Timing (7682 compatible)
(Phase = 1, Mode = 1)

The MP76L86 converts analog voltages into 64 digital codes by encoding the outputs of comparators. A comparator is used to generate the overflow bit. The conversion is synchronous with the sample clock. A complete conversion cycle is accomplished in 1.5 cycles. Data is transferred from the comparator latches to the output register each cycle at the same time the input is sampled.

The clock signal generates the two internal phases, ϕ_B (CLK high = balance) and ϕ_S (CLK low = sample). Phase B connects the comparators to the reference tap points. Phase S connects the comparators to the analog input voltage.

The reference resistance ladder is a series of 65 resistors. The first and the last resistors of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = R \bullet 64$ $V_{REF} = V_{REF(+)} - V_{REF(-)} = 64 \bullet LSB$

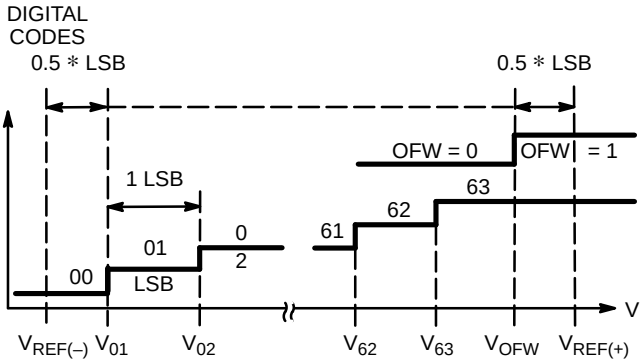


Figure 8. Ideal A/D Transfer Function

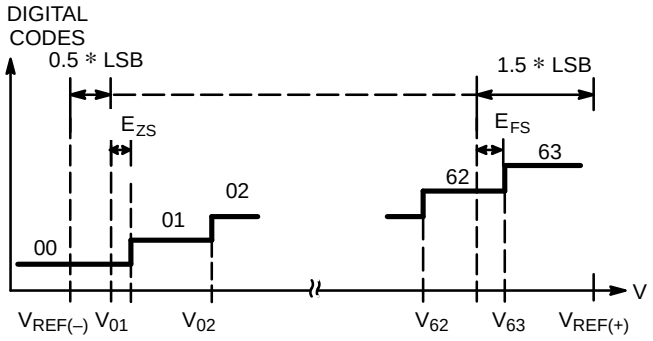


Figure 9. Real A/D Transfer Curve

For MP76L86 the overflow flag is ideally set at

$V_{OFW} = V_{REF(+)} - 0.5 * LSB$

Thus the first and last transition of the data bits take place at

$V_{IN} = V_{01} = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{63} = V_{REF(+)} - 1.5 * LSB$

$LSB = (V_{63} - V_{01}) / 62$

MP76L86 also has zero scale and full scale errors which indicate the deviations from the ideal initial and final transitions, thus

the various error relationships for Differential Non-Linearity (DNL), Integral Non-Linearity (INL) and the zero and full scale errors (E_{ZS} and E_{FS}) can be described as follows:

DNL (01) = $V_{02} - V_{01}$ – LSB

: : :

DNL (62) = $V_{63} - V_{62}$ – LSB

E_{FS} (full scale error) = $V_{63} - [V_{REF(+)} - 1.5 * LSB]$

E_{ZS} (zero scale error) = $V_{01} - [V_{REF(-)} + 0.5 * LSB]$

INL (i) = Σ DNL (i)

Systems that adjust the V_{REF} voltages only increase the DNL accuracy at the two extreme points. In the MP76L86, such adjustments have little impact at frequencies lower than 2.5 MHz.

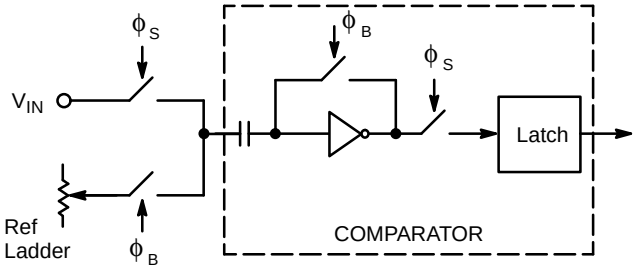


Figure 10. MP76L86 Comparator

The MP76L86 uses the balance phase (ϕ_B) to charge one plate of the capacitors to the reference ladder tap point and the other to the inverter/comparator trigger point (*Figure 10.*). During the sample phase (ϕ_S) one plate of the capacitor switches to V_{IN}. The change in voltage ($V_{IN} - V_{TAP}$) transfers across the capacitor and forces the inverter into one of the two possible logic states. A latch (connected to the comparator during ϕ_S) restores and propagates the digital level to the decode logic.

The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latch from the comparator. This delay is called aperture delay (t_{AP}).

The aperture delay is not constant but changes from one cycle to the next. Internal thermal noise and slow input clock edges are major contributors to this variation. The aperture jitter (t_{AP}) is the variation of the aperture delay distribution.

This uncertainty shows as digital code errors if the input slew rate multiplied by t_{AJ} is of the same order of magnitude as the LSB. That is, if (dv/dt) * $t_{AJ} \approx V_{REF}/64$, an internal 1 LSB of error results.

The logic encodes the 64 bits into a binary code and latches the data in a D-type flip-flop for output. The inputs $\overline{OE1}$ and OE2 control the output buffers in an asynchronous mode.

$\overline{OE1}$	OE2	OFW	DB5-DB0
X	0	High Z	High Z
1	1	Valid	High Z
0	1	Valid	Valid

Table 1. Output Enable Logic

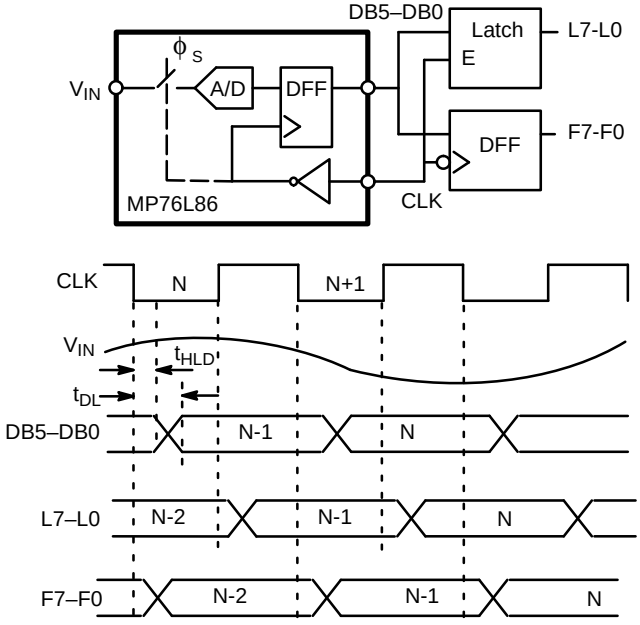


Figure 11. MP76L86 Functional Equivalent Circuit and Interface Timing (Pipeline Mode)

The MP76L86 functional equivalent circuit as shown is to help the designer to correctly design the timing of his system. The MP76L86 is equivalent to an A/D converter followed by a D-type flip-flop (DFF) with the hold and delay times specified in the electrical characteristics.

If another DFF is to follow the ADC, we recommend that the system latches the data at the negative going edge of the clock. If a latch follows the ADC, the positive half of the clock used as enable signal should guarantee stable output at the end of the enable pulse. At high sampling frequencies (F_S > 2.5 MHz), the user should verify in his system that the MP76L86 digital outputs do not change when the digital logic is trying to latch the data. If this problem occurs, it may be necessary to invert the logic state

of the input PHASE or to change the edge that latches the data into the external circuitry.

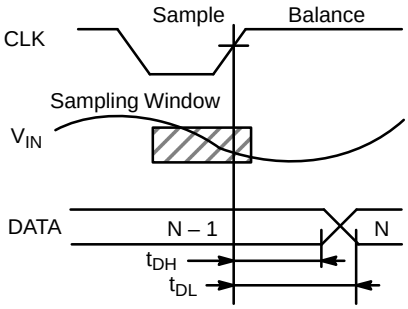


Figure 12. One Shot Mode Timing
(Phase = 0, Mode = 0)

One Shot Mode (Mode = Low, Phase = Low)

While the pipeline mode requires three clock edges (two clock pulses) to accomplish one A/D conversion, the One Shot mode (see *Figure 12.*) requires only two edges (one clock pulse) to complete a conversion.

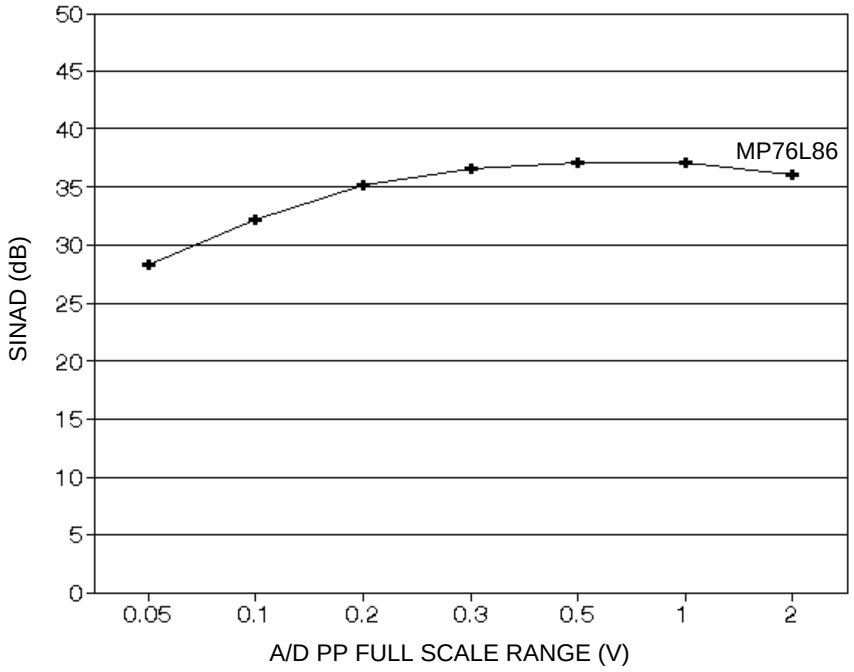
Reserved (Mode = Low, Phase = High)

This mode is not a valid operational mode.

Reference Voltages

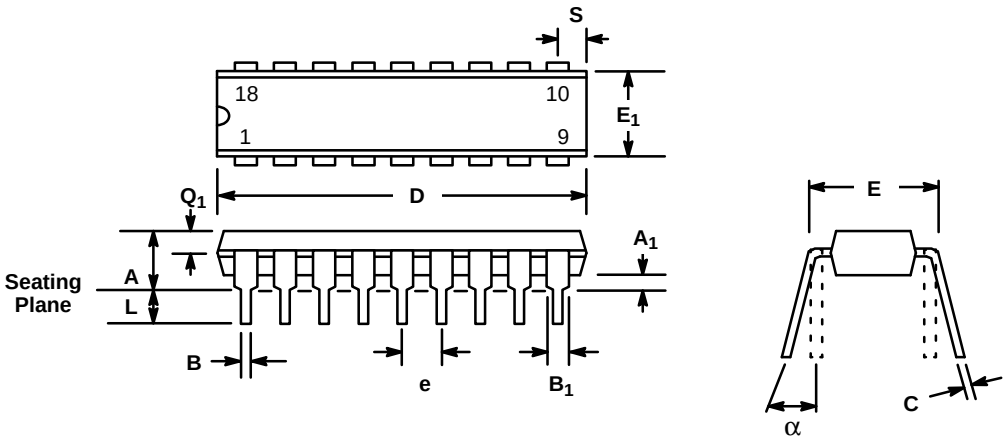
If the input bandwidth is limited to the Nyquist region ($F_{IN} < F_S/2$), then the two reference voltages can be set at any two values between the supplies. V_{REF} (their difference) can be reduced down to 1.5 volts with minor change in accuracy. If the input bandwidth exceeds $F_S/2$, then it is recommended that V_{REF} be lower than $V_{DD}/2$.

PERFORMANCE CHARACTERISTICS



Graph 1. 6-Bit Low Level Input Performance
V_{DD} = 3 V, F_S = 5 MHz, F_{IN} = 100kHz

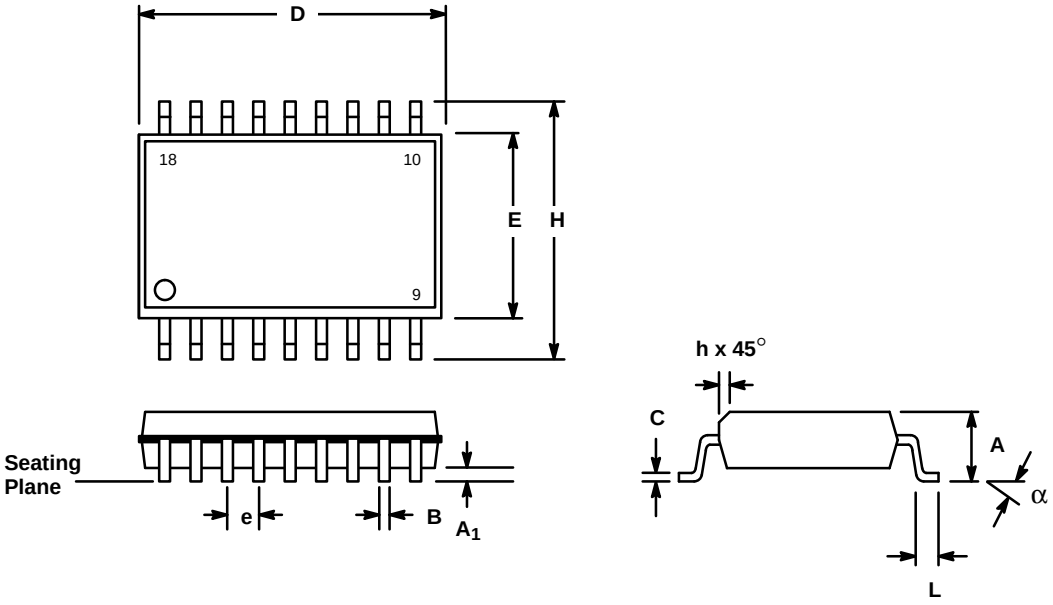
18 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N18



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.845	0.925	21.46	23.50
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.098	1.02	2.49

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

18 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S18



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.641
A_1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.451	0.461	11.46	11.71
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

Notes

NOTICE

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