

FEATURES

- Sampling Rates from 1 kHz to 2 MHz
- DNL better than 1/2 LSB (typ) up to 1 MHz
- Very Low Power CMOS - 30 mW (typ)
- Monotonic; No Missing Codes
- Interface to any Input Range between GND and V_{DD}
- No S/H needed for Input Signals Less Than 10 kHz
- Single Power Supply (4 to 6.5 Volts)
- Latch-Up Free
- High ESD Protection: 4000 Volts Minimum
- For New Designs use MP8784 or MP8795

BENEFITS

- Reduced Board Space (Small Package)
- Reduced External Parts, No Sample/Hold Needed
- Suitable for Battery & Power Critical Applications
- Designer Can Adapt Input Range & Scaling

APPLICATIONS

- Low Power A/D Applications
- High Resolution Imaging
- Multiplexed Data Acquisition
- Radar Pulse Analysis

GENERAL DESCRIPTION

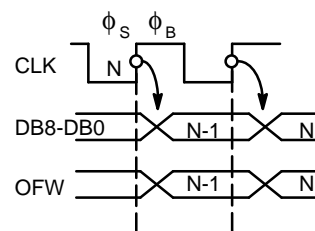
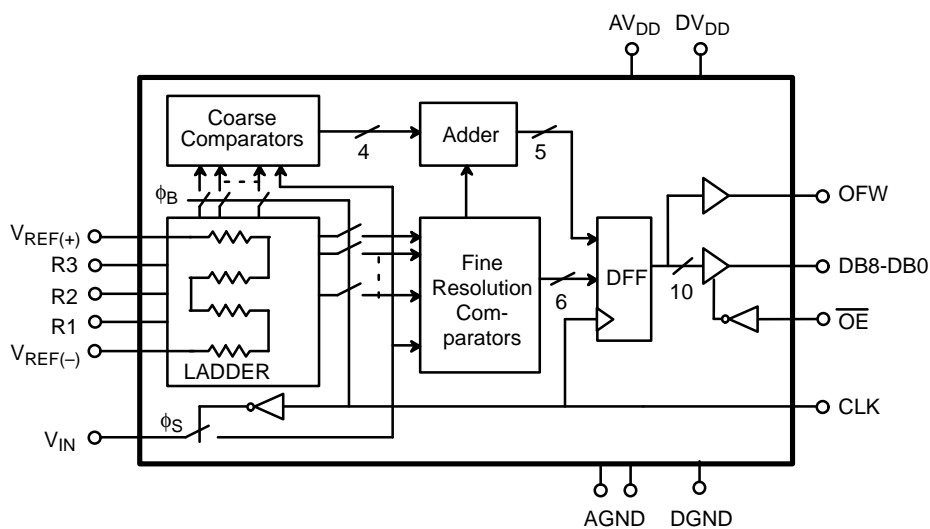
The MP7696 is a 9-bit CMOS Analog-to-Digital Converter designed for precision applications demanding *Low Power Consumption*. The input architecture of the MP7696 allows direct interface to any analog input range between AGND and AV_{DD} (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

The MP7696 uses a two-step flash technique. The first

segment converts the 3 MSBs and consists of 8 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

With 30 mW power dissipation, the MP7696 achieves its excellent performance due to the inherent high speed of our proprietary 2 μ Refractory Molybdenum CMOS Process.

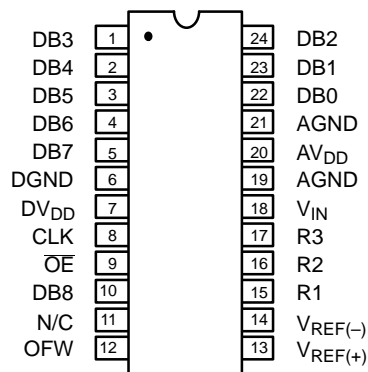
SIMPLIFIED BLOCK AND TIMING DIAGRAM



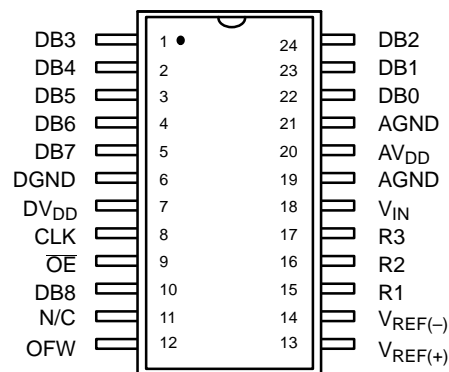
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	-40 to +85°C	MP7696AN	±1	1
SOIC	-40 to +85°C	MP7696AS	±1	1

PIN CONFIGURATIONS



**24 Pin PDIP (0.300")
NN24**



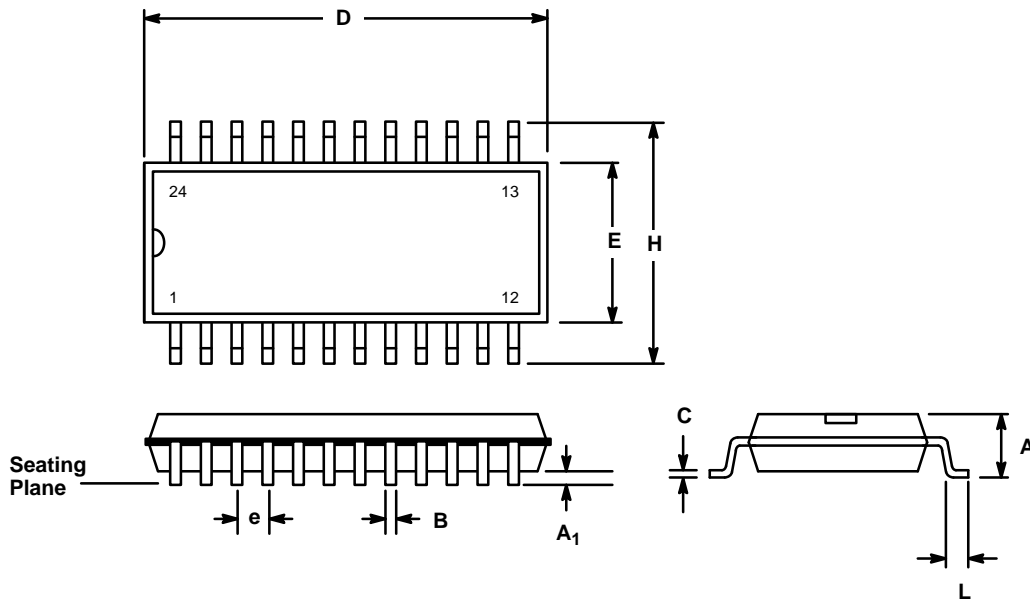
**24 Pin SOIC (EIAJ, 0.335")
R24**

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB3	Data Output Bit 3
2	DB4	Data Output Bit 4
3	DB5	Data Output Bit 5
4	DB6	Data Output Bit 6
5	DB7	Data Output Bit 7
6	DGND	Digital Ground
7	DVDD	Digital VDD
8	CLK	Clock Input
9	OE	Output Enable (Active Low)
10	DB8	Data Output Bit 8 (MSB)
11	N/C	No Connection
12	OFW	Overflow Output

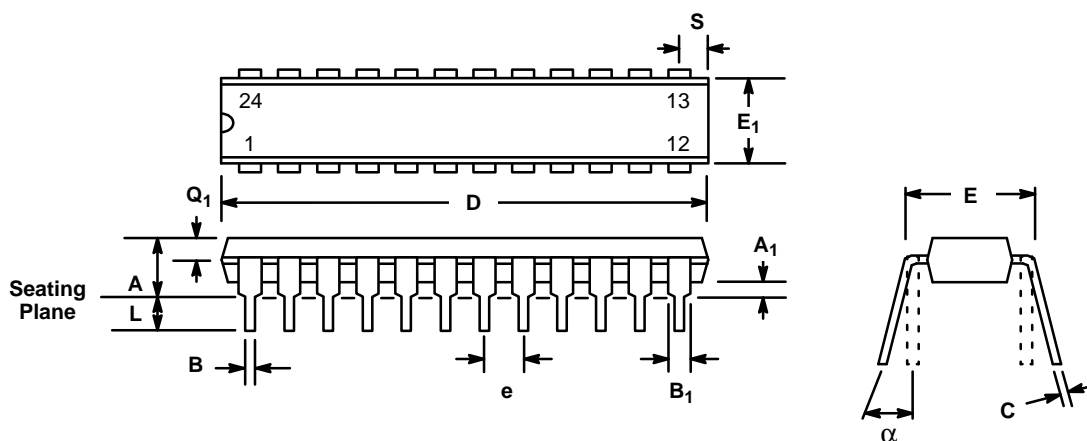
PIN NO.	NAME	DESCRIPTION
13	VREF(+)	Upper Reference Voltage
14	VREF(-)	Lower Reference Voltage
15	R1	Reference Ladder Tap
16	R2	Reference Ladder Tap
17	R3	Reference Ladder Tap
18	VIN	Analog Signal Input
19	AGND	Analog Ground
20	AVDD	Analog VDD
21	AGND	Analog Ground
22	DB0	Data Output Bit 0 (LSB)
23	DB1	Data Output Bit 1
24	DB2	Data Output Bit 2

**24 LEAD SMALL OUTLINE
(335 MIL EIAJ SOIC)
R24**



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.60	2.80	0.102	0.110
A1	0.2 (typ.)		0.008 (typ.)	
B	0.3	0.50	.012	0.020
C	0.10	0.20	0.004	0.008
D	15.0	15.4	0.590	0.606
E	8.3	8.5	0.327	0.335
e	1.27 (typ.)		0.050 (typ.)	
H	11.5	12.1	0.453	0.477
L	0.8	1.2	0.031	0.047

24 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP) NN24



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A ₁	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B ₁ (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.16	1.280	29.46	32.51
E	0.295	0.325	7.49	8.26
E ₁	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q ₁	0.055	0.070	1.40	1.78
S	0.028	0.098	0.711	2.49

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

Notes

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