MP7695

1 MSPS, CMOS
Very Low Power 10-Bit
Analog-to-Digital Converter

FEATURES

- **Sampling Rates from <1 kHz to 2 MHz**
- **DNL better than 1/2 LSB (typ) up to 1 MHz**
- **Very Low Power CMOS - 30 mW (typ)**
- **Monotonic; No Missing Codes**
- **Interface to any Input Range between GND and V_{DD}**
- **No S/H Required for CCD or most Muxed Input Applications**
- **Single Power Supply (4 to 6 volts)**
- **Latch-Up Free**
- **High ESD Protection: 4000 Volts Minimum**
- **Use MP8795 For New Designs**
- **No S/H Required for Signals <25kHz**

BENEFITS

- **Reduced External Parts, No Sample/Hold Needed**
- **Suitable for Battery & Power Critical Applications**
- **Designer Can Adapt Input Range & Scaling**

APPLICATIONS

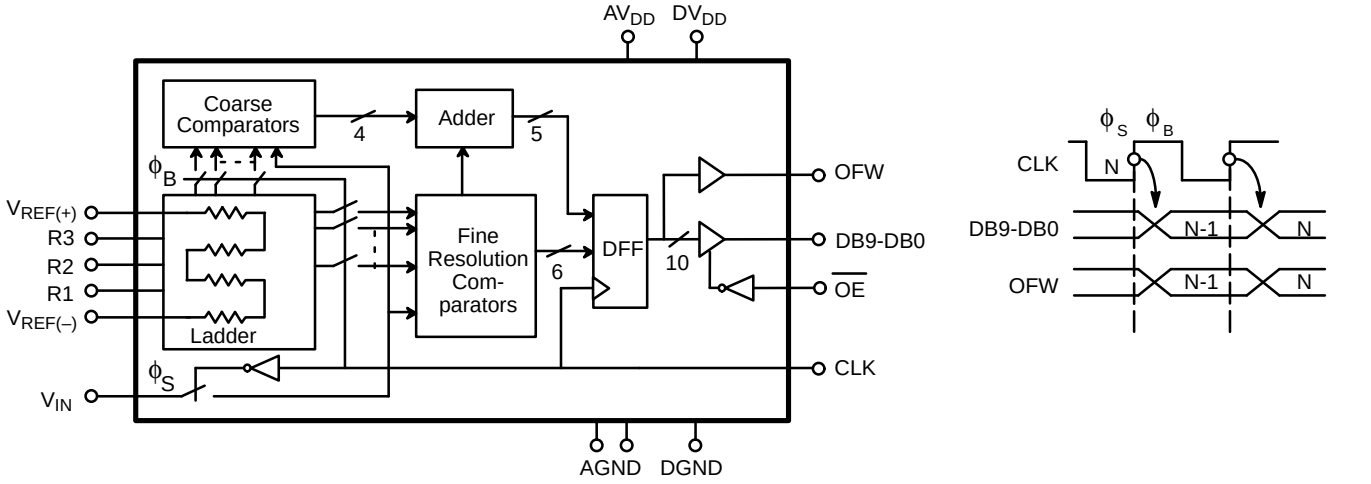
- **µP/DSP Interface and Control Applications**
- **High Resolution Imaging – Scanners, Copiers, Facsimile**
- **Multiplexed Data Acquisition**
- **Radar Pulse Analysis**
- **Low Power A/D Applications**

GENERAL DESCRIPTION

The MP7695 is a flexible, easy to use, precision 10-bit Analog-to-Digital Converter that operates over a wide range of input and sampling conditions. The MP7695 can operate with pulsed "on demand" conversion operation or continuous "pipeline" operation for sampling rates up to 2 MHz. The elimination of S/H, operation of 5 V supply and small board space offer the designer a low cost solution, while also offering very low power consumption (30mW typ.) even at high speed (1 MHz) operation. No sample and hold is required for CCD applications, up to 2 MHz, or multiplexed input applications when the signal source bandwidth is limited to 25 kHz. The input architecture of the MP7695 allows direct interface to any analog input range between AGND and AV_{DD} (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets $V_{REF(+)}$ and $V_{REF(–)}$ to encompass the desired input range.

The MP7695 uses a two-step flash technique. The first segment converts the 4 MSBs and consists of 15 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

SIMPLIFIED BLOCK AND TIMING DIAGRAM



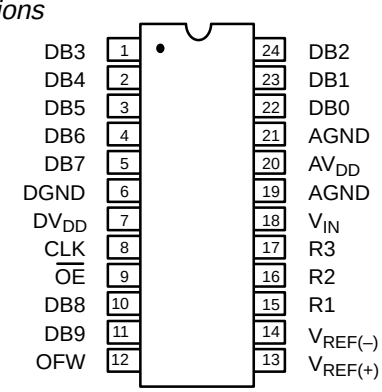
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP7695AN	±1	1 1/4
SOIC	–40 to +85°C	MP7695AS	±1	1 1/4
Ceramic Dip	–40 to +85°C	MP7695AD	±1	1 1/4
Ceramic Dip	–55 to +125°C	MP7695SD*	±1	1 1/4

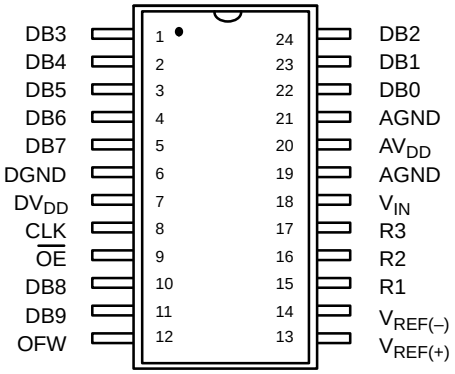
*Contact factory for non-compliant military processing

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin CDIP, PDIP (0.300")
DN24, NN24



24 Pin SOIC (EIAJ, 0.335")
R24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB3	Data Output Bit 3
2	DB4	Data Output Bit 4
3	DB5	Data Output Bit 5
4	DB6	Data Output Bit 6
5	DB7	Data Output Bit 7
6	DGND	Digital Ground
7	DV_{DD}	Digital V_{DD}
8	CLK	Clock Input
9	$\overline{OE}$	Output Enable (Active Low)
10	DB8	Data Output Bit 8
11	DB9	Data Output Bit 9 (MSB)
12	OFW	Overflow Output

PIN NO.	NAME	DESCRIPTION
13	$V_{REF(+)}$	Upper Reference Voltage
14	$V_{REF(–)}$	Lower Reference Voltage
15	R1	Reference Ladder Tap
16	R2	Reference Ladder Tap
17	R3	Reference Ladder Tap
18	V_{IN}	Analog Signal Input
19	AGND	Analog Ground
20	AV_{DD}	Analog V_{DD}
21	AGND	Analog Ground
22	DB0	Data Output Bit 0 (LSB)
23	DB1	Data Output Bit 1
24	DB2	Data Output Bit 2

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, F_S = 1 MHz (50% Duty Cycle), $V_{REF(+)}$ = 4.6, $V_{REF(–)}$ = AGND, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		10			10		Bits	
Sampling Rate	F_S	.001		1	.001	1	MHz	For Rated Performance
ACCURACY[2]								
Differential Non-Linearity	DNL							
AN, AS, AD				±3/4		±3/4	LSB	99.2% of Codes
				±1 1/4		±1 1/4	LSB	100% of Codes
Integral Non-Linearity	INL							
AN, AS, AD			±3/4	2		2	LSB	Best Fit Line
Zero Scale Error	EZS		±2				mV	
Full Scale Error	EFS		±10				mV	
DYNAMIC ACCURACY[1]								Histogram Test
Differential Non-Linearity	DNL		±1/2				LSB	F_{IN} = 7 kHz
	DNL		±1				LSB	F_{IN} = 10 kHz
REFERENCE VOLTAGES								
Positive Ref. Voltage	$V_{REF(+)}$			AV_{DD}		AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(–)}$	AGND			AGND		V	
Differential Ref. Voltage[5]	V_{REF}	2.0		V_{DD}	3.0	V_{DD}	V	
Ladder Resistance	R_L	525	675	900	475	1200	Ω	
Ladder Temp. Coefficient[1]	R_{TCO}					3000	ppm/°C	
ANALOG INPUT[1]								
Input Voltage Range[7]	V_{IN}	$V_{REF(–)}$		$V_{REF(+)}$	$V_{REF(–)}$	$V_{REF(+)}$	V	
Input Capacitance[3]	C_{IN}		60				pF	
Aperture Delay	t_{AP}		35				ns	
DIGITAL INPUTS								
Logical “1” Voltage	V_{IH}	2.0			2.0		V	
Logical “0” Voltage	V_{IL}			0.8		0.8	V	
Leakage Currents	I_{IN}							V_{IN}=DGND to DV_{DD}
CLK				±100		±100	µA	
$\overline{OE}$ (Internal Res to GND)		–5		30	–5	30	µA	
Input Capacitance			5				pF	
Clock Timing (*See Figure 1.*)[1]								
Clock Period	t_S	1000			1000		ns	
Rise & Fall Time[4]	t_R, t_F			10		10	ns	
“High” Time[6]	t_B	500		500,000	500	500,000	ns	
“Low” Time[6]	t_S	500		500,000	500	500,000	ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS								C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	DV_{DD}-0.5			DV_{DD}-0.5		V	I_{LOAD} = 2 mA
Logical "0" Voltage	V_{OL}			0.4		0.4	V	I_{LOAD} = 4 mA
Tristate Leakage	I_{OZ}	0		±5		±10	µA	V_{OUT} = DGND to DV_{DD}
Data Hold Time (*See Figure 1.*)[1]	t_{HLD}		30		20		ns	
Data Valid Delay[1]	t_{DL}		70			90	ns	
Data Enable Delay[1]	t_{DEN}		25			50	ns	
Data Tristate Delay[1]	t_{DHZ}		15			35	ns	
POWER SUPPLIES[8]								
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4	5	6.5	4	6.5	V	
Current (AV_{DD} + DV_{DD})	I_{DD}		6	10		12	mA	V_{IN} = 2 V

NOTES:

1 Guaranteed. Not tested.

2 Tester measures code transition voltages by dithering the voltage of the analog input (V_{IN}). The difference between the measured code width and the ideal value (V_{REF}/1024) is the DNL error (*see Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*See Figure 4.*).

3 See V_{IN} input equivalent circuit (*see Figure 5.*).

4 Clock specification to meet aperture specification (t_{AP}). Actual rise/fall time can be less stringent with no loss of accuracy.

5 Specified values guarantee functional device. Refer to other parameters for accuracy.

6 System can clock MP7695 with any duty cycle as long as all timing conditions are met.

7 Input range where input is converted correctly into binary code. Input voltage outside specified range converts to zero or full scale output.

8 AV_{DD} & DV_{DD} are connected through silicon substrate. Connect together at package.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} (to GND) ..... +7 V

$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND –0.5 to V_{DD} +0.5 V

V_{IN} ..... GND –0.5 to V_{DD} +0.5 V

All Inputs ..... GND –0.5 to V_{DD} +0.5 V

All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C

Lead Temperature (Soldering 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C

CDIP, PDIP, SOIC 1000mW

Derates above 75°C ..... 13mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

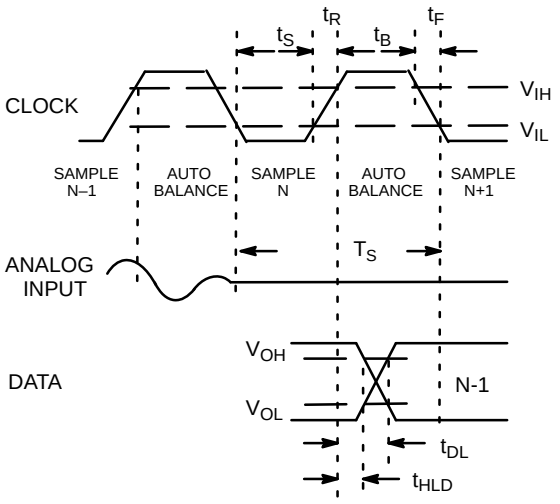


Figure 1. MP7695 Timing Diagram

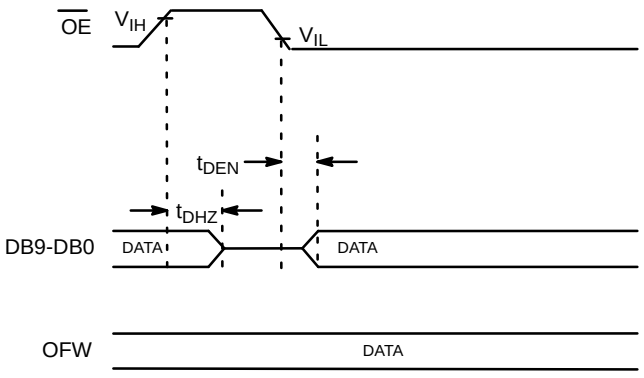
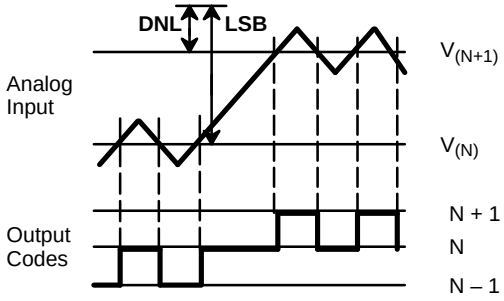


Figure 2. Output Enable/Disable Timing Diagram



(N+1) Code Width = $V_{(N+1)} – V_{(N)}$
LSB = [$V_{REF(+)} – V_{REF(–)}$] / 1024

$DNL_{(N)} = [V_{(N+1)} – V_{(N)}] – LSB$

Figure 3. DNL Measurement On Production Tester

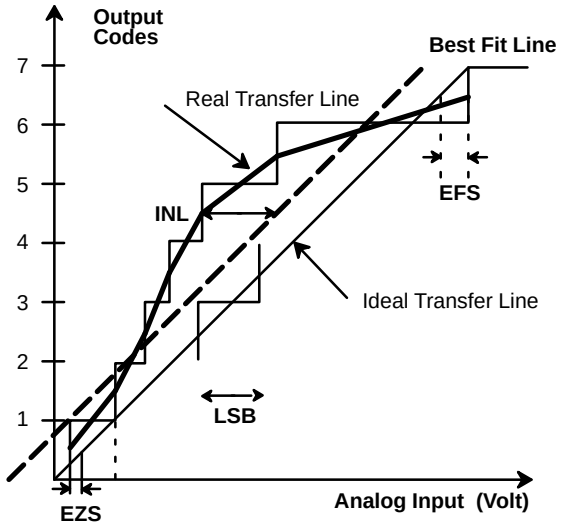


Figure 4. INL Error Calculation

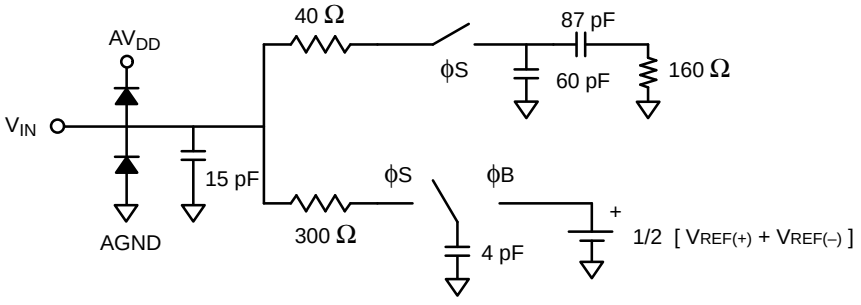


Figure 5. Analog Input Equivalent Circuit

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP7695 converts analog voltages into 1024 digital codes by encoding the outputs of 15 coarse and 67 fine comparators. Digital logic is used to generate the overflow bit. The conversion is synchronous with the clock and is accomplished in 2 clock periods.

The reference resistance ladder is a series of 1025 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 1024 * R \quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 1024 * LSB$

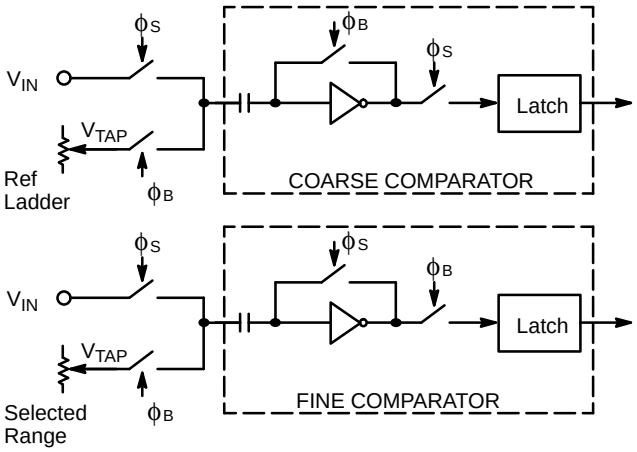


Figure 6. MP7695 Comparators

The clock signal generates the two internal phases, ϕ_B (CLK high) and ϕ_S (CLK low = sample) (*See Figure 6.*). The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The coarse comparators make the first pass conversion and select a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next ϕ_B phase.

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 7.*

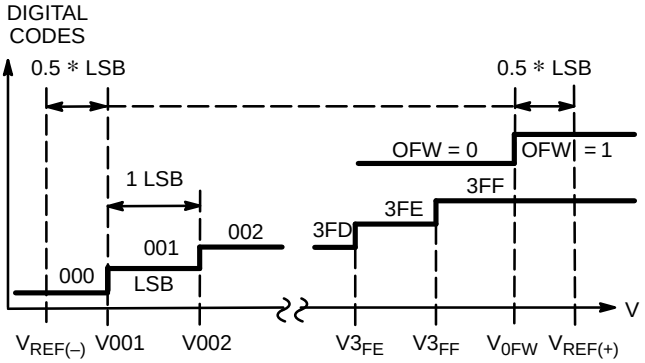


Figure 7. Ideal A/D Transfer Function

The overflow transition (V_{OFW}) takes place at:

$V_{IN} = V_{OFW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V001 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V3_{FF} = V_{REF(+)} - 1.5 * LSB$

$LSB = V_{REF} / 1024 = (V3_{FF} - V001) / 1022$

Note that the overflow transition is a flag and has no impact on the data bits.

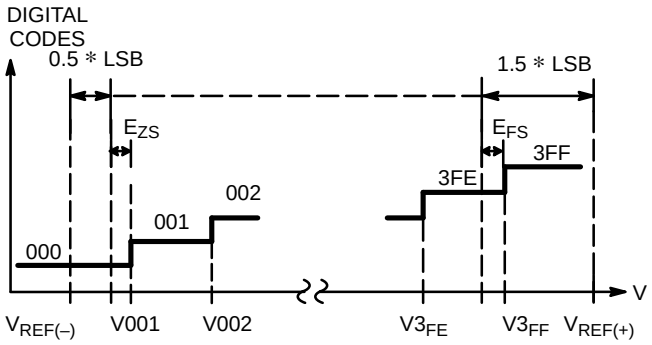


Figure 8. Real A/D Transfer Curve

In a "real" converter, the code-to-code transitions don't fall exactly every $V_{REF}/1024$ volts.

A positive DNL (Differential-Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSB's.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = $\pm$ 0.5 LSB means that all code widths are within 0.5 and 1.5 LSB. If V_{REF} = 4.608 V then 1 LSB = 4.5 mV and every code width is within 2.25 and 6.75 mV.

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (E_{ZS}, E_{FS}) are:

DNL (001) = V002 – V001 – LSB

: : :

DNL (3FE) = $V3_{FF} - V3_{FE}$ – LSB

E_{FS} (full scale error) = $V3_{FF} - [V_{REF(+)} - 1.5 * LSB]$

E_{ZS} (zero scale error) = $V_{001} - [V_{REF(-)} + 0.5 * LSB]$

Figure 8. shows the zero scale and full scale error terms.

Figure 4. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, the computer draws a line parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and and the negative INL errors. For example, an INL error of –1 to +2 LSB's relative to the Ideal Line would be ±1.5 LSB's relative to the Best Fit Line.

Clock and Conversion Timing

A system will clock the MP7695 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 9a* shows normal operation, while the timing of *Figure 9b* keeps the MP7695 in balance and ready to sample the analog input.

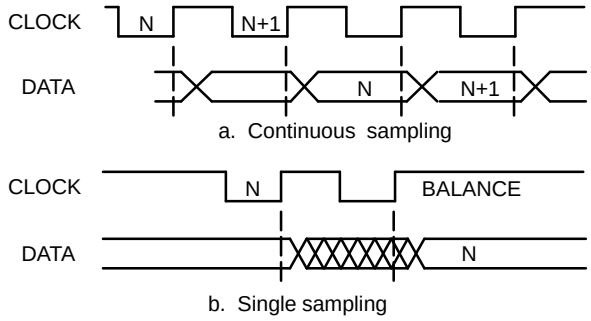


Figure 9. Relationship of Data to Clock

Analog Input

The MP7695 has very flexible input range characteristics. The user may set $V_{REF(+)}$ and $V_{REF(–)}$ to two fixed voltages and then vary the input DC and AC levels to match the V_{REF} range. Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP7695's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. *NO TAG* shows the equivalent circuit for A_{IN}.

Reference Voltages

The input/output relationship is a function of V_{REF}:

$$A_{IN} = V_{IN} – V_{REF(–)}$$
$$V_{REF} = V_{REF(+)} – V_{REF(–)}$$
$$DATA = 1023 * (A_{IN}/V_{REF})$$

A system can increase total gain by reducing V_{REF}.

Digital Interfaces

The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output. The input $\overline{OE}$ controls the output buffers in an asynchronous mode.

$\overline{OE}$	OFW	DB9 – DB0
1	Valid	High Z
0	Valid	Valid

Table 1. Output Enable Logic

The functional equivalent of the MP7695 (*Figure 10.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An ideal analog switch which samples V_{IN}.
3) An ideal A/D which tracks and converts V_{IN} with no delay.
4) A series of two DFF's with specified hold (t_{HLD}) and delay (t_{DL}) times.

t_{AP}, t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

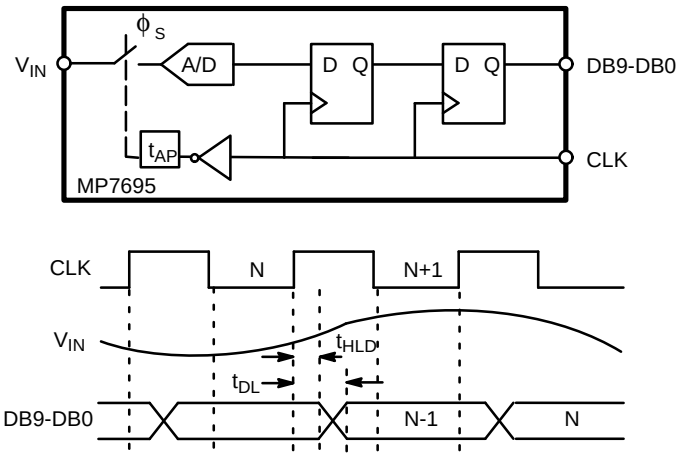
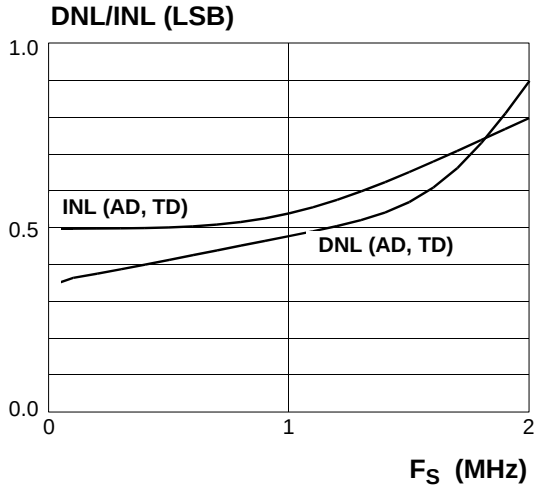


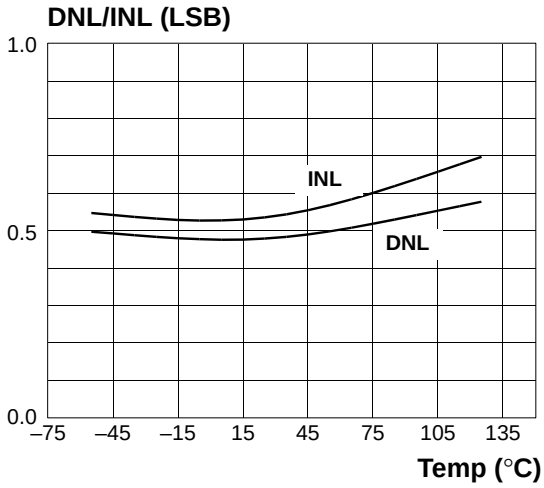
Figure 10. MP7695 Functional Equivalent Circuit and Interface Timing

CHARACTERIZATION CHARTS

(Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 5$ V, $F_S =$ 1 MHz (50% Duty Cycle), $V_{REF(+)} = 4.6$, $V_{REF(-)} =$ AGND, $T_A = 25°C$



Accuracy (DNL/INL)
vs. Sampling Rate (F_S)



Accuracy (DNL/INL)
vs. Ambient Temperature (T)

APPLICATION NOTES

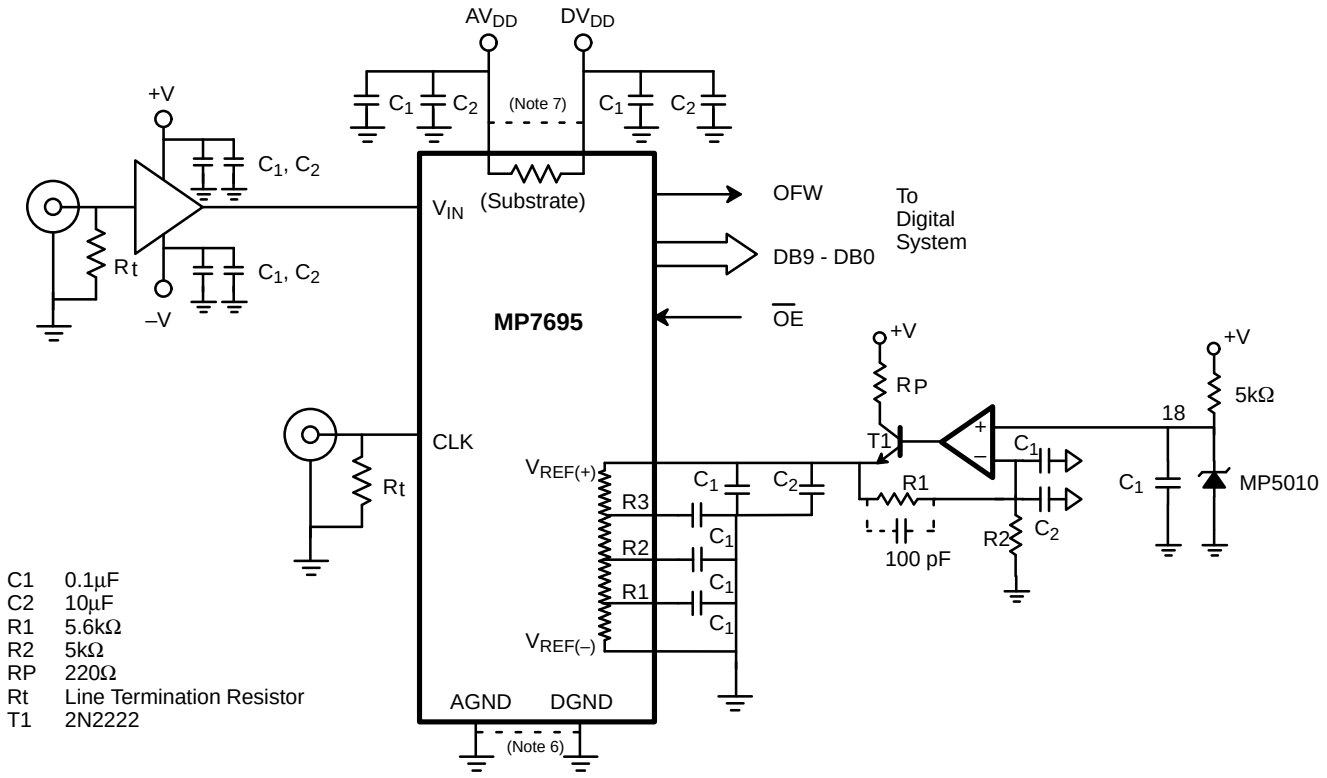
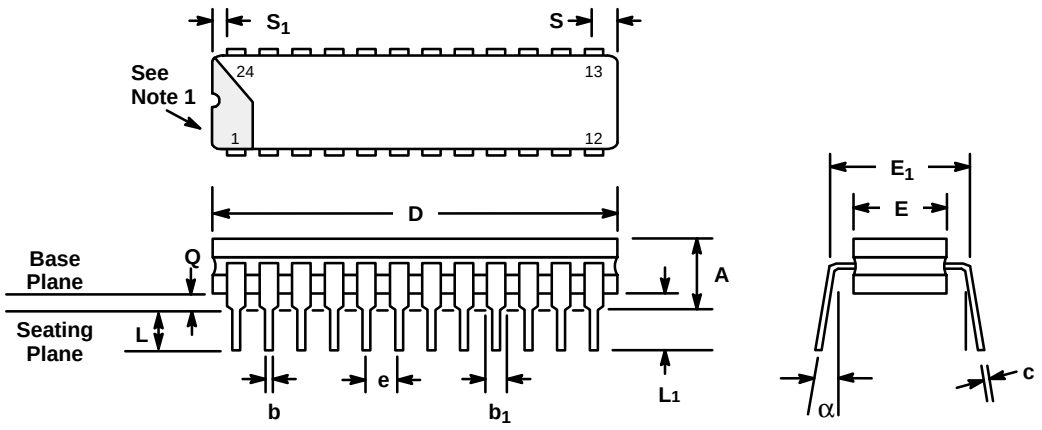


Figure 11. Typical Circuit Connections

The following information will be useful in maximizing the performance of the MP7695.

1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V or DGND –0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP7684A inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP7695. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths. *DGND should not be shared with other digital circuitry.* If separate low impedance paths cannot be provided, DGND should be connected to AGND next to the MP7695.
7. *DV_{DD} should not be shared with other digital circuitry* to avoid conversion errors caused by digital supply transients. DV_{DD} for the MP7695 should be connected to AV_{DD} next to the MP7695.
8. DV_{DD} and AV_{DD} are connected inside the MP7695 through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used.

24 LEAD CERAMIC DUAL-IN-LINE
(300 MIL CDIP)
DN24

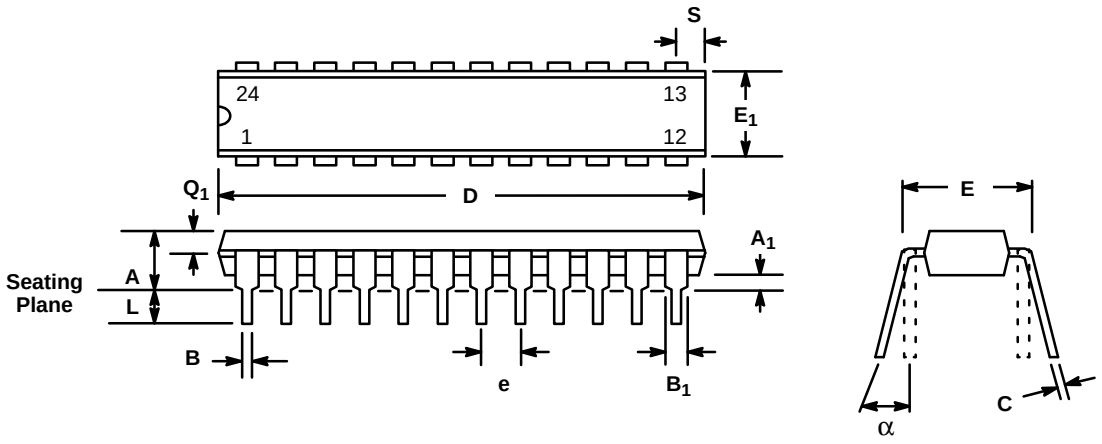


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	1.280	—	32.51	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.381	1.52	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

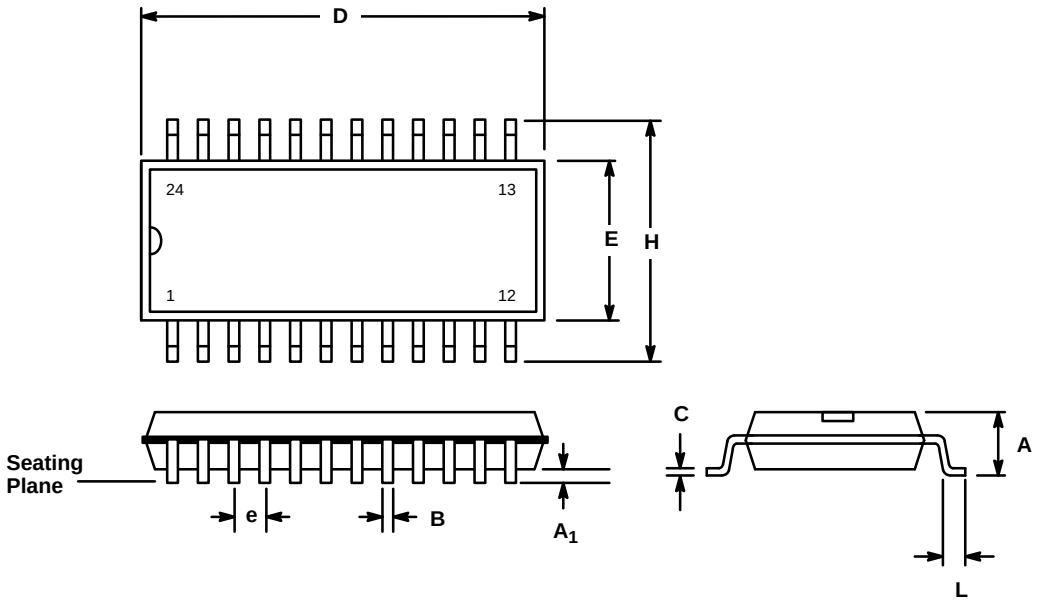
24 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
NN24



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.16	1.280	29.46	32.51
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.028	0.098	0.711	2.49

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

24 LEAD SMALL OUTLINE
(335 MIL EIAJ SOIC)
R24



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.60	2.80	0.102	0.110
A1	0.2 (typ.)		0.008 (typ.)	
B	0.3	0.50	.012	0.020
C	0.10	0.20	0.004	0.008
D	15.0	15.4	0.590	0.606
E	8.3	8.5	0.327	0.335
e	1.27 (typ.)		0.050 (typ.)	
H	11.5	12.1	0.453	0.477
L	0.8	1.2	0.031	0.047

Notes

Notes

Notes

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