MP7693

CMOS
Low Power 8-Bit
Analog-to-Digital Converter

FEATURES

- **Sampling Rates from 1 kHz to 2.5 MHz**
- **DNL better than 1/2 LSB (typ) up to 3 MHz**
- **Low Power CMOS - 75 mW at 5 V**
- **Monotonic; No Missing Codes**
- **Interface to any Analog Input Range between GND and V_{DD}**
- **No S/H needed for CCD Outputs or Input Signals less than100 kHz**
- **Single Power Supply**
- **ESD Protection to 2000 Volts**
- **Latch-Up Free**

BENEFITS

- **Reduced Board Space (Small Package)**
- **Reduced External Parts, No Sample/Hold Needed**
- **Suitable for Battery & Power Critical Applications**
- **Designer can Adapt Input Range & Scaling**

APPLICATIONS

- **Low Power A/D Applications**
- **High Resolution Imaging**
- **Multiplexed Data Acquisition**
- **Radar Pulse Analysis**

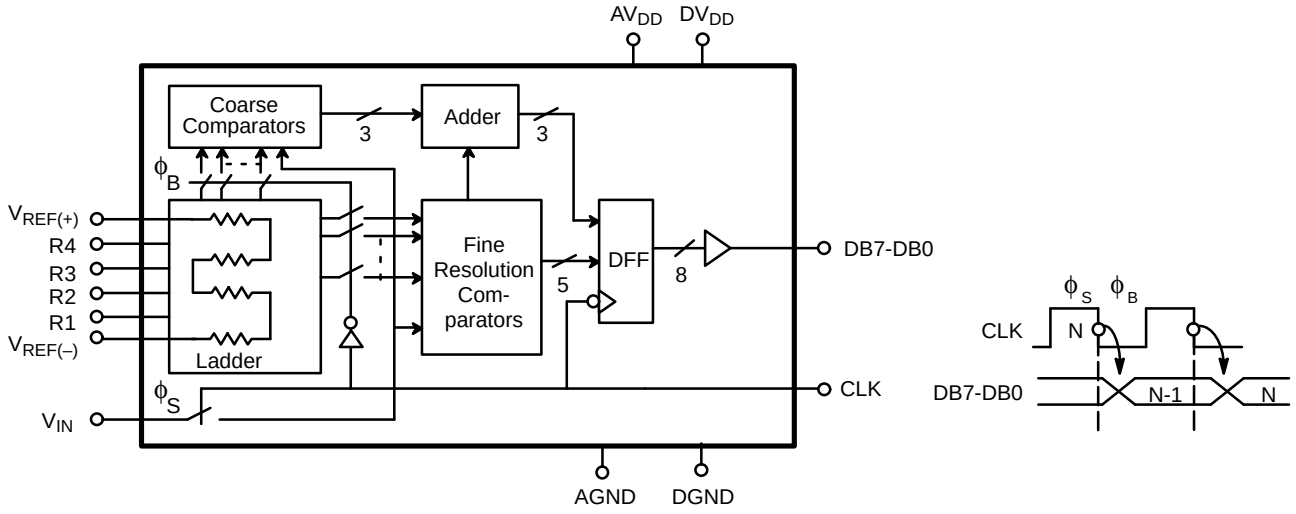
GENERAL DESCRIPTION

The MP7693 is an 8-bit monolithic CMOS Analog-to-Digital Converter designed for precision applications demanding low power consumption and fast conversion. The input architecture of the MP7693 allows direct interface to any analog input range between AGND and AVDD (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets VREF(+) and VREF(–) to encompass the desired input range.

The MP7693 uses a two-step flash technique. The first segment converts the 3 MSBs and consists of 7 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 5 LSBs.

With 75 mW typical and 100 mW maximum power dissipation, the MP7693 achieves its excellent performance due to the inherent high speed of a proprietary CMOS Process.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

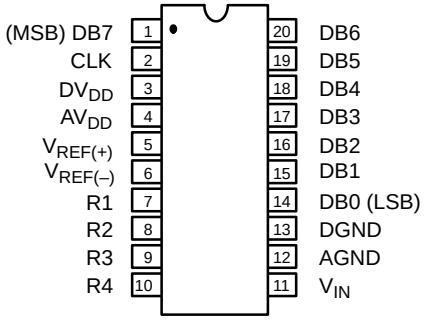


ORDERING INFORMATION

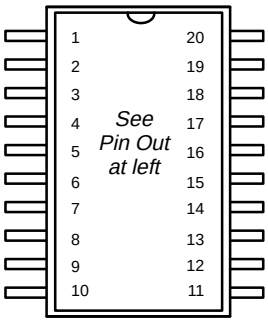
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP7693BN	±3/4	3/4
PLCC	–40 to +85°C	MP7693BP	±3/4	3/4
SOIC	–40 to +85°C	MP7693BS	±3/4	3/4

PIN CONFIGURATIONS

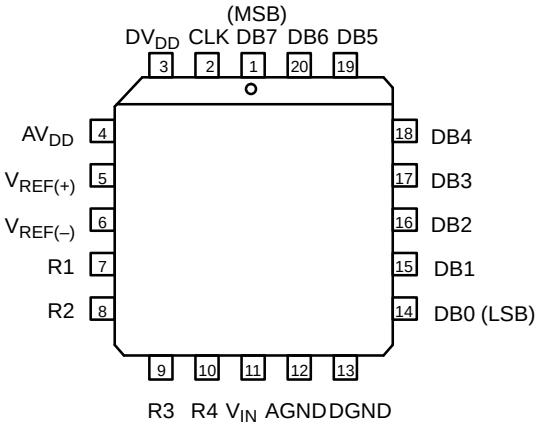
See Packaging Section for Package Dimensions



20 Pin PDIP (0.300")
N20



20 Pin SOIC (Jedec, 0.300")
S20



20 Pin PLCC
P20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB7	Data Output Bit 7 (MSB)
2	CLK	Clock Input
3	DV_{DD}	Power Supply
4	AV_{DD}	Analog Power Supply
5	$V_{REF(+)}$	Upper Ref. Voltage
6	$V_{REF(–)}$	Lower Ref. Voltage
7	R1	Ref. Ladder Tap
8	R2	Ref. Ladder Tap
9	R3	Ref. Ladder Tap
10	R4	Ref. Ladder Tap

PIN NO.	NAME	DESCRIPTION
11	V_{IN}	Analog Signal Input
12	AGND	Analog Ground
13	DGND	Digital Ground
14	DB0	Data Output Bit 0 (LSB)
15	DB1	Data Output Bit 1
16	DB2	Data Output Bit 2
17	DB3	Data Output Bit 3
18	DB4	Data Output Bit 4
19	DB5	Data Output Bit 5
20	DB6	Data Output Bit 6

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, F_S = 2.5 MHz (50% Duty Cycle), $V_{REF(+)}$ = 4.1, $V_{REF(–)}$ = GND, T_A = 25°C

Parameter	Symbol	T_A = 25°C Min	Typ	Max	Tmin to Tmax Min	Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		8			8		Bits	
Sampling Rate[1]	F_S	.001		3	.001	3	MHz	
ACCURACY[2]								
Differential Non-Linearity	DNL			±3/4		±3/4	LSB	
Integral Non-Linearity (Relative Accuracy)	INL			±3/4		±3/4	LSB	Best Fit Line (Max INL – Min INL) / 2
Zero Scale Error	EZS		10				mV	
Full Scale Error	EFS		10				mV	
REFERENCE VOLTAGES								
Positive Ref. Voltage	$V_{REF(+)}$			V_{DD}		V_{DD}	V	
Negative Ref. Voltage	$V_{REF(–)}$	GND			GND		V	
Differential Ref. Voltage[5]	V_{REF}	2.0		V_{DD}	2.0	V_{DD}	V	
Ladder Resistance	R_L	500		1500	300	1950	Ω	
Ladder Temp. Coefficient[1]	R_{TCO}					3000	ppm/°C	
ANALOG INPUT[1]								
Input Voltage Range[7]	V_{IN}	$V_{REF(–)}$		$V_{REF(+)}$	$V_{REF(–)}$	$V_{REF(+)}$	V	
Input Capacitance[3]	C_{IN}		50				pF	
Aperture Delay[1]	t_{AP}		55				ns	
DIGITAL INPUTS								
Logical “1” Voltage	V_{IH}	3.5			3.5		V	
Logical “0” Voltage	V_{IL}			1.5		1.5	V	
Leakage Currents	I_{IN}							V_{IN}=GND to V_{DD}
CLK		–10		10	–10	10	µA	
Input Capacitance			5				pF	
Clock Timing (*See Figure 1.*)[1]								
Clock Period	t_S	333			333		ns	
Rise & Fall Time[4]	t_R, t_F			10		10	ns	
“High” Time[6]	t_S	166		500,000	250	500,000	ns	
“Low” Time[6]	t_B	166		500,000	250	500,000	ns	
DIGITAL OUTPUTS								C_{OUT}=15 pF
Logical “1” Voltage	V_{OH}	V_{DD}-0.5			V_{DD}-0.5		V	I_{LOAD} = 1 mA
Logical “0” Voltage	V_{OL}			0.4		0.4	V	I_{LOAD} = 2 mA
Data Hold Time	t_{HLD}	10			10		ns	(*See Figure 1.*) (1)
Data Valid Delay[1]	t_{DL}			55			ns	
POWER SUPPLIES[8]								
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4	5	6	4	6	V	(1)
Current (AV_{DD} + DV_{DD})	I_{DD}		15	20		35	mA	V_{IN} = 2 V

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

NOTES

1 Guaranteed by Design. Not production tested.

2 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured code width and the ideal value (V_{REF}/256) is the DNL error (*Figure 2.*). The INL error is the maximum distance (in LSB's) from the best fit line to any transition voltage (*Figure 3.*).

3 See V_{IN} input equivalent circuit (*Figure 4.*).

4 Clock specification to meet aperture specification (t_{AP}). Actual rise/fall time can be less stringent with no loss of accuracy.

5 Specified values guarantee functionality. Refer to other parameters for accuracy.

6 System can clock MP7693 with any duty cycle as long as all timing conditions are met.

7 Input range where input is converted correctly into binary code. Input voltage outside specified range converts to zero or full scale output.

8 DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} (to GND) . . . . . +7 V

$V_{REF(+)}$ & $V_{REF(–)}$ . . . . . GND –0.5 to V_{DD} +0.5 V

V_{IN} . . . . . GND –0.5 to V_{DD} +0.5 V

All Inputs . . . . . GND –0.5 to V_{DD} +0.5 V

All Outputs . . . . . GND –0.5 to V_{DD} +0.5 V

Storage Temperature . . . . . –65 to +150°C

Lead Temperature (Soldering 10 seconds) . . . . . +300°C

Package Power Dissipation Rating to 75°C

PDIP, PLCC, SOIC 900mW

Derates above 75°C . . . . . 12mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

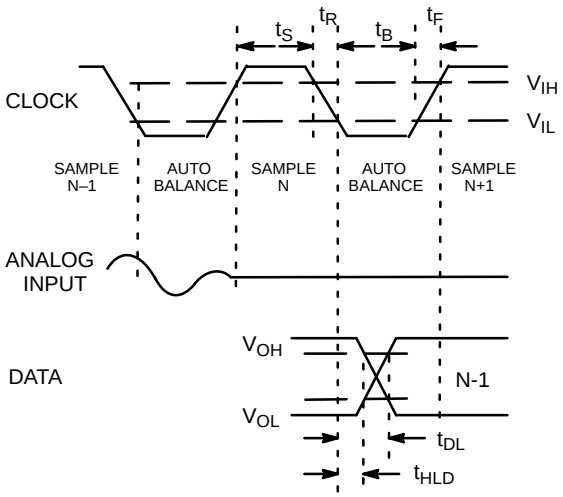
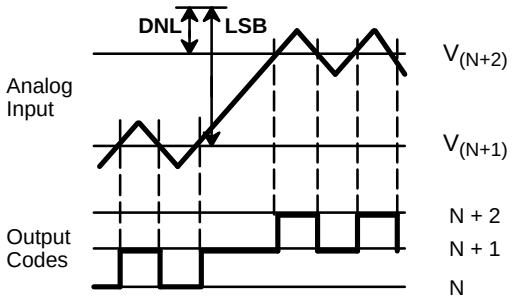


Figure 1. MP7693 Timing Diagram



(N+1) Code Width = $V_{(N+2)} - V_{(N+1)}$
LSB = [$V_{REF(+)} - V_{REF(-)}$] / 256

$DNL_{(N+1)} = [V_{(N+2)} - V_{(N+1)}] - LSB$

Figure 2. DNL Measurement On Production Tester

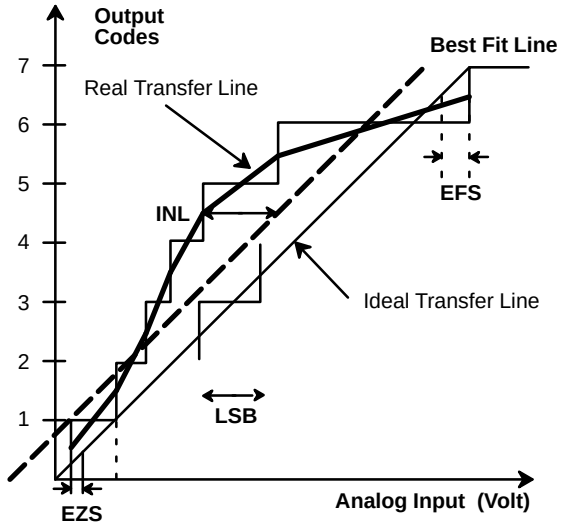


Figure 3. INL Error Calculation

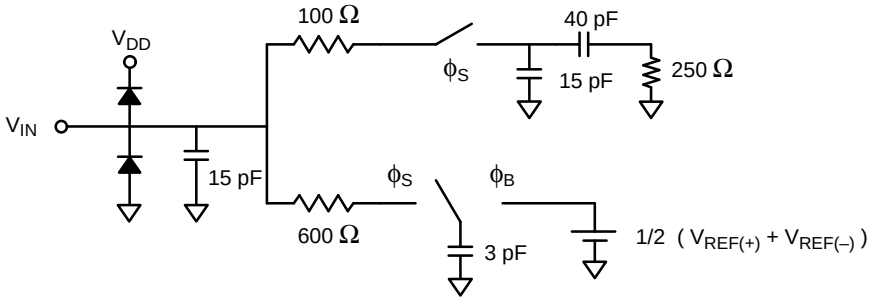


Figure 4. Analog Input Equivalent Circuit

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP7693 converts analog voltages into 256 digital codes by encoding the outputs of 7 coarse and 33 fine comparators. The conversion is synchronous with the clock and is accomplished in 2 clock periods.

The reference resistance ladder is a series of 257 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 256 * R$ $V_{REF} = V_{REF(+)} - V_{REF(-)} = 256 * LSB$

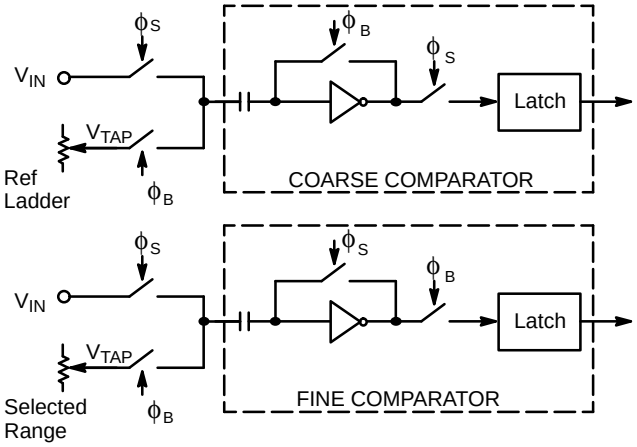


Figure 5. MP7693 Comparators

The clock signal generates the two internal phases, ϕ_B (CLK high) and ϕ_S (CLK low = sample) (*See Figure 5.*). The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The coarse comparators make the first pass conversion and select a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next ϕ_B phase.

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 6.*

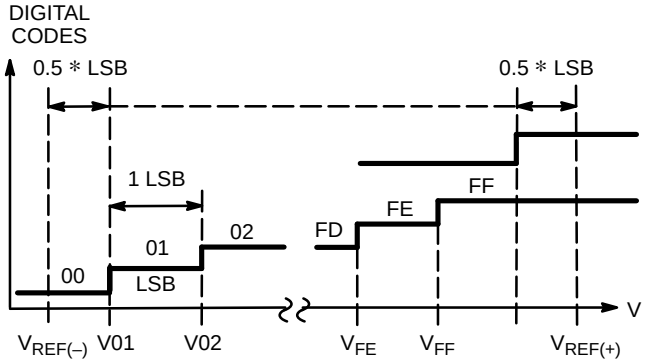


Figure 6. Ideal A/D Transfer Function

The first and the last transitions for the data bits take place at:

$V_{IN} = V001 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{FF} = V_{REF(+)} - 1.5 * LSB$

$LSB = V_{REF} / 256 = (V_{FF} - V01) / 254$

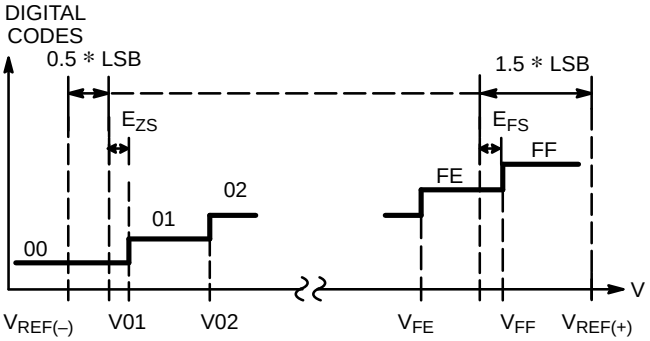


Figure 7. Real A/D Transfer Curve

In a "real" converter, the code-to-code transitions do not fall exactly every $V_{REF}/256$ volts.

A positive DNL (Differential-Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSBs.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = $\pm$0.5 LSB means that all code widths are within 0.5 and 1.5 LSB. If V_{REF} = 4.096 V then 1 LSB = 16.0 mV and every code width is within 8 and 24 mV.

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (EZS, EFS) are:

DNL (01) = V02 – V01 – LSB

: : :

DNL (FE) = $V_{FF} - V_{FE}$ – LSB

E_{FS} (full scale error) = $V_{FF} - [V_{REF(+)} - 1.5 * LSB]$

E_{ZS} (zero scale error) = $V_{01} - [V_{REF(-)} + 0.5 * LSB]$

Figure 7. shows the zero scale and full scale error terms.

Figure 3. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated

DNL errors to show the deviation of the real transfer curve from the ideal one.

After all transition voltages are measured, a best straight line is drawn (*see Figure 3.*) so that the positive INL error equals the negative INL error in magnitude., i.e. best fit line INL = (maximum positive – maximum negative) / 2.

Clock and Conversion Timing

A system will clock the MP7693 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 8a* shows normal operation, while the timing of *Figure 8b* keeps the MP7693 in balance and ready to sample the analog input.

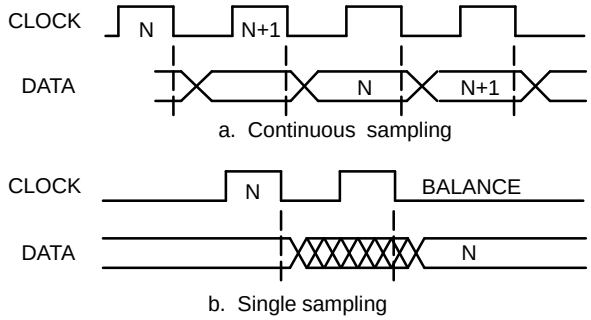


Figure 8. Relationship of Data to Clock

Analog Input

The MP7693 has very flexible input range characteristics. The user may set $V_{REF(+)}$ and $V_{REF(–)}$ to two fixed voltages and then vary the input DC and AC levels to match the V_{REF} range. Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP7693's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. *NO TAG* shows the equivalent circuit for A_{IN}.

Reference Voltages

The input/output relationship is a function of V_{REF}:

$$A_{IN} = V_{IN} – V_{REF(–)}$$
$$V_{REF} = V_{REF(+)} – V_{REF(–)}$$
$$DATA = 255 * (A_{IN}/V_{REF})$$

A system can increase total gain by reducing V_{REF}.

Digital Interfaces

The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output.

The functional equivalent of the MP7693 (*Figure 9.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An ideal analog switch which samples V_{IN}.
3) An ideal A/D which tracks and converts V_{IN} with no delay.
4) A series of two DFF's with specified hold (t_{HLD}) and delay (t_{DL}) times.

t_{AP}, t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

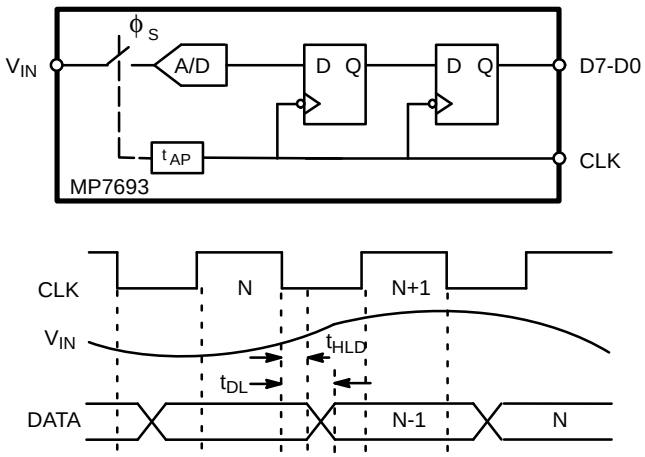


Figure 9. MP7693 Functional Equivalent Circuit and Interface Timing

APPLICATION NOTES

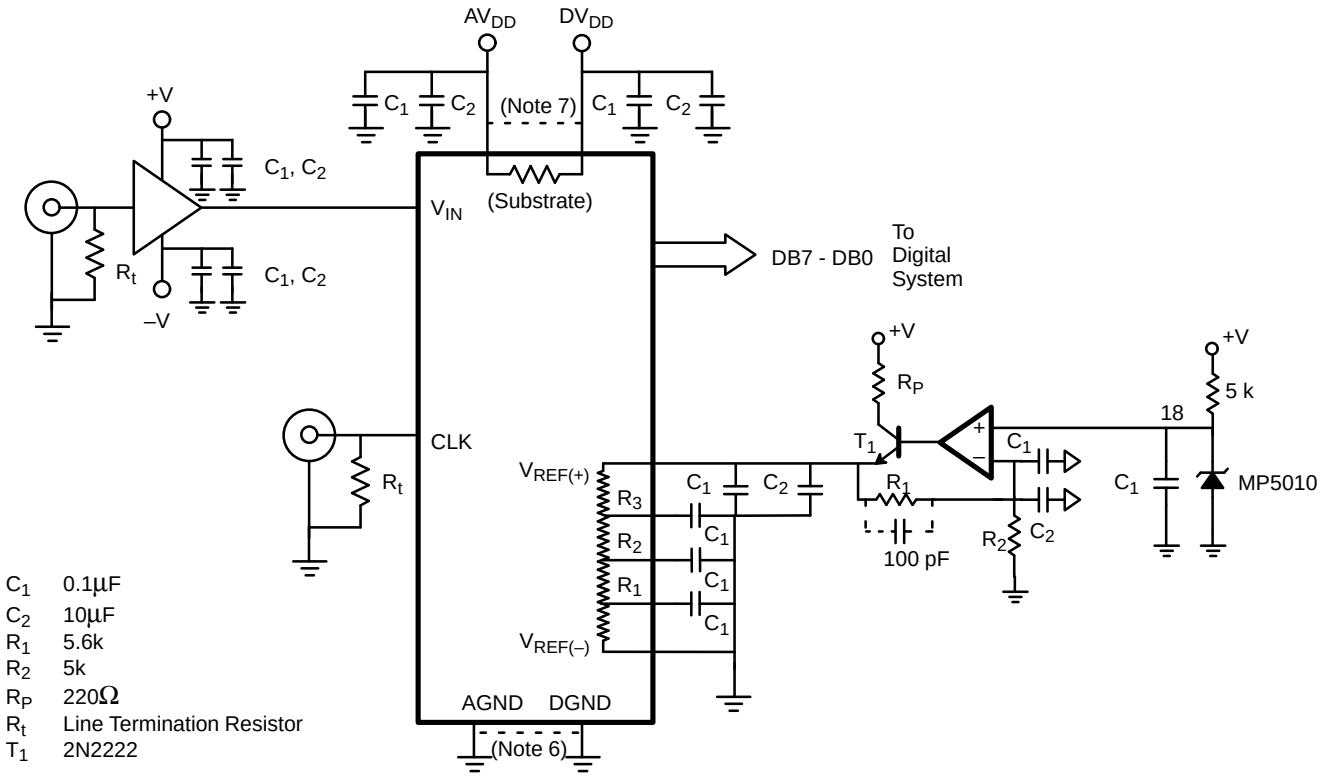
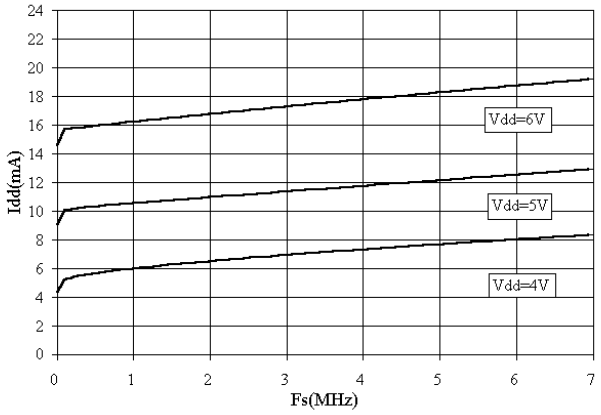


Figure 10. Typical Circuit Connections

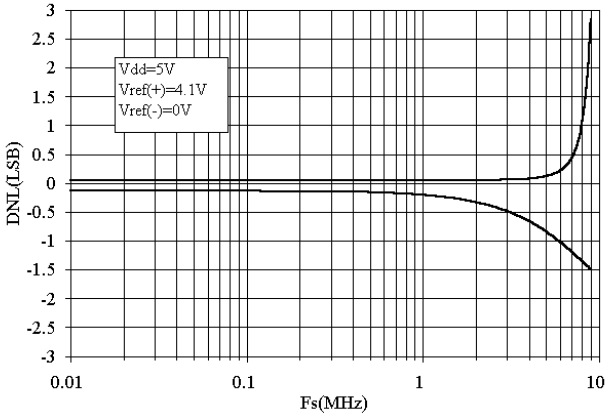
The following information will be useful in maximizing the performance of the MP7693.

1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V or DGND –0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP7684A inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP7693. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. Separate low impedance ground paths will reduce noise levels. *DGND should not be shared with other digital circuitry.* DGND should be connected to AGND next to the MP7693.
7. *DV_{DD} should not be shared with other digital circuitry* to avoid conversion errors caused by digital supply transients. DV_{DD} should be connected to AV_{DD} next to the MP7693.
8. DV_{DD} and AV_{DD} are connected inside the MP7693 through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not be driving long wires as the capacitative coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used.

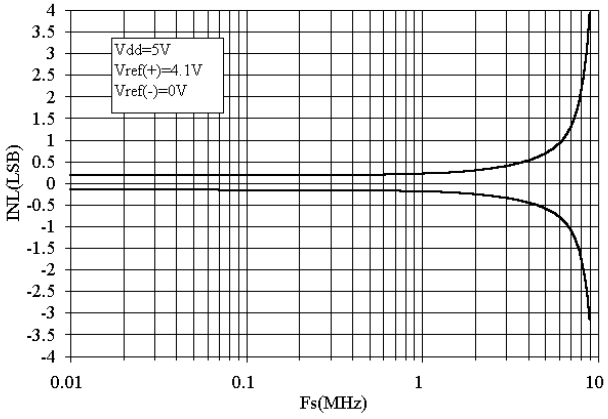
PERFORMANCE CHARACTERISTICS



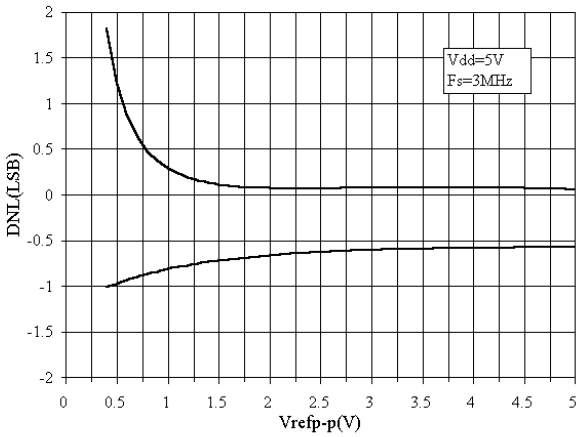
Graph 1. Supply Current vs. Sampling Frequency



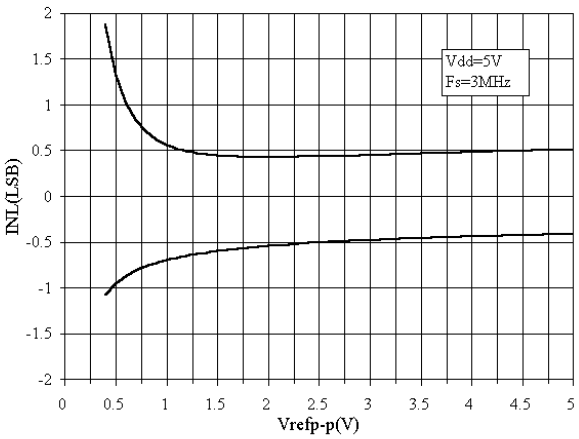
Graph 2. DNL vs. Sampling Frequency



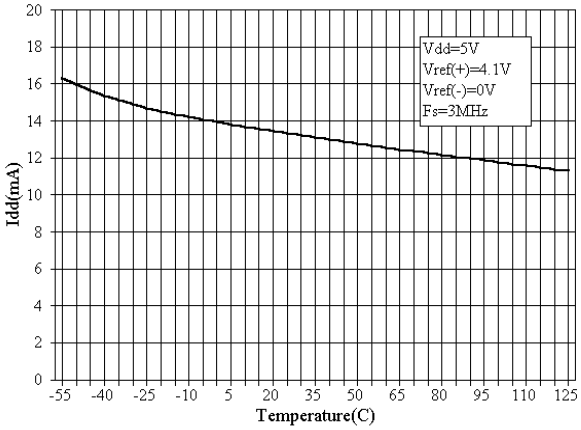
Graph 3. INL vs. Sampling Frequency



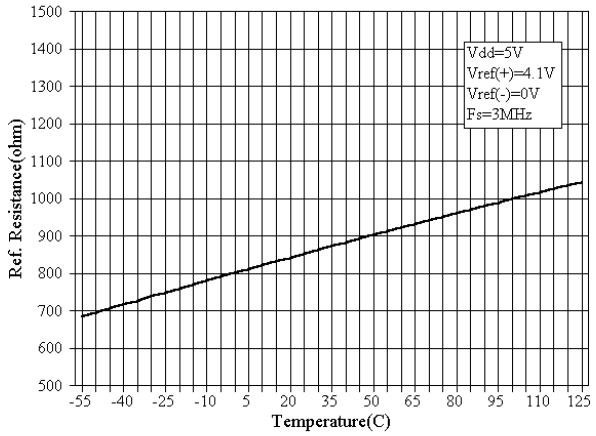
Graph 4. DNL vs. Reference Voltage



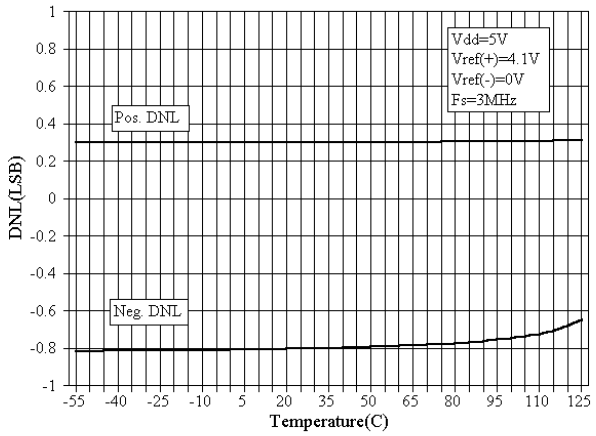
Graph 5. INL vs. Reference Voltage



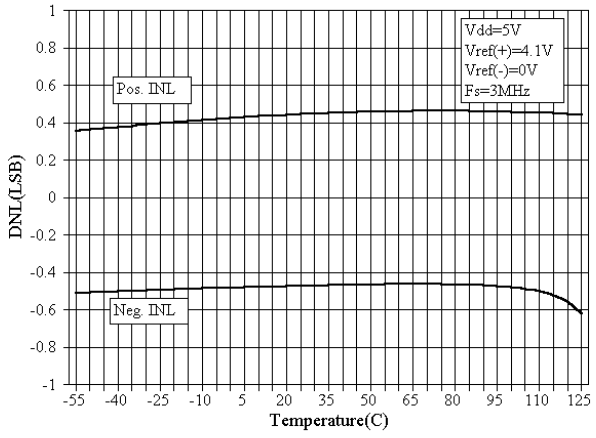
Graph 6. Supply Current vs. Temperature



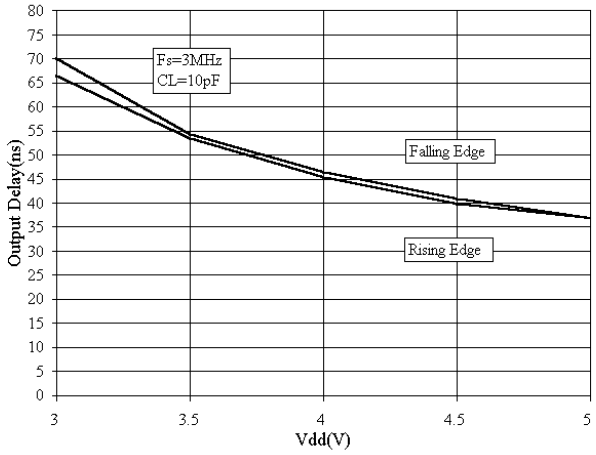
Graph 7. Reference Resistance vs. Temperature



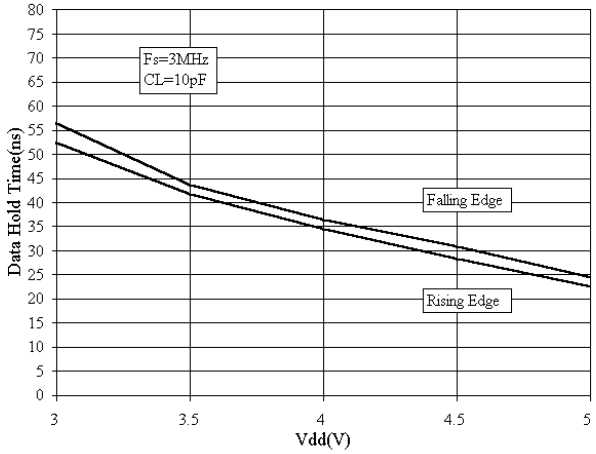
Graph 8. DNL vs. Temperature



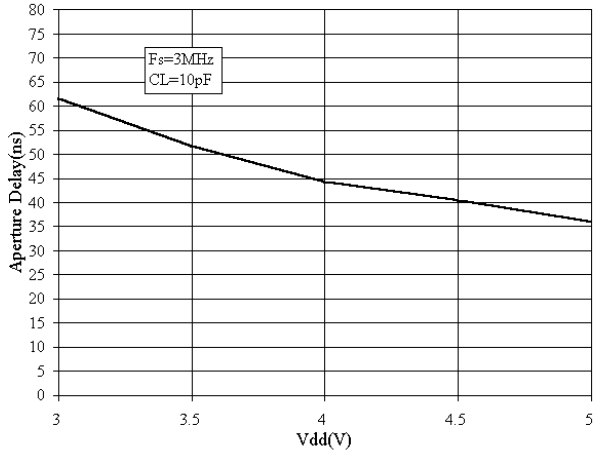
Graph 9. INL vs. Temperature



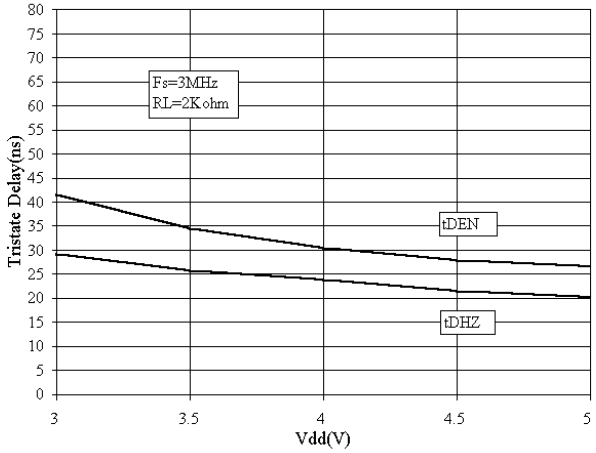
Graph 10. Output Delay vs. Supply Voltage



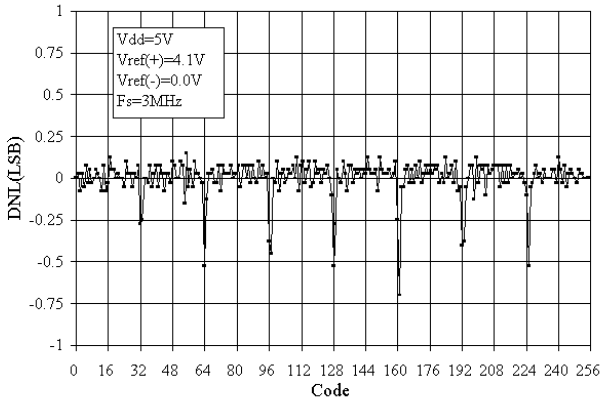
Graph 11. Data Hold Time vs. Supply Voltage



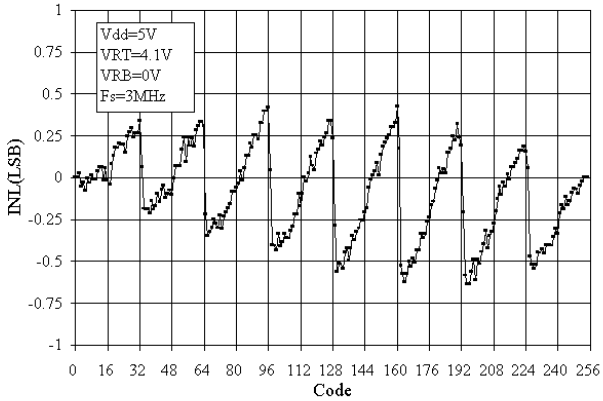
Graph 12. Aperture Delay vs. Supply Voltage



Graph 13. Tristate Enable Delay vs. Supply Voltage



Graph 14. DNL Error Plot



Graph 15. INL Error Plot

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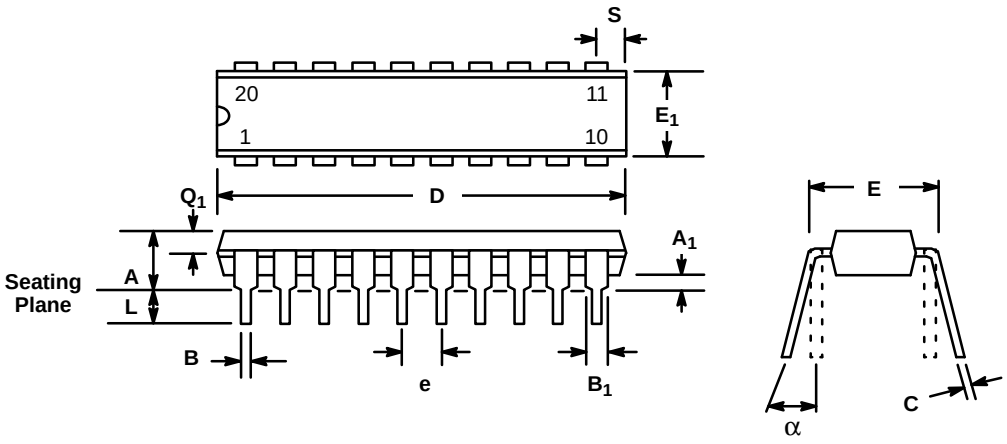
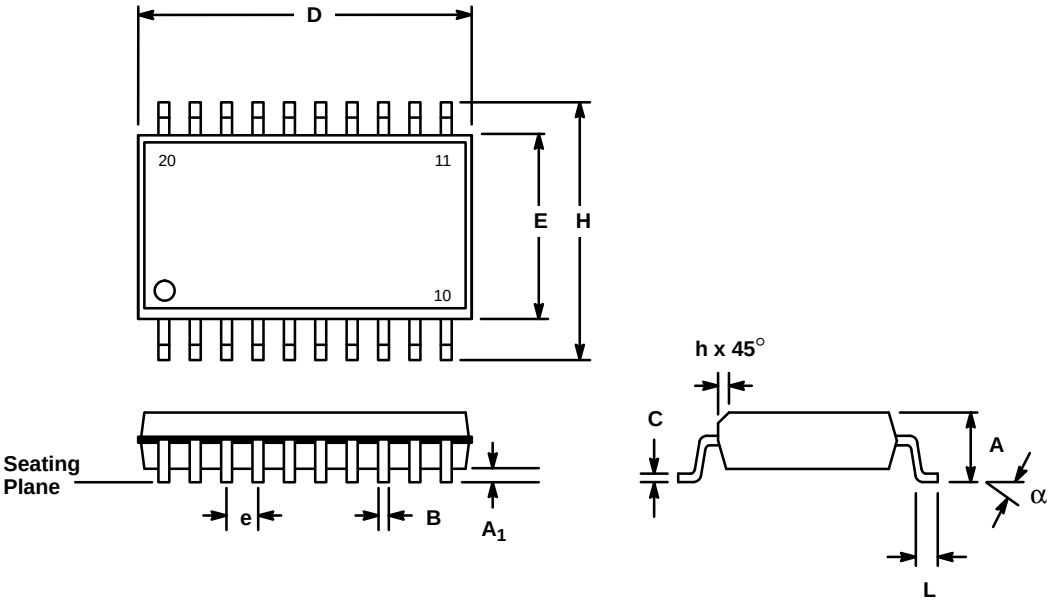
20 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.945	1.060	24.0	26.92
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.080	1.02	2.03

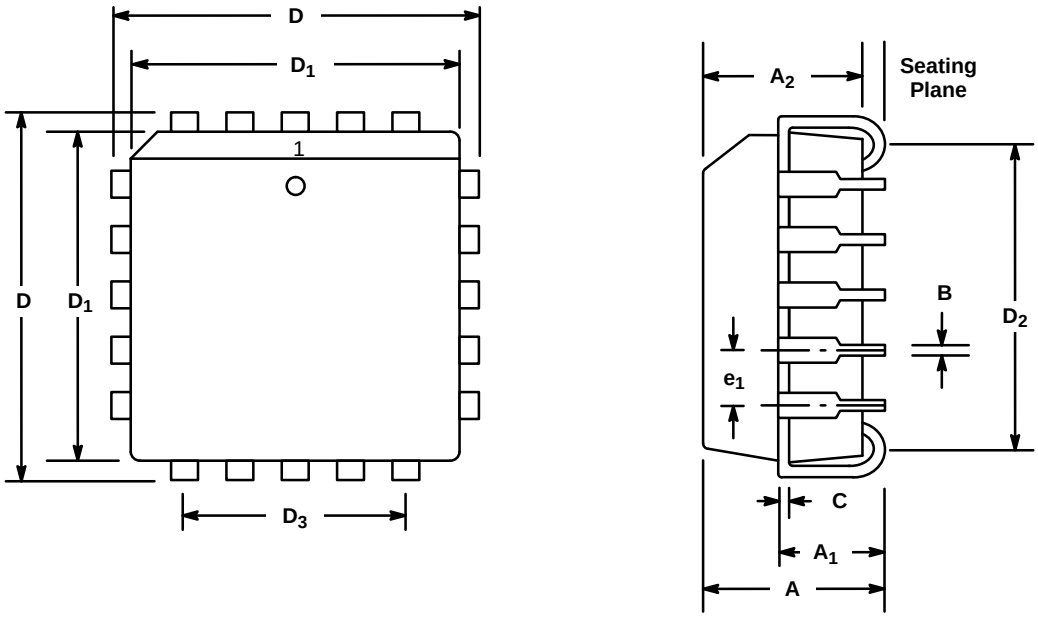
Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

20 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.642
A_1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.500	0.510	12.70	12.95
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

20 LEAD PLASTIC LEADED CHIP CARRIER (PLCC) P20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A_1	0.100	0.110	2.54	2.79
A_2	0.148	0.156	3.76	3.96
B	0.013	0.021	0.330	0.533
C	0.008	0.012	0.203	0.305
D	0.385	0.395	9.78	10.03
D_1 (1)	0.350	0.354	8.89	8.99
D_2	0.290	0.330	7.37	8.38
D_3	0.200 Ref		5.08 Ref.	
e_1	0.050 BSC		1.27 BSC	

Note: (1) Dimension D_1 does not include mold protrusion. Allowed mold protrusion is 0.254 mm/0.010 in.

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