MP7690A

CMOS
Programmable Input Range 8-Bit
High Speed Analog-to-Digital Converter

FEATURES

- **Sampling Rates from 1 kHz to 20 MHz (MSPS)**
- **DNL better than 1/4 LSB from 1 kHz to 10 MHz**
- **DNL better than 1/2 LSB to 14 MHz**
- **Adjustable Input Range between GND and V_{DD}**
- **Pin Compatible Upgrade of MP7690A**
- **Monotonic; No Missing Codes**
- **Single Power Supply (4 to 6 volt)**
- **Low Power CMOS (300 mW)**
- **ESD Protection: 4000 Volts Minimum**
- **Latch-Up Free**

BENEFITS

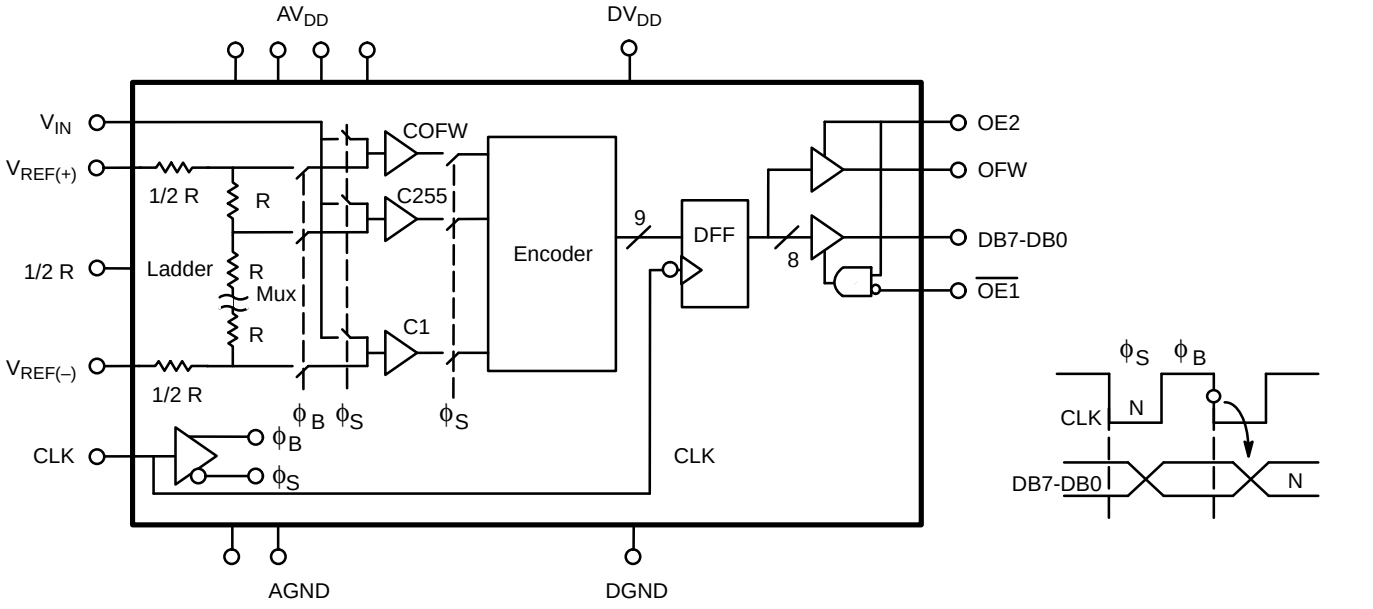
- **Reduced Board Space (Small Package) and Reduced External Parts**
- **No External Sample/Hold Needed, Reducing System Cost and Improving Ease of Design**
- **Adjustable Input Range and Scaling**

GENERAL DESCRIPTION

The MP7690A is an 8-bit monolithic CMOS single step high speed Analog-to-Digital Converter designed for precision applications in video and data acquisition requiring conversion rates to 14 MHz with differential linearity error less than 1/2 LSB and low power consumption. The input architecture of the MP7690A allows direct interface to any analog input range between AGND and DV_{DD} (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

The MP7690A includes 256 clocked comparators, encoders, 3-state output buffers, a reference ladder resistor and associated timing circuitry. An overflow bit (or flag) is provided.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

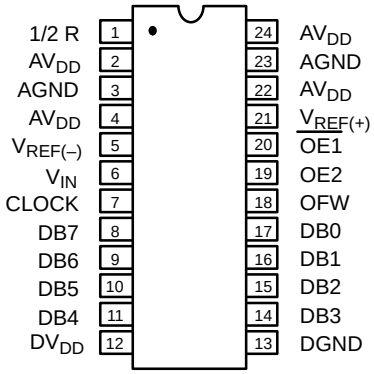


ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Ceramic Dip	–40 to +85°C	MP7690AAD	±1	±2
Ceramic Dip	–40 to +85°C	MP7690ABD	±3/4	±1 3/4
Ceramic Dip	–55 to +125°C	MP7690ASD	±1	±2
Ceramic Dip	–55 to +125°C	MP7690ATD	±3/4	±1 3/4

PIN CONFIGURATION

See Packaging Section for Package Dimensions



24 Pin CDIP (0.300")
DN24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	1/2R	Center Point of Reference Ladder
2	AV_{DD}	Analog Power Supply Voltage
3	AGND	Analog Ground
4	AV_{DD}	Analog Power Supply Voltage
5	$V_{REF(-)}$	Lower Reference Voltage Input
6	V_{IN}	Analog Input Voltage
7	CLK	Sampling Clock Input
8	DB7	Data Output Bit 7 (MSB)
9	DB6	Data Output Bit 6
10	DB5	Data Output Bit 5
11	DB4	Data Output Bit 4
12	DV_{DD}	Digital Power Supply Voltage

PIN NO.	NAME	DESCRIPTION
13	DGND	Digital Ground
14	DB3	Data Output Bit 3
15	DB2	Data Output Bit 2
16	DB1	Data Output Bit 1
17	DB0	Data Output Bit 0 (LSB)
18	OFW	Overflow Bit Output
19	OE2	Output Enable Control Pin
20	$\overline{OE1}$	Output Enable Control Pin
21	$V_{REF(+)}$	Upper Reference Voltage Input
22	AV_{DD}	Analog Power Supply Voltage
23	AGND	Analog Ground Return
24	AV_{DD}	Analog Power Supply Voltage

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 5$ V, $F_S =$ 14.0 MHz (Duty Cycle: 1/3 Sample & 2/3 Balance), $V_{REF(+)} = 4.1$, $V_{REF(–)} = GND$, $T_A = 25°C$

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		8			8		Bits	
Sampling Rate	FS	0.001		14	0.001	14	MHz	For Specified Accuracy
ACCURACY (A, S Grades)[1]								
Differential Non-Linearity	DNL			±3/4		±1	LSB	
Integral Non-Linearity (Relative Accuracy)	INL			±1 1/2		±2	LSB	Best Fit Line (Max INL – Min INL) / 2
Zero Scale Error	EZS		2				LSB	
Full Scale Error	EFS		2				LSB	
ACCURACY (B, T Grades)[1]								
Differential Non-Linearity	DNL			±1/2		±3/4	LSB	
Integral Non-Linearity	INL			±1		±1 3/4	LSB	Best Fit Line
Zero Scale Error	EZS		2				LSB	
Full Scale Error	EFS		2				LSB	
DYNAMIC ACCURACY								Histogram Test
Differential Non-Linearity	DNL		±0.30				LSB	F_{IN} = 1 MHz
	DNL		±0.65				LSB	F_{IN} = 5 MHz
REFERENCE VOLTAGES								
Positive Ref. Voltage[2]	$V_{REF(+)}$			V_{DD}		V_{DD}	V	
Negative Ref. Voltage	$V_{REF(–)}$	GND			GND		V	
Ladder Resistance	R_L	170	225	300	130	330	Ω	
Ladder Temp. Coefficient[3]	R_{TCO}					3000	ppm/°C	
ANALOG INPUT								
Input Voltage Range	V_{IN}	$V_{REF(–)}$		$V_{REF(+)}$	$V_{REF(–)}$	$V_{REF(+)}$	V p-p	
Input Impedance	Z_{IN}		10				MΩ	
Input Capacitance Sample[4]	C_{INA}		50				pF	
Aperture Delay	t_{AP}		15				ns	
Aperture Uncertainty (Jitter)	t_{AJ}		45				ps	
Clock Kickback Pulse			20				pAs	V_{REF} = 4 V
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	2.0			2.0		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Leakage Currents[5]								V_{IN}=GND to V_{DD}
CLK	I_{IN}	–10		10	–10	10	µA	
$\overline{OE2}$ (Internal Res to V_{DD})[6]		–50		5	–50	5	µA	
$\overline{OE1}$ (Internal Res to GND)[7]		–5		50	–5	50	µA	

ELECTRICAL CHARACTERISTICS TABLE CONT'D

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS								C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	V_{DD}-0.5			V_{DD}-0.5		V	I_{LOAD} = –4.0 mA
Logical "0" Voltage	V_{OL}			0.4		0.4	V	I_{LOAD} = 4.0 mA
Tristate Leakage	I_{OZ}			±10		±20	µA	V_{OUT}=GND to V_{DD}
Data Valid Delay[3]	t_{DL}		23	33	23	35	ns	
Data Enable Delay[3]	t_{DEN}			20		25	ns	
Data Tristate Delay[3]	t_{DHZ}			20		25	ns	
POWER SUPPLIES[9]								
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4	5	6	4	6	V	
Current (AV_{DD} + DV_{DD})	I_{DD}			80		85	mA	
AC PARAMETERS[3]								RMS/RMS Measures
Signal Noise Ratio[10]	SNR		47				dB	FS = 3X NTSC
	SNR		46				dB	FS = 4X NTSC
Differential Gain Error	dG		2				%	FS = 3X NTSC
Differential Phase Error	dPh		1				Degree	

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (*Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 4.*). Accuracy is a function of the sampling rate (F_S).

2 For best results it is recommended that the reference voltage be limited to (V_{DD} –0.5 V) maximum.

3 Guaranteed. Not tested.

4 See V_{IN} input equivalent circuit (*Figure 5.*). Switched capacitor analog input requires driver with low output resistance.

5 All inputs have diodes to V_{DD} and GND. Input $\overline{OE1}$ has an internal pull down. Input OE2 has an internal pull up. Input DC currents will not exceed specified limits for any input voltage between GND and V_{DD}.

6 Internal resistor to V_{DD} biases unconnected input to active high logical level.

7 Internal resistor to GND biases unconnected input to active low logical level.

8 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.

9 DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package and to the analog supply loop.

10 SNR: Ratio of RMS signal to RMS noise up to 1/2 F_S in dB.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... +7 V
$V_{REF(+)}$ & $V_{REF(–)}$ ..... GND –0.5 to V_{DD} +0.5 V
V_{IN} ..... GND –0.5 to V_{DD} +0.5 V
All Digital Inputs ..... GND –0.5 to V_{DD} +0.5 V
All Digital Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP 1100mW
Derates above 75°C ..... 15mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

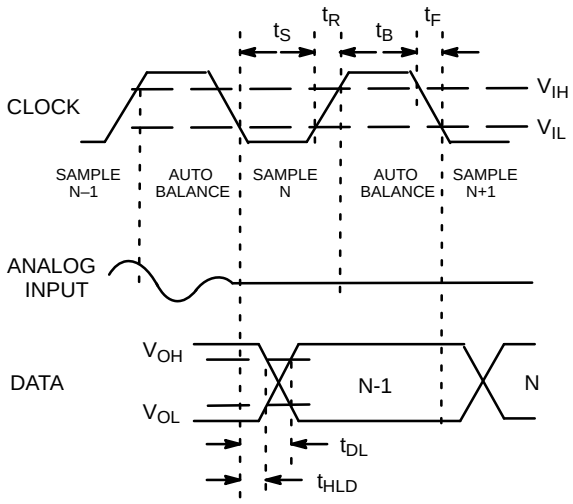


Figure 1. MP7690A Timing Diagram

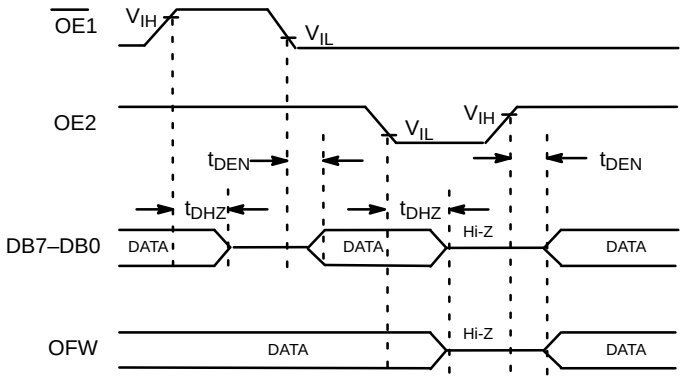
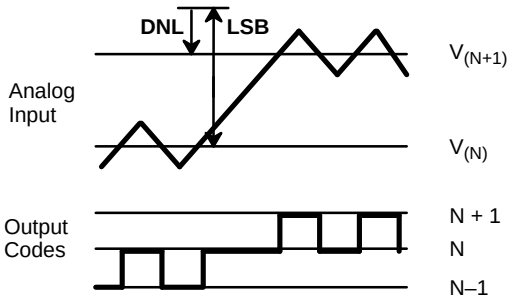


Figure 2. Output Enable/Disable Timing Diagram



(N) Code Width = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{REF(+)} - V_{REF(-)}$] / 256

$DNL_{(N)} = [\ V_{(N+1)} - V_{(N)}\ ] - LSB$

Figure 3. DNL Measurement

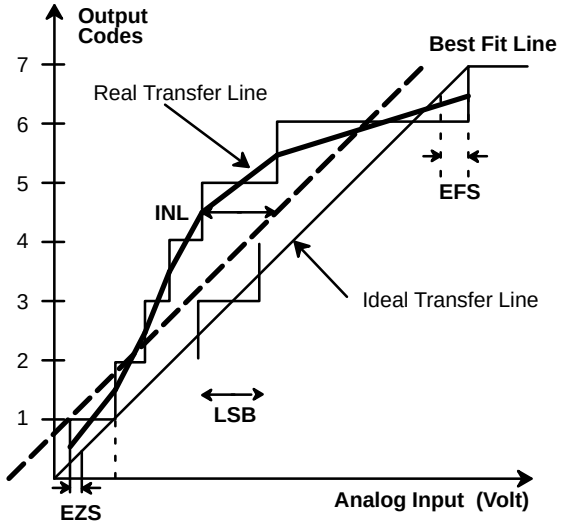


Figure 4. INL Error Calculation

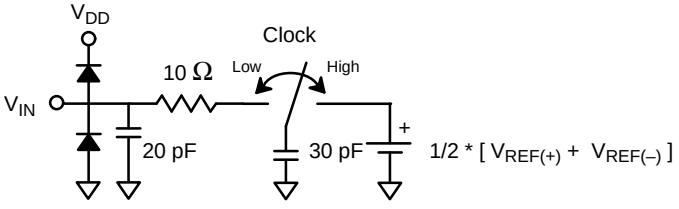


Figure 5. Analog Input Equivalent Circuit

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP7690A converts analog voltages into 256 digital codes by encoding the outputs of 255 comparators. A 256th comparator is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 1.5 clock periods. Data is transferred from the comparator latches to the output registers each clock period and at the same time the input is sampled.

The clock signal generates the two internal phases, ϕ_B (CLK high = balance) and ϕ_S (CLK low = sample). ϕ_B connects the comparators to the reference tap points. ϕ_S connects the comparators to the analog input voltage.

The reference resistance ladder is a series of 257 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 256 * R$ $\quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 256 * LSB$

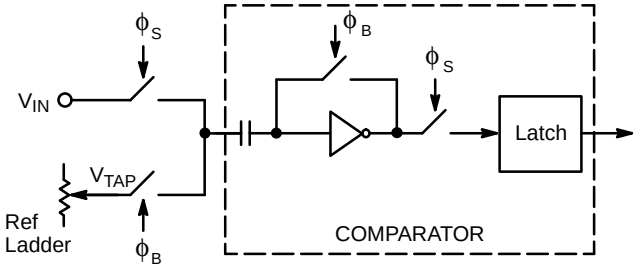


Figure 6. MP7690A Comparator

The MP7690A comparators use the balance phase (ϕ_B) to charge one plate of the capacitors to the reference ladder tap point (V_{TAP}) and the other to the inverter/comparator trigger point. During the sample phase (ϕ_S) one plate of the capacitors switches to V_{IN}. The change in voltage ($V_{IN} - V_{TAP}$) transfers across the capacitors and forces the inverters into one of the two possible logic states. Latches (connected to the comparators during ϕ_S) restore and propagate the digital level to the decode logic.

The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The aperture delay may vary from one cycle to the next. Internal thermal noise, power supply noise and slow input clock edges are major contributors to this variation. The aperture jitter (t_{AJ}) is the variation of the aperture delay distribution.

This uncertainty shows as digital code errors if the input slew rate multiplied by t_{AJ} is of the same order of magnitude as the LSB. That is, if $(dv/dt) * t_{AJ} \approx V_{REF}/256$ then one LSB of error results.

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 7.*

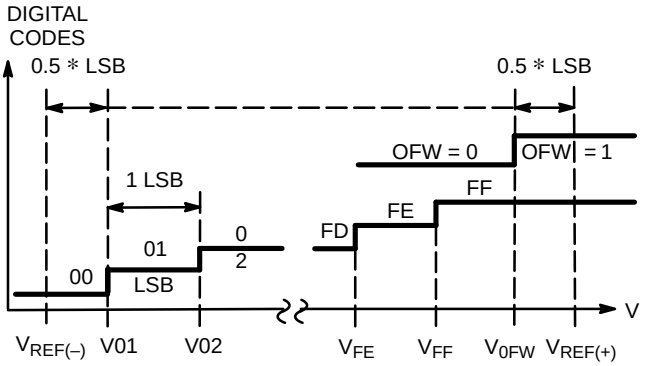


Figure 7. Ideal A/D Transfer Function

The overflow transition (V_{0FW}) takes place at:

$V_{IN} = V_{0FW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V_{01} = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{FF} = V_{REF(-)} - 1.5 * LSB$

$LSB = V_{REF} / 256 = (V_{FF} - V_{01}) / 254$

Note that the overflow bit has no impact on the data bits.

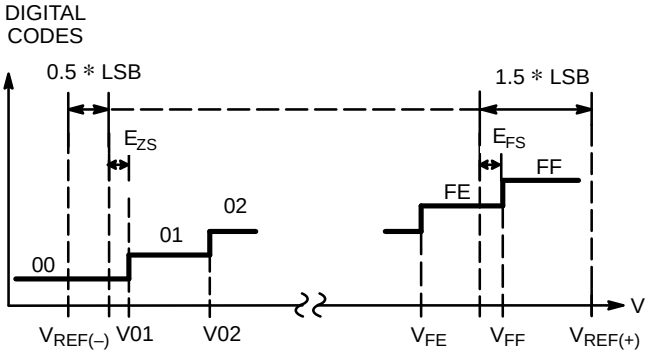


Figure 8. Real A/D Transfer Curve

In a "real" converter, the code-to-code transitions are not always exactly every $V_{REF}/256$ volts.

A positive DNL (Differential Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSB's.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated values. A specification of Max DNL = $\pm$ 0.5 LSB means that all codes are within 0.5 and 1.5 LSB. If V_{REF} = 4.096 V then 1 LSB = 16mV and every code width is between 8 and 24 mV.

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (EZS, EFS) are:

DNL (01) = V02 – V01 – LSB

: : :

DNL (FE) = $V_{FF} – V_{FE}$ – LSB

EFS (full scale error) = $V_{FF} – [V_{REF(+)} – 1.5 * LSB]$

EZS (zero scale error) = $V01 – [V_{REF(–)} + 0.5 * LSB]$

Figure 8. shows the zero scale and full scale error terms.

Systems that adjust the V_{REF} voltages to correct for EFS and EZS only increase the accuracy at the two extreme points. In the MP7690A, such adjustments have little impact at frequencies lower than 10 MHz and generally are not required. Refer to the characterization data for temperature and frequency dependence.

Figure 4. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from an ideal one.

INL is specified in terms of best fit line. Best fit line makes the INL+ and INL– errors equal by using the algebraic sum divided by 2. For example, an INL error of –1 to +2 LSB's relative to the Ideal Line would be ±1.5 LSB's relative to the Best Fit Line.

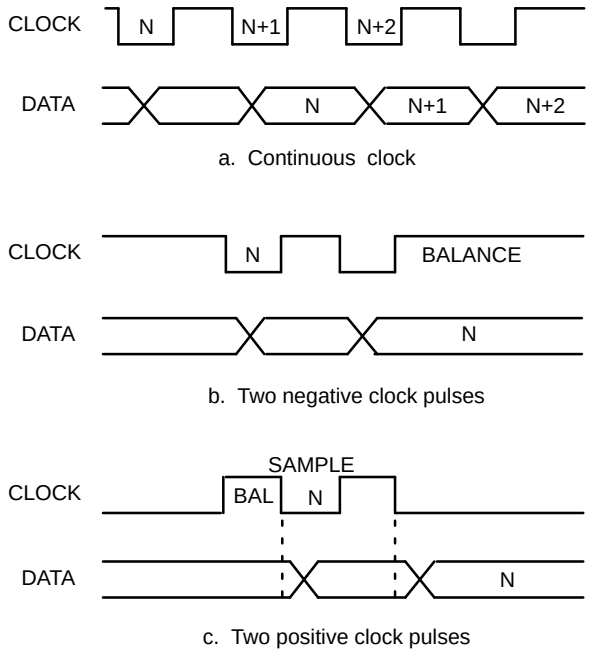


Figure 9. Relationship of Data to Clock

Clock and Conversion Timing

A system will clock the MP7690A (*Figure 9b.)* continuously or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 9b.* keeps the MP7690A comparators in balance and ready to sample the analog input. This mode draws the most current from V_{DD}. The timing of *Figure 9c.* leaves the comparator inputs floating (and AC coupled to the V_{IN} input) and a balance phase is needed before a valid sampling phase. In this mode, I_{DD} varies because of the floating comparator inputs.

Analog Input

The MP7690A has very flexible input range characteristics. The user may set $V_{REF(+)}$ and $V_{REF(–)}$ to two fixed voltages and then vary the input DC and AC levels to match the V_{REF} range. Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP7690A's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input.

Reference Voltages

If the input bandwidth is limited to the Nyquist region ($F_{IN} < F_S/2$) then the two reference voltages can be set at any two values between the supplies. V_{REF} (their difference) can be reduced down to 1.5 volts with minor change in accuracy. If the input bandwidth exceeds $F_S/2$, then it is recommended that VREF be lower than $V_{DD}/2$.

If V_{REF} is reduced below 1.5 V, accuracy will be degraded due to the decreased signal-to-noise ratio.

The input/output relationship is a function of V_{REF}:

$$A_{IN} = V_{IN} – V_{REF(–)}$$
$$V_{REF} = V_{REF(+)} – V_{REF(–)}$$
$$DATA = 255 * (A_{IN}/V_{REF}) \text{ (Full Scale)}$$

a) **Gain adjustment.** A system can increase total gain by reducing V_{REF}.

b) **Increasing dynamic range**. A system can increase dynamic range by using DACs to control V_{REF} and by "focusing" on input ranges of interest. In digitizing "static" information (an image in a scanner) a first digitization would point to the input range in which most of the output codes fall. The system can then adjust the DACs to generate $VR_{EF(+)}$ and $V_{REF(–)}$ to include just the range of interest for the second and final pass.

c) **Subranging; increasing resolution**. Where practical, multiple passes at different V_{REF} ranges can increase resolution without changing hardware. A system needs to make four passes to increase the resolution to 10 bits. The merg-

ing of the data from the four passes can create DNL errors at the borders of the ranges. One solution is to “overlap” the ranges and to use software methods to properly merge the ranges.

Digital Interfaces

The logic encodes the 255 input bits into a binary code and latches the data in a D-type flip-flop for output. The inputs $\overline{OE1}$ and OE2 control the output buffers in an asynchronous mode.

The functional equivalent of the MP7690A (*Figure 10.*) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An A/D which tracks and converts V_{IN} with no delay.
3) A DFF (D type flip-flop) with specified hold (t_{HLD}) and de lay (t_{DL}) times. t_{AP}, t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

$\overline{OE1}$	OE2	OFW	DB7–DB0
X	0	High Z	High Z
1	1	Valid	High Z
0	1	Valid	Valid

Table 1. Output Enable Logic

If an external DFF is to follow the MP7690A, it is recommended that the system latches the data at the negative going edge of the clock. This will work at any frequency. If the system must latch with the positive going edge then care must be taken to avoid the overlay of the clock edge with the changing outputs.

If a latch follows the ADC, the positive half of the clock used as an enable signal for the latch guarantees stable output at the end of the enable pulse.

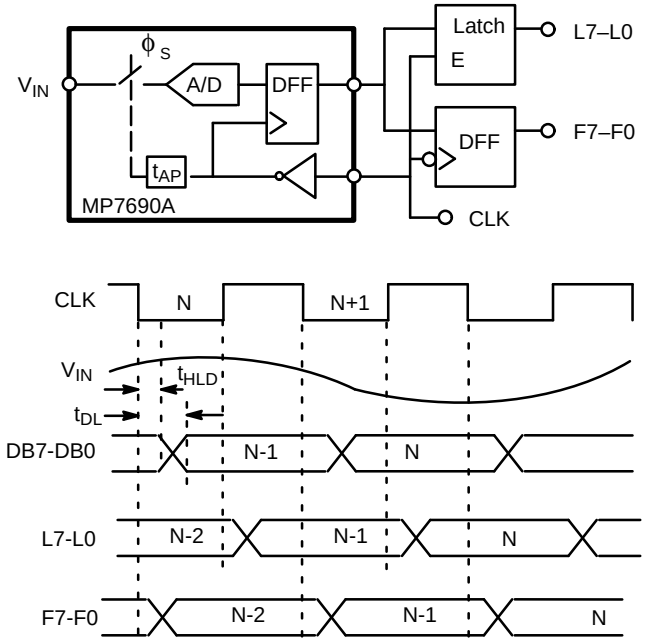


Figure 10. MP7690A Functional Equivalent Circuit and Interface Timing

APPLICATION NOTES

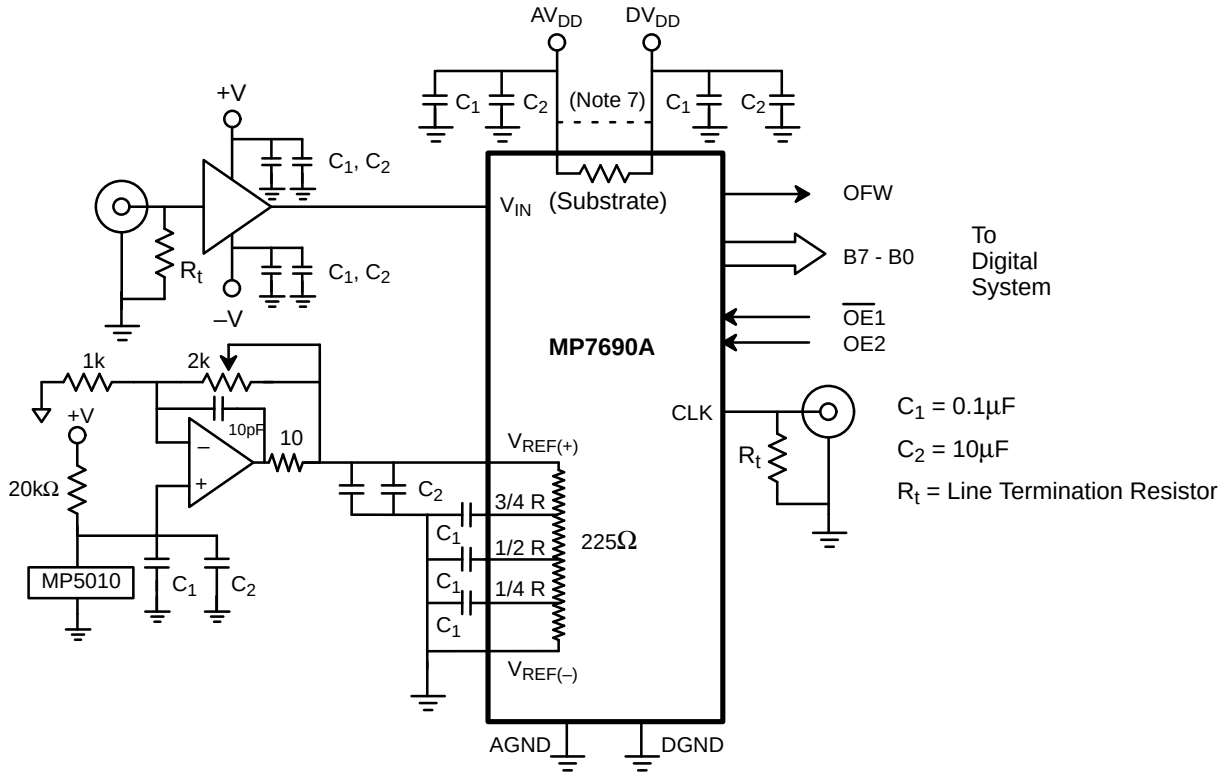
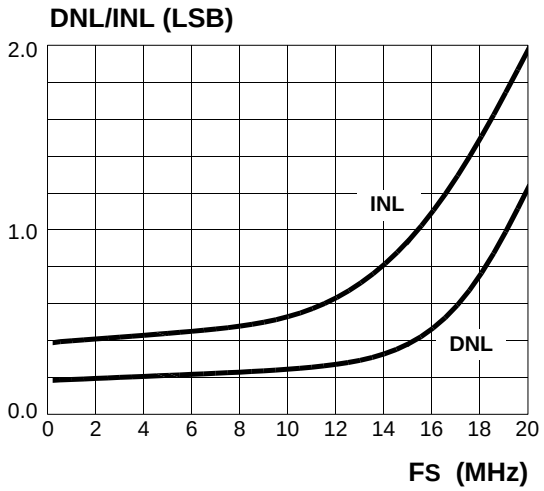


Figure 11. Typical Circuit Connections

The following information will be useful in maximizing the performance of the MP7690A.

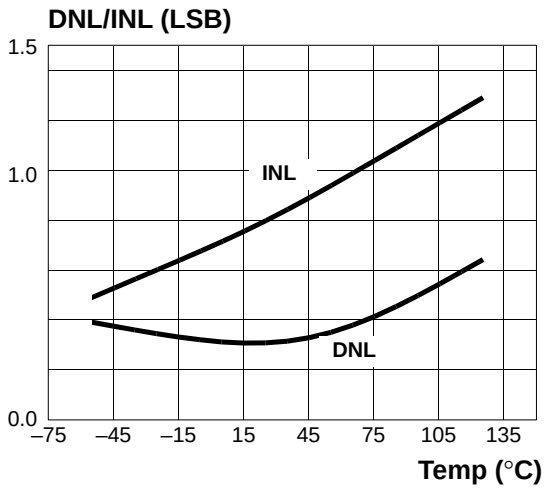
1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP7684A inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP7690A. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths.
7. DV_{DD} should not be shared with other digital circuitry to avoid conversion errors caused by digital supply transients. DV_{DD} should be connected to AV_{DD} next to the MP7690A.
8. DV_{DD} and AV_{DD} are connected inside the MP7690A through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used.

CHARACTERIZATION CHARTS (Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, F_S = 14 MHz (50% Duty Cycle), $V_{REF(+)}$ = 4.1 V, $V_{REF(–)}$ = GND, T_A = 25°C



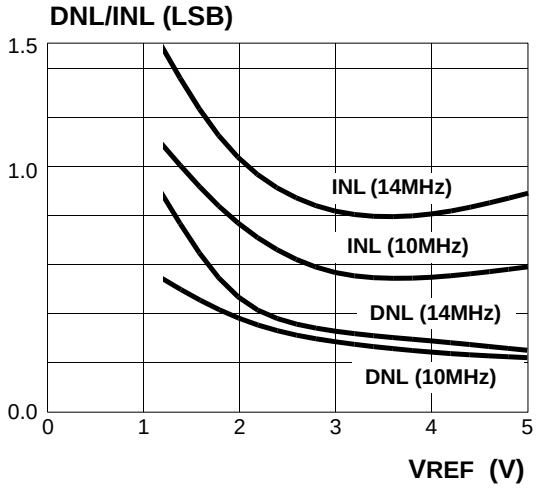
Accuracy (DNL/INL)
vs. Sampling Rate (FS)

Graph 1.



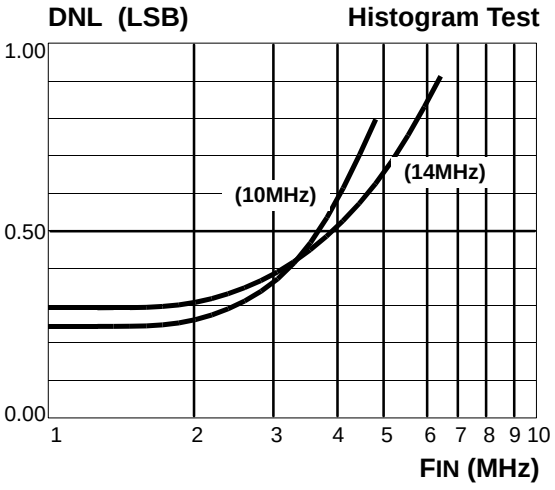
Accuracy (DNL/INL)
vs. Ambient Temperature (T)

Graph 2.



Accuracy (DNL/INL)
vs. Reference Voltage (VREF)
vs. Sampling Rate (FS = 10, 14 MHz)
(VIN p-p = VREF)

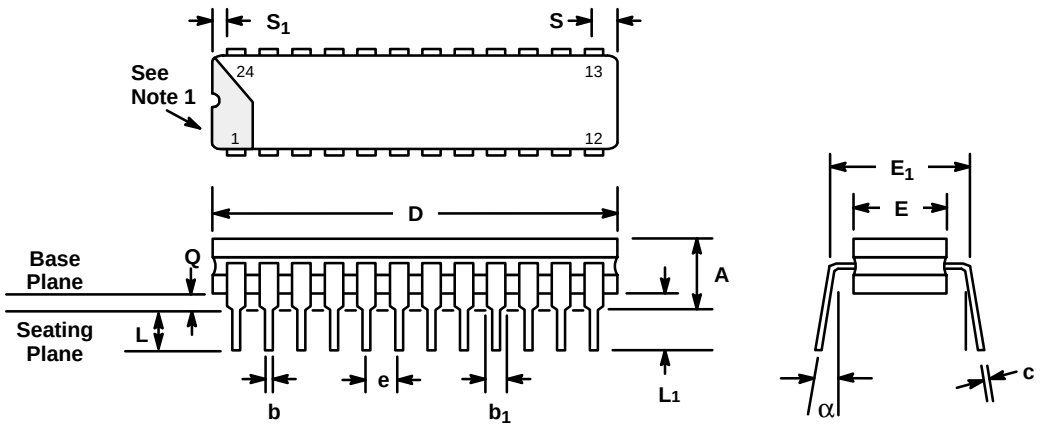
Graph 3.



Dynamic (DNL/INL)
vs. Input Sinewave (FIN)
vs. Sampling Rate (FS = 10, 14 MHz)

Graph 4.

24 LEAD CERAMIC DUAL-IN-LINE
(300 MIL CDIP)
DN24



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	1.280	—	32.51	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.381	1.52	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

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