

FEATURES

- Sampling Rates from 1 kHz to 15 MHz (MSPS)
- DNL better than 1/2 LSB from 1 kHz to 10 MHz
- Interface to any Input Range between GND and V_{DD}
- Monotonic; No Missing Codes
- Single Power Supply (4 to 6 volt)
- Low Power CMOS (300 mW)
- Latch-Up Free
- 2000 Volt ESD Protection

BENEFITS

- Reduced Board Space (small package)
- Excellent Accuracy Without High System Power
- Reduced External Parts, No Sample/Hold Needed
- Designer Can Adapt Input Range and Scaling
- Use MP7690A for New Designs

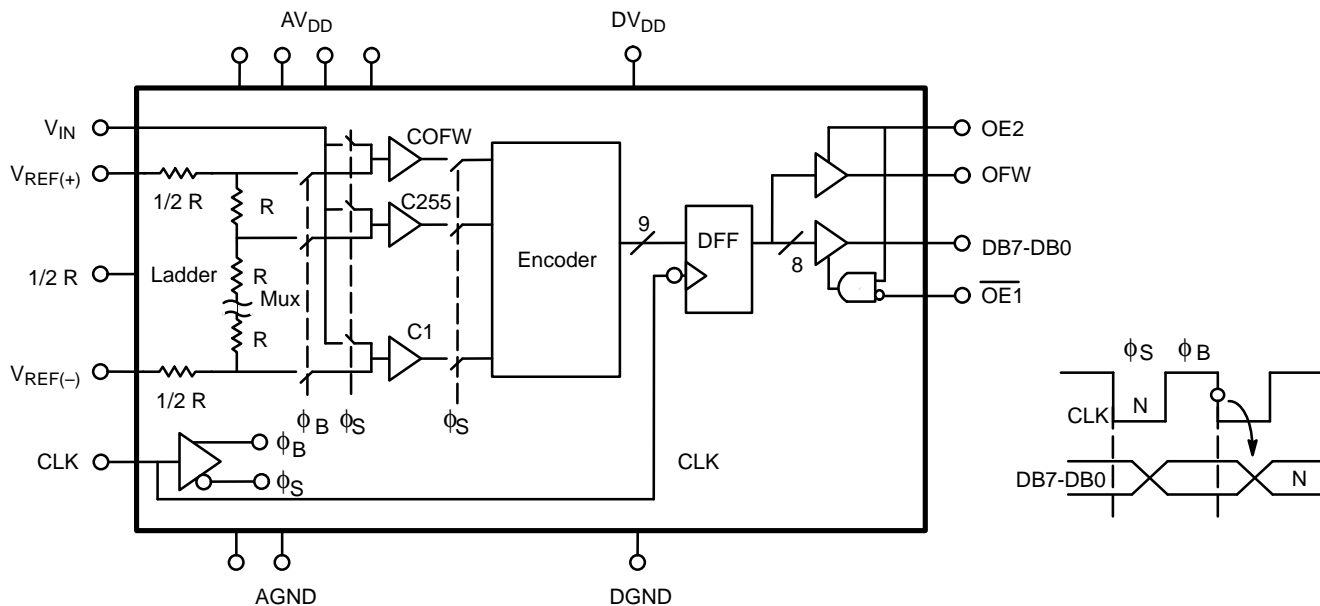
GENERAL DESCRIPTION

The MP7690 is an 8-bit monolithic CMOS single step high speed Analog-to-Digital Converter designed for precision applications in video and data acquisition requiring conversion rates to 10 MHz with differential linearity error less than 1/2 LSB and low power consumption. The input architecture of the MP7690 allows direct interface to any analog input range

between AGND and AV_{DD} (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

The MP7690 includes 256 clocked comparators, encoders, 3-state output buffers, a reference ladder resistor and associated timing circuitry. An overflow bit (or flag) is provided.

SIMPLIFIED BLOCK AND TIMING DIAGRAM

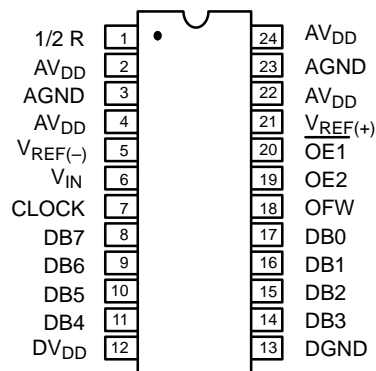


ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Ceramic Dip	-40 to +85°C	MP7690JD	±1 1/2	2
Ceramic Dip	-40 to +85°C	MP7690KD	±1	1 1/2
Ceramic Dip	-55 to +125°C	MP7690SD	±1 1/2	2
Ceramic Dip	-55 to +125°C	MP7690TD	±1	1 1/2

PIN CONFIGURATION

See Packaging Section for
Package Dimensions



24 Pin CDIP (0.300")
DN24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	1/2R	Center of Reference Resistance Ladder
2	AV _{DD}	Analog Power Supply Voltage
3	AGND	Analog Ground Return
4	AV _{DD}	Analog Power Supply Voltage
5	V _{REF(-)}	Lower Reference Voltage Input
6	V _{IN}	Analog Input Voltage
7	CLK	Sampling Clock Input
8	DB7	Data Bit 7 (MSB)
9	DB6	Data Output Bit 6
10	DB5	Data Output Bit 5
11	DB4	Data Output Bit 4
12	DV _{DD}	Digital Power Supply Voltage

PIN NO.	NAME	DESCRIPTION
13	DGND	Digital Ground Return
14	DB3	Data Output Bit 3
15	DB2	Data Output Bit 2
16	DB1	Data Output Bit 1
17	DB0	Data Output Bit 0 (LSB)
18	OFW	Overflow flag
19	OE2	Output Enable Control Pin
20	OE1	Output Enable Control Pin
21	V _{REF(+)}	Upper Reference Voltage Input
22	AV _{DD}	Analog Power Supply Voltage
23	AGND	Analog Ground Return
24	AV _{DD}	Analog Power Supply Voltage

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 5\text{ V}$, $F_S = 10.0\text{ MHz}$ (Duty Cycle: 1/3 Sample & 2/3 Balance),
 $V_{REF(+)} = 4.1$, $V_{REF(-)} = \text{GND}$, $T_A = 25^\circ\text{C}$

Parameter	Symbol	25°C			Tmin to Tmax		Units	Test Conditions/Comments
Min		Typ	Max	Min	Max			
KEY FEATURES								
Resolution		8			8	Bits		
Sampling Rate	F _S	0.001	10	0.001	10	MHz	For Specified Accuracy	
ACCURACY (J, S Grades) ¹								
Differential Non-Linearity	DNL		±3/4		±1 1/2	LSB	Best Fit Line (Max INL – Min INL) / 2	
Integral Non-Linearity	INL		±1 1/2		±2	LSB		
(Relative Accuracy)								
Zero Scale Error	EZS	2				LSB		
Full Scale Error	EFS	2				LSB		
ACCURACY (K, T Grades) ¹								
Differential Non-Linearity	DNL		±1/2		±1	LSB	Best Fit Line	
Integral Non-Linearity	INL		±1		±1 1/2	LSB		
Zero Scale Error	EZS	2				LSB		
Full Scale Error	EFS	2				LSB		
REFERENCE VOLTAGES								
Positive Ref. Voltage ²	V _{REF(+)}		V _{DD}		V _{DD}	V		
Negative Ref. Voltage	V _{REF(-)}	GND		GND		V		
Ladder Resistance	R _L	120	400	90	430	Ω		
Ladder Temp. Coefficient ³	R _{TCO}				3000	ppm/°C		
ANALOG INPUT								
Input Voltage Range	V _{IN}	V _{REF(-)}	V _{REF(+)}	V _{REF(-)}	V _{REF(+)}	V p-p		
Input Impedance	Z _{IN}		10			MΩ		
Input Capacitance Sample ⁴	C _{INA}		50			pF		
Aperture Delay	t _{AP}		25			ns		
Aperture Uncertainty (Jitter)	t _{AJ}		60			ps		
DIGITAL INPUTS								
Logical “1” Voltage	V _{IH}	3.5		3.5		V	V _{IN} =GND to V _{DD}	
Logical “0” Voltage	V _{IL}		1.5		1.5	V		
Leakage Currents ⁵								
CLK	I _{IN}	–100	100	–150	150	μA		
OE2 (Internal Res to V _{DD}) ⁶		–60	1	–100	1	μA		
OE1 (Internal Res to GND) ⁷		–1	50	–1	75	μA		
DIGITAL OUTPUTS								
Logical “1” Voltage	V _{OH}	4.3		4.3		V	C _{OUT} =15 pF I _{LOAD} = –1.0 mA I _{LOAD} = 2.0 mA V _{OUT} =GND to V _{DD}	
Logical “0” Voltage	V _{OL}		0.6		0.6	V		
Tristate Leakage	I _{OZ}		±0.6	±1	±0.8	±1.5		μA
Data Valid Delay ³	t _{DL}		50					ns
Data Enable Delay ³	t _{DEN}		40					ns
Data Tristate Delay ³	t _{DHZ}		40					ns

ELECTRICAL CHARACTERISTICS TABLE CONT'D

Parameter	Symbol	25°C			Tmin to Tmax		Units	Test Conditions/Comments
		Min	Typ	Max	Min	Max		
POWER SUPPLIES ⁹								
Operating Voltage (AV _{DD} , DV _{DD})	V _{DD}	4	5	6			V	
Current (AV _{DD} + DV _{DD})	I _{DD}		52	75		90	mA	

NOTES

- ¹ Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (*Figure 3*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 4*). Accuracy is a function of the sampling rate (F_S).
- ² For best results it is recommended that the reference voltage be limited to (V_{DD} – 0.5 V) maximum.
- ³ Guaranteed. Not tested.
- ⁴ See V_{IN} input equivalent circuit (*Figure 5*). Switched capacitor analog input requires driver with low output resistance.
- ⁵ All inputs have diodes to V_{DD} and GND. Input OE1 has an internal pull down. Input OE2 has an internal pull up. Input DC currents will not exceed specified limits for any input voltage between GND and V_{DD}.
- ⁶ Internal resistor to V_{DD} biases unconnected input to active high logical level.
- ⁷ Internal resistor to GND biases unconnected input to active low logical level.
- ⁸ Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.
- ⁹ DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package and to the analog supply.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)^{1, 2, 3}

V _{DD} to GND +7 V	Storage Temperature –65 to +150°C
V _{REF} (+) & V _{REF} (–) GND –0.5 to V _{DD} +0.5 V	Lead Temperature (Soldering 10 seconds) +300°C
V _{IN} GND –0.5 to V _{DD} +0.5 V	Package Power Dissipation Rating to 75°C	
All Inputs GND –0.5 to V _{DD} +0.5 V	CDIP 1100mW
All Outputs GND –0.5 to V _{DD} +0.5 V	Derates above 75°C 15mW/°C

NOTES:

- ¹ Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- ² Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100μs.
- ³ V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

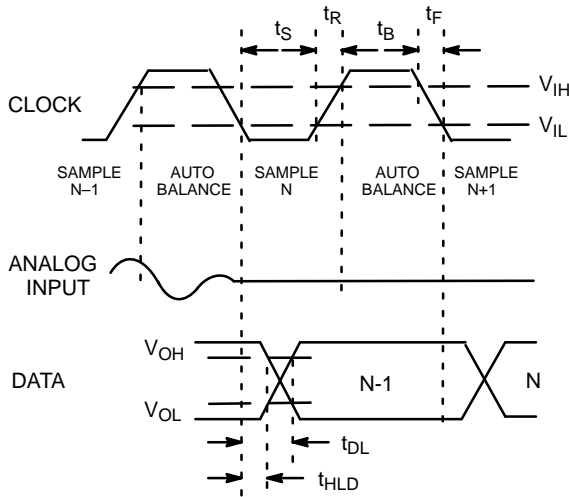


Figure 1. MP7690 Timing Diagram

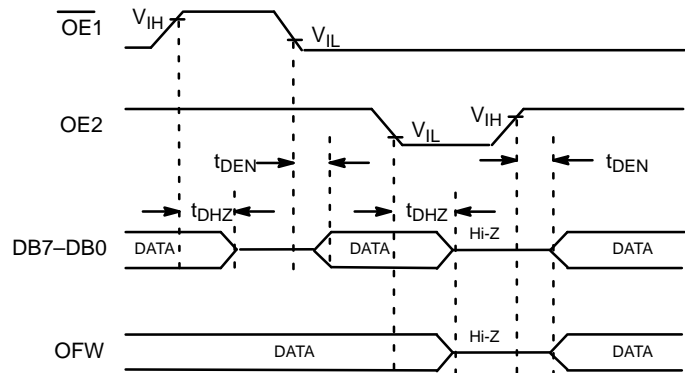


Figure 2. Output Enable/Disable Timing Diagram

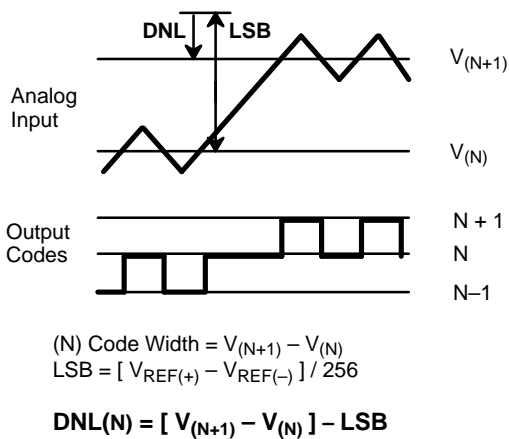


Figure 3. DNL Measurement

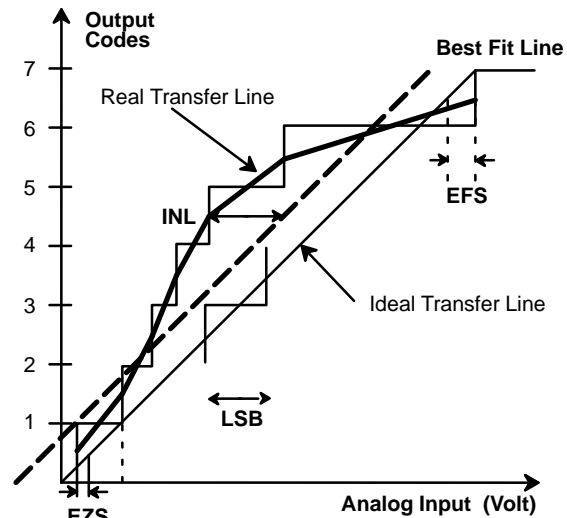


Figure 4. INL Error Calculation

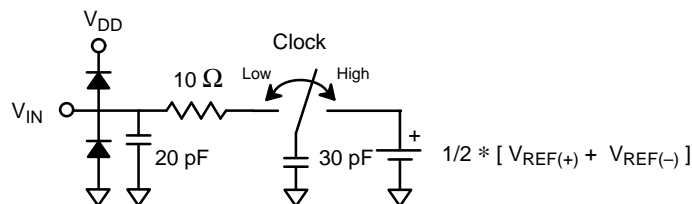


Figure 5. Analog Input Equivalent Circuit

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP7690 converts analog voltages into 256 digital codes by encoding the outputs of 255 comparators. A 256th comparator is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 1.5 clock periods. Data is transferred from the comparator latches to the output registers each clock period and at the same time the input is sampled.

The clock signal generates the two internal phases, ϕ_B (CLK high = balance) and ϕ_S (CLK low = sample). ϕ_B connects the comparators to the reference tap points. ϕ_S connects the comparators to the analog input voltage.

The reference resistance ladder is a series of 257 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$$R_{REF} = 256 * R \quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 256 * LSB$$

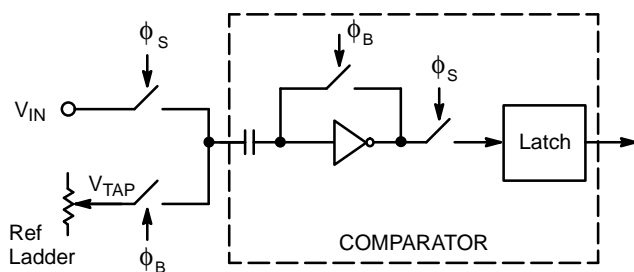


Figure 6. MP7690 Comparator

The MP7690 comparators use the balance phase (ϕ_B) to charge one plate of the capacitors to the reference ladder tap point (V_{TAP}) and the other to the inverter/comparator trigger point. During the sample phase (ϕ_S) one plate of the capacitors switches to V_{IN} . The change in voltage ($V_{IN} - V_{TAP}$) transfers across the capacitors and forces the inverters into one of the two possible logic states. Latches (connected to the comparators during ϕ_S) restores and propagates the digital level to the de-code logic.

The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The aperture delay may vary from one cycle to the next. Internal thermal noise, power supply noise and slow input clock edges are major contributors to this variation. The aperture jitter (t_{AJ}) is the variation of the aperture delay distribution.

This uncertainty shows as digital code errors if the input slew rate multiplied by t_{AJ} is in the same order of magnitude of the

LSB. That is, if $(dv/dt) * t_{AJ} \approx V_{REF}/256$, an internal error of 1 LSB results.

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in Figure 7.

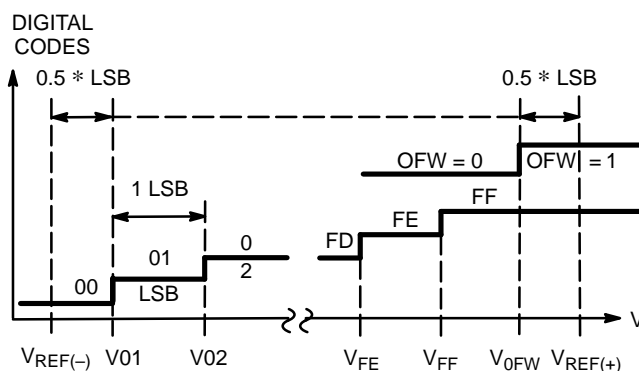


Figure 7. Ideal A/D Transfer Function

The overflow transition (V_{0FW}) takes place at:

$$V_{IN} = V_{0FW} = V_{REF(+)} - 0.5 * LSB$$

The first and the last transitions for the data bits take place at:

$$V_{IN} = V_{01} = V_{REF(-)} + 0.5 * LSB$$

$$V_{IN} = V_{FF} = V_{REF(+)} - 1.5 * LSB$$

$$LSB = (V_{REF(+)} - V_{REF(-)}) / 256 = (V_{FF} - V_{01}) / 254$$

Note that the overflow transition is a flag and has no impact on the data bits.

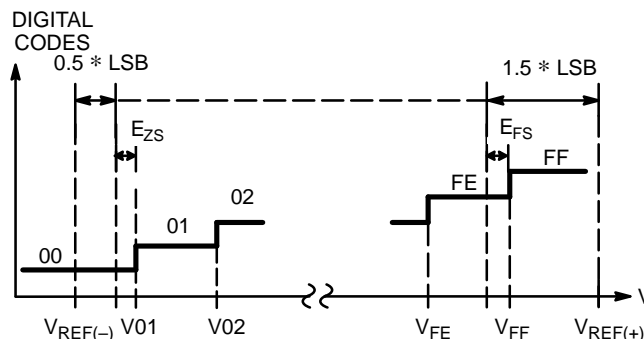


Figure 8. Real A/D Transfer Curve

In a "real" converter, the code-to-code transitions do not fall exactly every $(V_{REF(+)} - V_{REF(-)}) / 256$ volts.

A positive DNL (Differential Non-Linearity) error means that the real width of a particular code is larger than or less than 1 LSB. This error is measured in fractions of LSBs.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = ± 0.5 LSB means that all codes are within 0.5 and 1.5 LSB. If $V_{REF} = 4.096$ V then 1 LSB = 16mV and every code width is within 8 and 24 mV.

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (EFS, EFS) are:

$$DNL(01) = V_{02} - V_{01} - LSB$$

: : :

$$DNL(FE) = V_{FF} - V_{FE} - LSB$$

$$EFS(\text{full scale error}) = V_{FF} - [V_{REF(+)} - 1.5 * LSB]$$

$$EFS(\text{zero scale error}) = V_{01} - [V_{REF(-)} + 0.5 * LSB]$$

Figure 8. shows the zero scale and full scale error terms.

Systems that adjust the V_{REF} voltages to correct for EFS and EZS only increase the accuracy at the two extreme points. In the MP7690, such adjustments have little impact at frequencies lower than 10 MHz and generally are not required. Refer to the characterization data for temperature and frequency dependence.

Figure 4. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, a line is drawn parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and the negative INL errors. For example, an INL error of -1 to $+2$ LSB's relative to the Ideal Line would be ± 1.5 LSB's relative to the Best Fit Line.

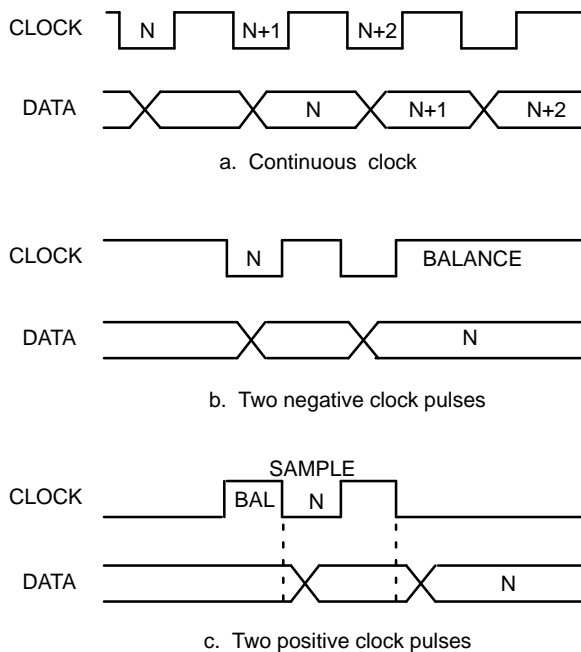


Figure 9. Relationship of Data to Clock

Clock and Conversion Timing

A system will clock the MP7690 continuously (Figure 9a.) or it will give clock pulses intermittently when a conversion is desired. The timing of Figure 9b. keeps the MP7690 comparators in balance and ready to sample the analog input. This mode draws the most current from V_{DD} . The timing of Figure 9c. leaves the comparator inputs floating (and AC coupled to the V_{IN} input) and a balance phase is needed before a valid sampling phase. In this mode, I_{DD} varies because of the floating comparator inputs.

Analog Input

The MP7690 has very flexible input range characteristics. The user may set $V_{REF(+)}$ and $V_{REF(-)}$ to two fixed voltages and then vary the input DC and AC levels to match the V_{REF} range. Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP7690's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input.

Reference Voltages

If the input bandwidth is limited to the Nyquist region ($F_{IN} < (F_S)/2$) then the two reference voltages can be set at any two values between the supplies. V_{REF} (their difference) can be reduced down to 1.5 volts with minor change in accuracy. If the input bandwidth exceeds $(F_S)/2$, then it is recommended that V_{REF} be lower than $V_{DD}/2$.

At $V_{REF} = 1.5$ V the LSB is reduced to 6mV. Further reductions show an increased error in terms of LSB (which is getting smaller) even if the error in terms of mV is about constant.

The input/output relationship as a function of V_{REF} :

$$A_{IN} = V_{IN} - V_{REF(-)}$$

$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$

$$DATA = 256 * (A_{IN}/V_{REF})$$

$$0 \leq V_{IN} \leq V_{REF} - 1 \text{ LSB}, DATA = 255 \text{ if } V_{IN} = V_{REF}$$

a) **Gain adjustment.** A system can increase total gain by reducing V_{REF} .

b) **Increasing dynamic range.** A system can increase dynamic range by using DAC's to control V_{REF} and by "focusing" on input ranges of interest. In digitizing "static" information (an image in a scanner), a first digitization would point to the input range in which most of the output codes fall. The system then would adjust the DAC's to generate $V_{REF(+)}$ and $V_{REF(-)}$ to include just the range of interest for the second and final pass.

c) **Subranging; increasing resolution.** Where practical, multiple passes at different V_{REF} ranges can increase resolution without changing hardware. A system needs to make four passes to increase the resolution to 10 bits. The merging of the data from the four passes can create DNL errors at the borders of the ranges. One solution is to "overlap" the ranges and to use software methods to properly merge the ranges.

Digital Interfaces

The logic encodes the 255 bits into a binary code and latches the data in a D-type flip-flop for output. The inputs $\overline{OE1}$ and $\overline{OE2}$ control the output buffers in an asynchronous mode.

The functional equivalent of the MP7690 (Figure 10.) is composed of:

- 1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_s).
- 2) An A/D which tracks and converts V_{IN} with no delay.
- 3) A DFF with specified hold (t_{HLD}) and delay (t_{DL}) times. t_{AP} , t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

$\overline{OE1}$	$\overline{OE2}$	DB0 – DB7	OFW
X	0	High Z	High Z
1	1	Valid	High Z
0	1	Valid	Valid

Table 1. Output Enable Logic

If an external DFF is to follow the MP7690, it is recommended that the system latches the data at the negative going edge of the clock. This will work at any frequency. If the system must latch with the positive going edge then care must be taken to avoid the overlay of the clock edge with the changing outputs.

If a latch follows the ADC, the positive half of the clock used as enable signal guarantees stable output at the end of the enable pulse.

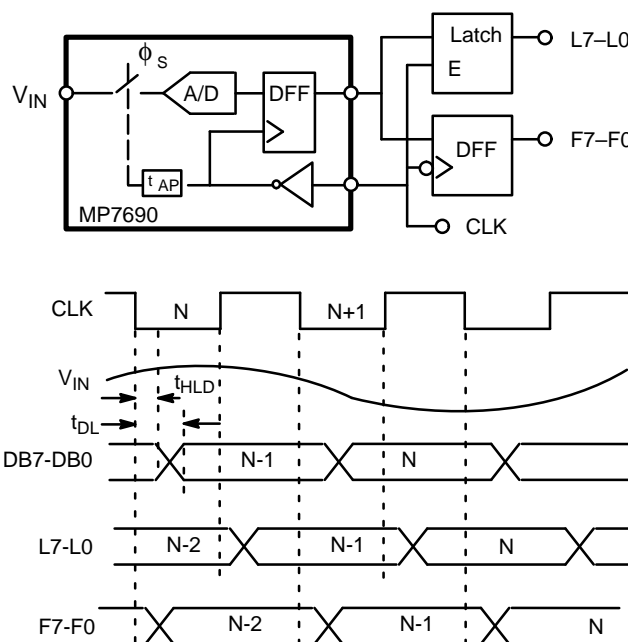


Figure 10. MP7690 Functional Equivalent Circuit and Interface Timing

APPLICATION NOTES

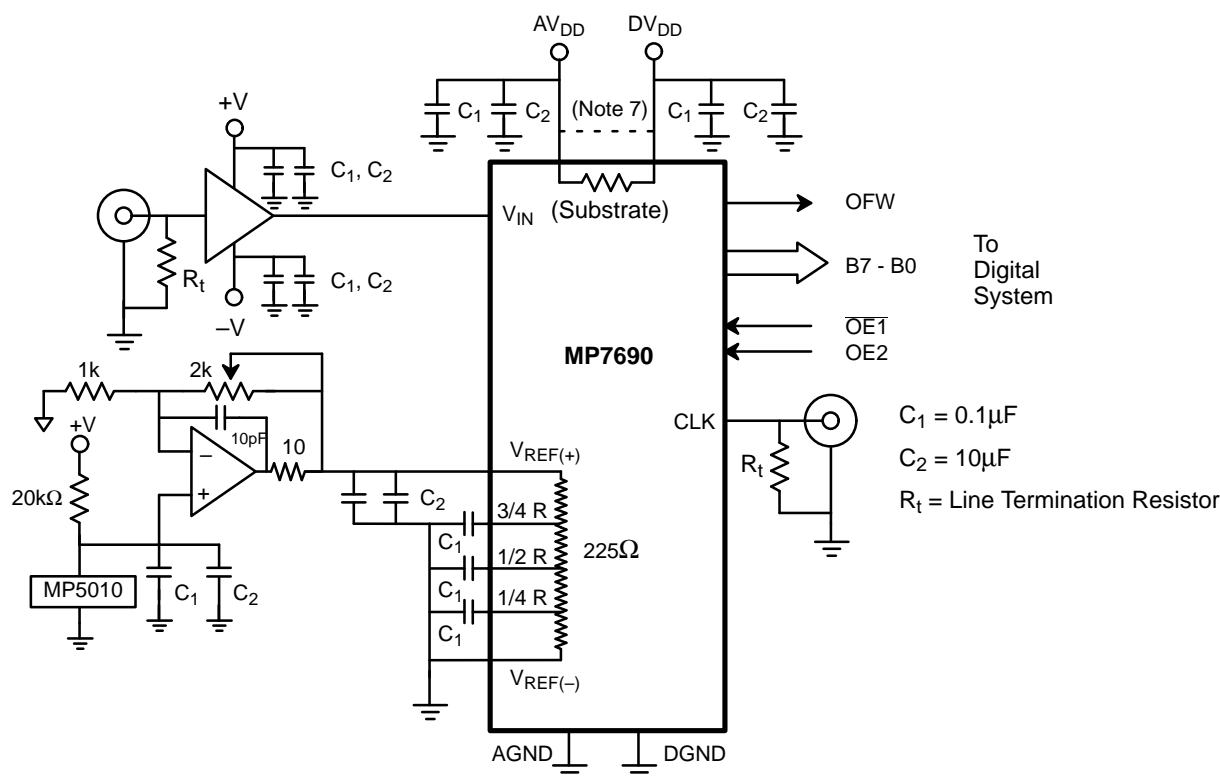
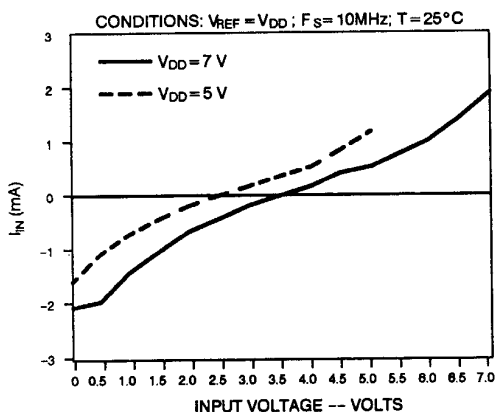


Figure 11. Typical Circuit Connections

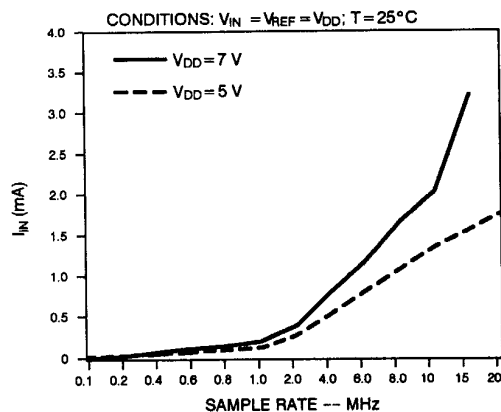
The following information will be useful in maximizing the performance of the MP7690.

1. All signals should not exceed $AV_{DD} + 0.5 V$ or $AGND - 0.5 V$ or $DV_{DD} + 0.5 V$.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or $DV_{DD} + 0.5 V$ or $AGND - 0.5 V$) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP7684A inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP7690. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths.
7. DV_{DD} should not be shared with other digital circuitry to avoid conversion errors caused by digital supply transients. DV_{DD} should be connected to AV_{DD} next to the MP7690.
8. DV_{DD} and AV_{DD} are connected inside the MP7690 through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. Each power supply and reference voltage pin should be decoupled with a ceramic ($0.1\mu F$) and a tantalum ($10\mu F$) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used.

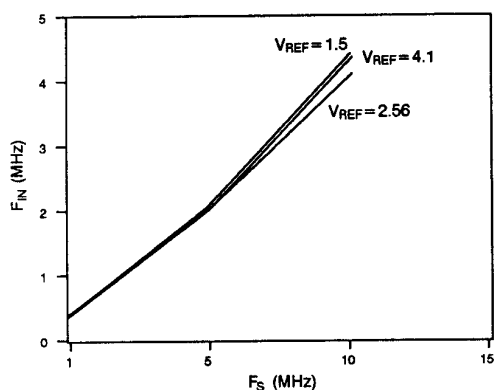
INPUT CURRENT vs. INPUT VOLTAGE



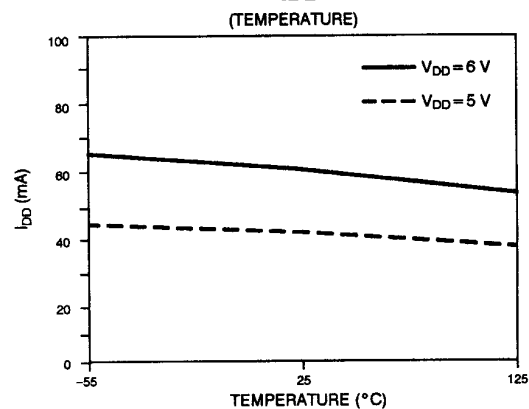
INPUT CURRENT vs. SAMPLE RATE



SMALL SIGNAL BANDWIDTH

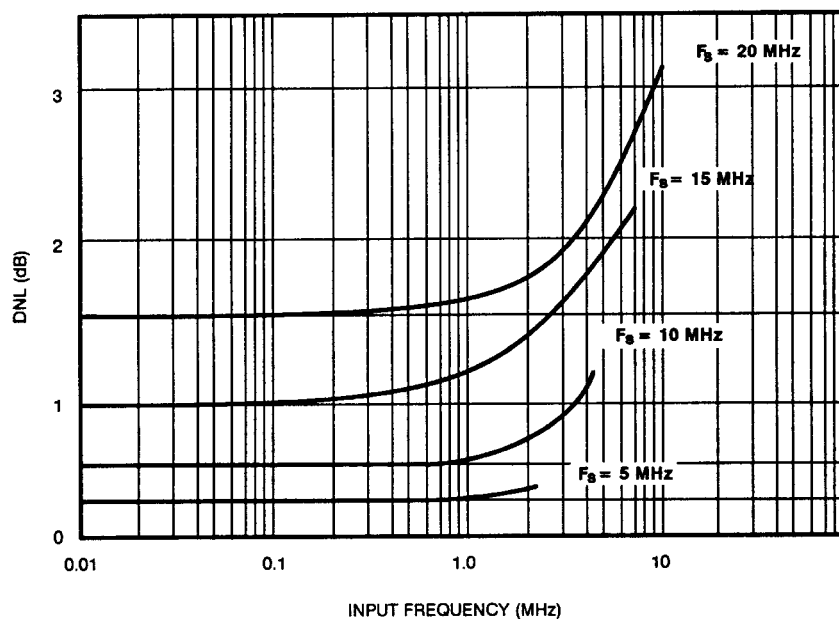


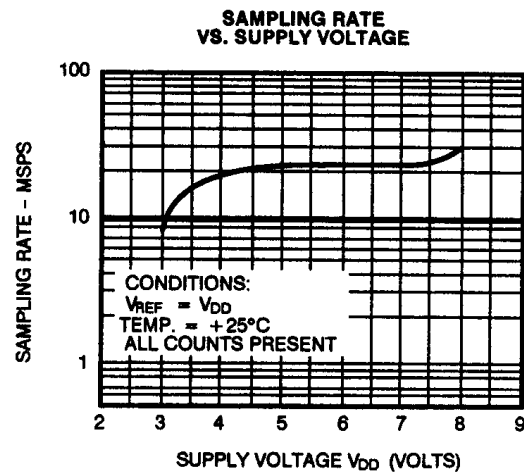
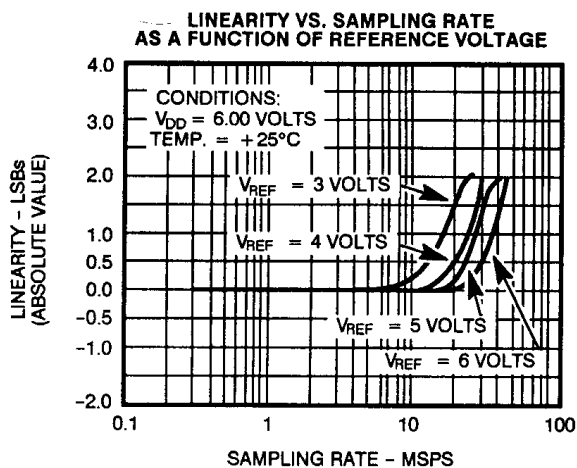
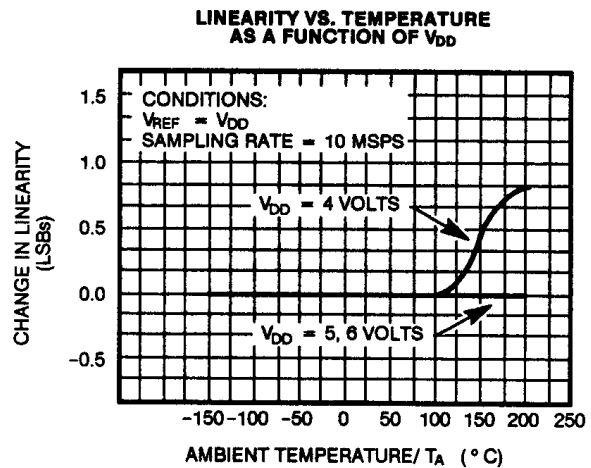
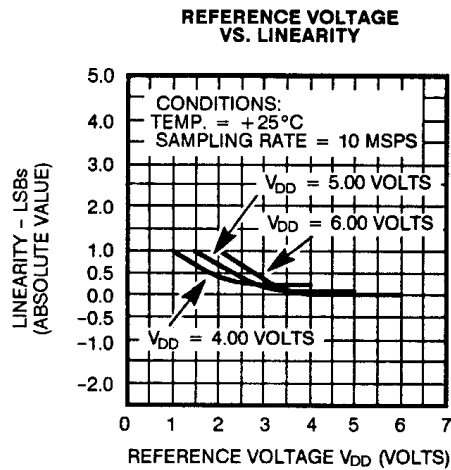
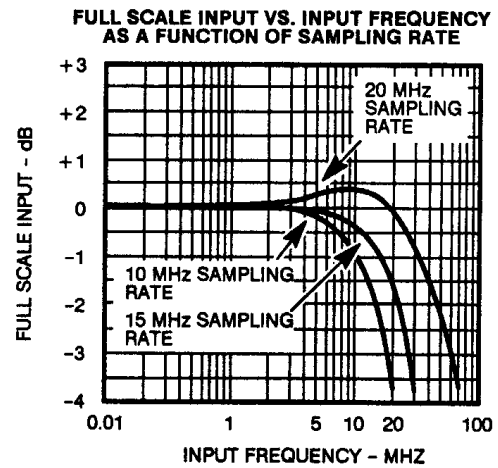
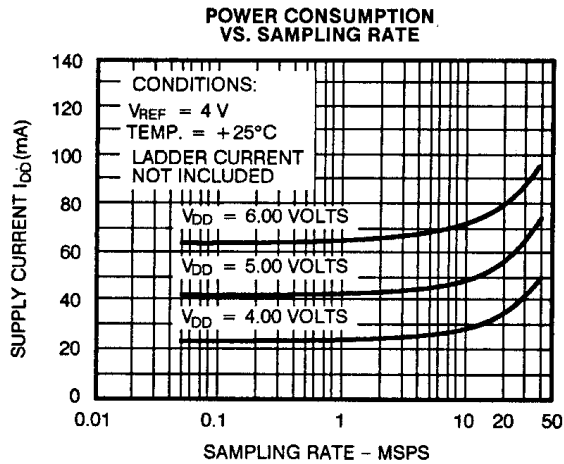
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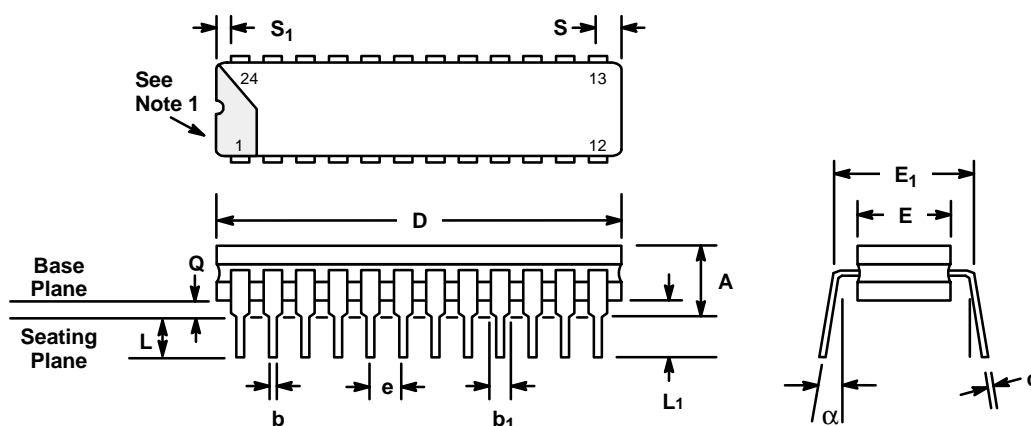
DNL vs. INPUT BANDWIDTH AS A FUNCTION OF SAMPLE RATE

(DNL IS THE LARGEST ERROR APPEARING ON THE HISTOGRAM)





24 LEAD CERAMIC DUAL-IN-LINE (300 MIL CDIP) DN24



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.356	0.584	—
b ₁	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	1.280	—	32.51	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.381	1.52	3
S	—	0.098	—	2.49	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b₁ may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

Notes

Notes

Notes

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