MP7684

CMOS
8-Bit High Speed
Analog-to-Digital Converter

FEATURES

- Sampling Rates from 0.001 to 15 MHz (MSPS)
- 1/2 LSB (K Grade) DNL to 6 MHz
- Interface to any Input Range between GND and V_{DD}
- Monotonic; No Missing Codes
- Single Power Supply (4 to 6 volt)
- Low Power CMOS (300 mW)
- 2000 Volts ESD Protection
- Latch-Up Free

BENEFITS

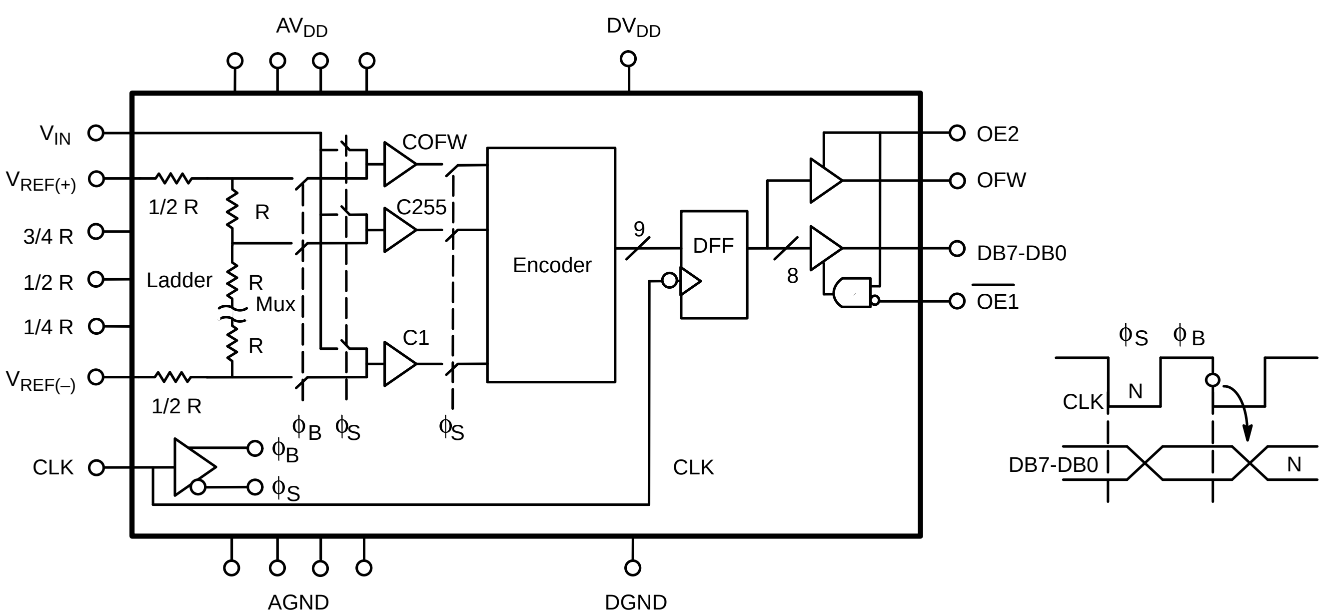
- Low Power for Lower System Noise
- Most Flexible Input Range of any A/D Available
- No Sample/Hold Needed
- Use MP7684A for New Designs

GENERAL DESCRIPTION

The MP7684 is an 8-bit monolithic CMOS single step high speed Analog-to-Digital Converter designed for precision applications in video and data acquisition requiring conversion rates to 10 MHz with differential linearity error less than 1/2 LSB and low power consumption. A unique feature of this converter is its input architecture which eliminates the need for an input track and hold and allows full scale input ranges from 1.2 to 5 volts peak-to-peak, referred to ground or offset. The user simply sets $V_{REF(-)}$ and $V_{REF(+)}$ to encompass the desired input range.

The MP7684 includes 256 clocked comparators, encoders, 3-state output buffers, a reference resistor ladder and associated timing circuitry. An overflow bit (or flag) has been provided to make it possible to achieve 9-bit resolution by connecting two devices in parallel. In normal operation this flag has no effect on the data bits.

SIMPLIFIED BLOCK AND TIMING DIAGRAM



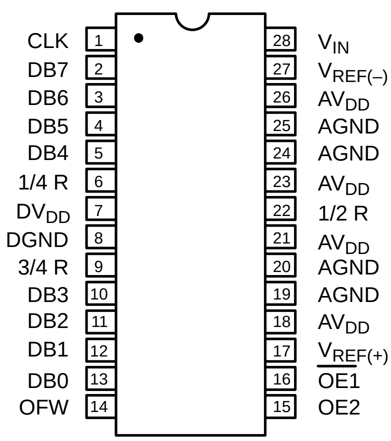
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP7684JN	±1 1/2	2
Plastic Dip	–40 to +85°C	MP7684KN	±1	1 1/2
SOIC	–40 to +85°C	MP7684JS	±1 1/2	2
SOIC	–40 to +85°C	MP7684KS	±1	1 1/2
Ceramic Dip	–40 to +85°C	MP7684JD	±1 1/2	2
Ceramic Dip	–40 to +85°C	MP7684KD	±1	1 1/2
Ceramic Dip	–55 to +125°C	MP7684SD*	±1 1/2	2
Ceramic Dip	–55 to +125°C	MP7684TD*	±1	1 1/2

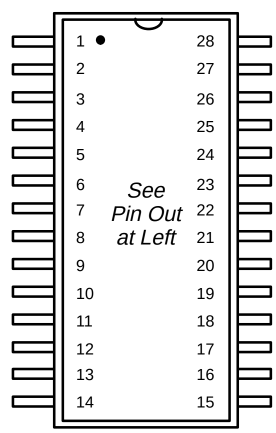
*Contact factory for availability

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP, CDIP (0.600”)
N28, D28



28 Pin SOIC (EIAJ, 0.335”)
R28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	CLK	Clock Input Pin
2	DB7	Data Output Bit 7 (MSB)
3	DB6	Data Output Bit 6
4	DB5	Data Output Bit 5
5	DB4	Data Output Bit 4
6	1/4R	1/4 of Resistance Ladder
7	DV_{DD}	Power Supply of Digital Circuit
8	DGND	Digital Ground
9	3/4R	3/4 of Resistance Ladder
10	DB3	Data Output Bit 3
11	DB2	Data Output Bit 2
12	DB1	Data Output Bit 1
13	DB0	Data Output Bit 0 (LSB)
14	OFW	Digital Output Overflow Pin
15	OE2	Output Enable Control Pin
16	$\overline{OE1}$	Output Enable Control Pin
17	$V_{REF(+)}$	Positive Reference Voltage Pin
18	AV_{DD}	Power Supply of Analog Circuit
19	AGND	Analog Circuit Ground
20	AGND	Analog Circuit Ground
21	AV_{DD}	Power Supply of Analog Circuit
22	1/2R	Center of Resistance Ladder
23	AV_{DD}	Power Supply of Analog Circuit
24	AGND	Analog Ground
25	AGND	Analog Ground
26	AV_{DD}	Power Supply of Analog Circuit
27	$V_{REF(-)}$	Negative Reference Voltage Pin
28	V_{IN}	Analog Input

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 5$ V, $F_S = 10$ MHz (Duty Cycle: 1/3 Sample & 2/3 Balance), $V_{REF(+)} = +4.1$ V, $V_{REF(-)}$ = AGND, $T_A = 25°C$

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		8			8		Bits	
Sampling Rate	F_S	0.1		6	0.1	6	MHz	For Specified Accuracy
ACCURACY (J, S Grades)[1]								
Differential Non-Linearity	DNL			±3/4		±1 1/2	LSB	
Integral Non-Linearity (Relative Accuracy)	INL			1 1/2		2	LSB	Best Fit Line (Max INL – Min INL) / 2
Zero Scale Error	EZS		2				LSB	
Full Scale Error	EFS		2				LSB	
ACCURACY (K, T Grades)[1]								
Differential Non-Linearity	DNL			±1/2		±1	LSB	
Integral Non-Linearity	INL			1		1 1/2	LSB	Best Fit Line
Zero Scale Error	EZS		2				LSB	
Full Scale Error	EFS		2				LSB	
DYNAMIC ACCURACY[2]								Histogram Test
Differential Non-Linearity	DNL		±0.3				LSB	F_{IN} = 390 kHz
REFERENCE VOLTAGES								
Positive Ref. Voltage[3]	$V_{REF(+)}$			AV_{DD}		AV_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			AGND		V	
Ladder Resistance	R_L	120		400	90	430	Ω	
Ladder Temp. Coefficient[2]	R_{TCO}					3000	ppm/°C	
ANALOG INPUT[2]								
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V p-p	
Input Capacitance Sample[4]	C_{IN}		50				pF	
Input Impedance	Z_{IN}		10				MΩ	
Aperture Delay	t_{AP}		25				ns	
Aperture Uncertainty (Jitter)	t_{AJ}		60				ps	
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	3.5			3.5		V	
Logical "0" Voltage	V_{IL}			1.5		1.5	V	
Leakage Currents[5]	I_{IN}							V_{IN}=DGND to DV_{DD}
CLK		–100		100		±100	µA	
$\overline{\text{OE1}}$[7]		–1		50	–1	75	µA	
OE2[6]		–60		1	–100	1	µA	
Input Capacitance[2]			5				pF	
Clock Timing (*See Figure 1.*)								
Duty Cycle			50				%	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Description	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Conditions
DIGITAL OUTPUTS								C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	4.3			4.3		V	I_{LOAD} = –1.0 mA
Logical "0" Voltage	V_{OL}			0.6		0.6	V	I_{LOAD} = 2.0 mA
Off Current	I_{OFF}		$\pm$1	10		$\pm$1.5 (typ)	µA	
Output Capacitance[2]	C_O		5				pF	
3-state Leakage	I_{OZ}		1	10		10	µA	V_{OUT}=DGND to DV_{DD}
Data Hold Time (*See Figure 1.*)[2]	t_{HLD}		50				ns	
Data Valid Delay[2]	t_{DL}		55				ns	
Data Enable Delay[2]	t_{DEN}		40				ns	
Data 3-state Delay[2]	t_{DHZ}		40				ns	
POWER SUPPLIES[9] (Tmin to Tmax)								
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4		6	4	6	V	
Current (AV_{DD} + DV_{DD})	I_{DD}			75		90	mA	

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (*Figure 3.*). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (*Figure 4.*). Accuracy is a function of the sampling rate (F_S).
2 Guaranteed. Not tested.
3 Specified values guarantee functionality. Refer to other parameters for accuracy.
4 See V_{IN} input equivalent circuit (*Figure 5.*). Switched capacitor analog input requires driver with low output resistance.
5 All inputs have diodes to DV_{DD} and DGND. Input $\overline{OE1}$ has internal pull down. Input OE2 has internal pull up. Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.
6 Internal resistor to DV_{DD} biases unconnected input to active high logical level.
7 Internal resistor to GND biases unconnected input to active low logical level.
8 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.
9 DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package and to the analog supply.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND . . . . +7 V
$V_{REF(+)}$ & $V_{REF(-)}$ . . . . GND –0.5 to V_{DD} +0.5 V
V_{IN} . . . . GND –0.5 to V_{DD} +0.5 V
All Inputs . . . . GND –0.5 to V_{DD} +0.5 V
All Outputs . . . . GND –0.5 to V_{DD} +0.5 V

Storage Temperature . . . . –65 to +150°C
Lead Temperature (Soldering 10 seconds) . . . . +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC, LCC 1050mW
Derates above 75°C . . . . 14mW/°C

NOTES:

(1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
(2) Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
(3) V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

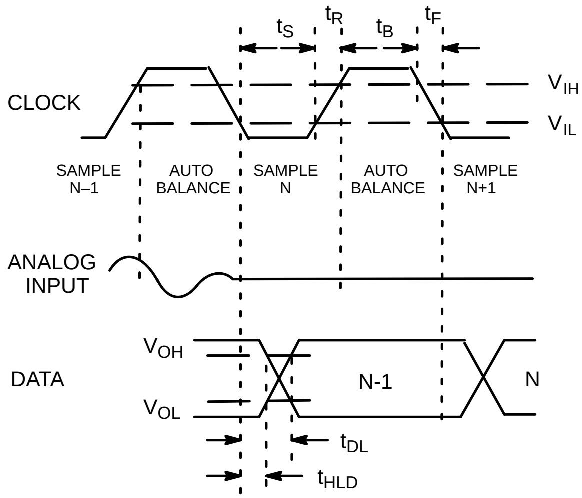


Figure 1. MP7684 Timing Diagram

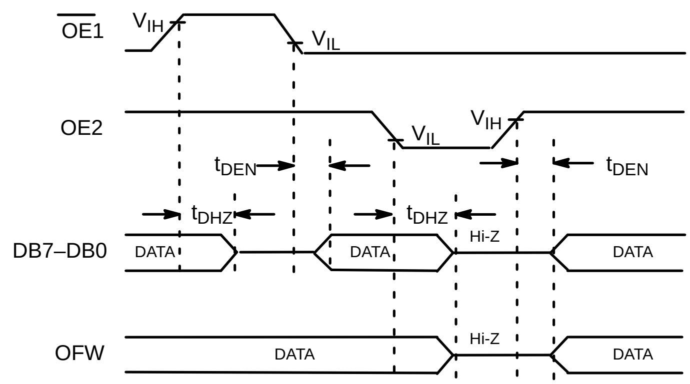
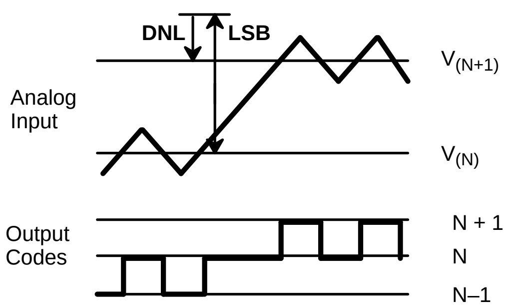


Figure 2. Output Enable/Disable Timing Diagram



(N) Code Width = $V_{(N+1)} - V_{(N)}$
LSB = [$V_{REF(+)} - V_{REF(-)}$] / 256

$$\mathbf{DNL_{(N)} = [\ V_{(N+1)} - V_{(N)}\ ] - LSB}$$

Figure 3. DNL Measurement

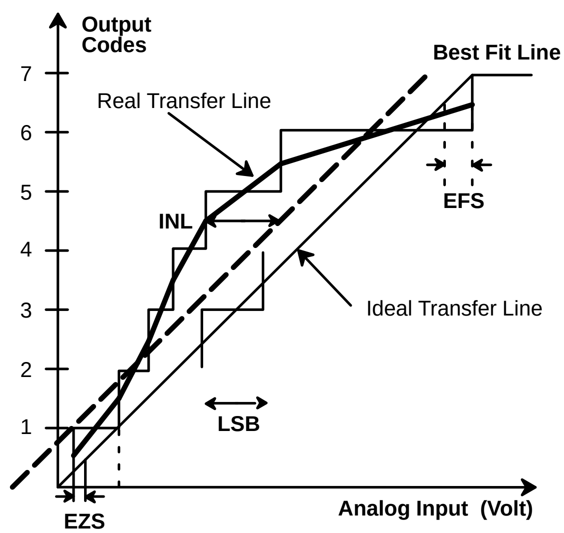


Figure 4. INL Error Calculation

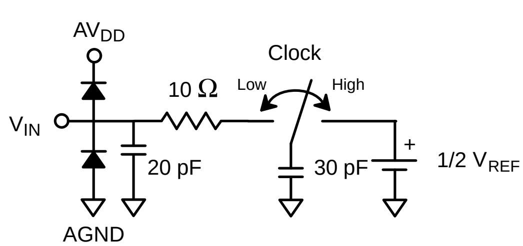


Figure 5. Analog Input Equivalent Circuit

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP7684 converts analog voltages into 256 digital codes by encoding the outputs of 255 comparators. A 256th comparator is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 1.5 clock periods. Data is transferred from the comparator latches to the output registers each clock period and at the same time the input is sampled.

The clock signal generates the two internal phases, ϕ_B (CLK high = balance) and ϕ_S (CLK low = sample). ϕ_B connects the comparators to the reference tap points. ϕ_S connects the comparators to the analog input voltage.

The reference resistance ladder is a series of 257 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 256 * R \qquad V_{REF} = V_{REF(+)} – V_{REF(–)} = 256 * LSB$

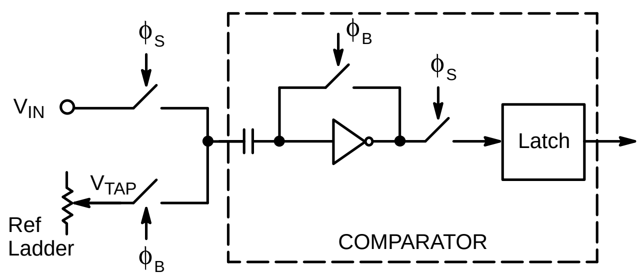


Figure 6. MP7684 Comparator

The MP7684 comparators use the balance phase (ϕ_B) to charge one plate of the capacitors to the reference ladder tap point (V_{TAP}) and the other to the inverter/comparator trigger point. During the sample phase (ϕ_S) one plate of the capacitors switches to V_{IN}. The change in voltage ($V_{IN} – V_{TAP}$) transfers across the capacitor and forces the inverter into one of the two possible logic states. A latch (connected to the comparator during ϕ_S) restores and propagates the digital level to the encode logic.

The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latch from the comparator. This delay is called aperture delay (t_{AP}).

The aperture delay is not constant but changes from one cycle to the next. Internal thermal noise, power supply noise and slow input clock edges are major contributors to this variation. The aperture jitter (t_{AJ}) is the variation of the aperture delay distribution.

This uncertainty shows as digital code errors if the input slew rate multiplied by t_{AJ} is of the same order of magnitude as the LSB. That is if $(dv/dt) * t_{AJ} \approx V_{REF}/256$, an internal error of 1 LSB results.

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 7.*

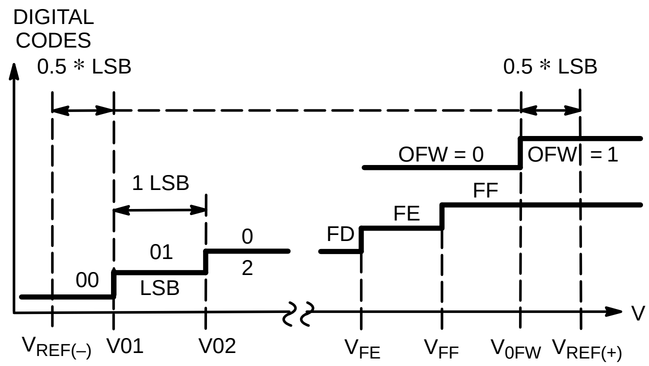


Figure 7. Ideal A/D Transfer Function

The overflow transition (V0FW) takes place at:

$V_{IN} = V_{0FW} = V_{REF(+)} – 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V01 = V_{REF(–)} + 0.5 * LSB$

$V_{IN} = V_{FF} = V_{REF(–)} – 1.5 * LSB$

$LSB = (V_{REF(+)} – V_{REF(–)} / 256 = (V_{FF} – V01) / 254$

Note that the overflow transition is a flag and has no impact on the data bits.

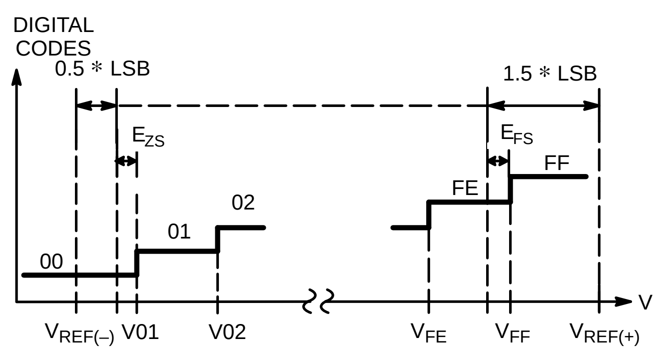


Figure 8. Real A/D Transfer Curve

In a “real” converter, the code-to-code transitions do not fall exactly every ($V_{REF(+)} – V_{REF(–)}$) / 256 volts.

A positive DNL (Differential Non Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSB’s.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = $\pm$ 0.5 LSB means that all codes are within 0.5 and 1.5

LSB. If V_{REF} = 4.096 V then 1 LSB = 16mV and every code width is within 8 and 24 mV.

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (EZS, EFS) are:

DNL (01) = V02 – V01 – LSB

: : :

DNL (FE) = $V_{FF} - V_{FE}$ – LSB

EFS (full scale error) = $V_{FF} - [V_{REF(+)} - 1.5 * LSB]$

EZS (zero scale error) = $V_{01} - [V_{REF(-)} + 0.5 * LSB]$

Figure 4. shows the zero scale and full scale error terms.

Systems that adjust the V_{REF} voltages to correct for EFS and EZS only increase the accuracy at the two extreme points. In the MP7684, such adjustments have little impact at frequencies lower than 10 MHz. Refer to the characterization data for temperature and frequency dependence.

Figure 4. gives a visual definition of the INL error. The chart shows a 3-bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, a line is drawn parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and the negative INL errors. This may change an INL of –1 to +2 LSB's relative to the Ideal Line into a $\pm$1.5 relative to the Best Fit Line.

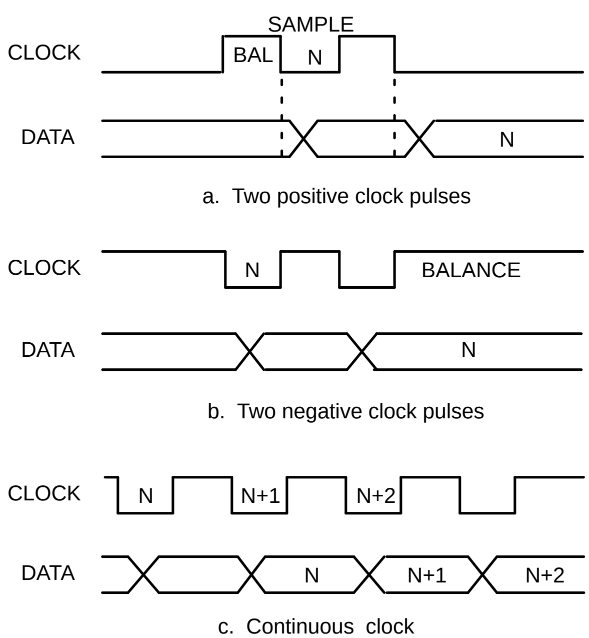


Figure 9. Relationship of Data to Clock

Clock Timing

A system will clock the MP7684 continuously (*Figure 9a.*) or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 9b.* keeps the MP7684 comparators in balance and ready to sample the analog input. This mode draws the most current from V_{DD}. The timing of *Figure 9c.* leaves the comparator inputs floating (and AC coupled to the V_{IN} input) and a balance phase is needed before a valid sampling phase. In this mode, I_{DD} varies because of the floating comparator inputs.

Analog Input

The MP7684 has very flexible input range characteristics. The user sets $V_{REF(+)}$ and $V_{REF(-)}$ to fixed voltages and then varies the input DC and AC levels to match the V_{REF} range.

Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The MP7684's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. These have an impact above 5 MHz and they are very important above 10 MHz. Use of Current Feedback Amplifiers is an easy and cost effective way to maximize performance.

Reference Voltages

If the input bandwidth is limited to the Nyquist region ($F_{IN} < F_S/2$) then the two reference voltages can be set at any two values between the supplies. V_{REF} (their difference) can be reduced down to 1.5 volts with minor change in accuracy. If the input bandwidth exceeds $F_S/2$, then it is recommended that VREF be lower than $V_{DD}/2$.

At V_{REF} = 1.5 V, the LSB is reduced to 6mV. Further reductions show an increased error in terms of LSB (which is getting smaller) even if the error in terms of mV remains constant.

The input/output relationship as a function of V_{REF}:

$$A_{IN} = (V_{IN} - V_{REF(-)})$$
$$DATA = 256 * (A_{IN}/V_{REF})$$

a) **Gain adjustment.** A system can increase total gain by reducing V_{REF}.

b) **Increasing dynamic range**. A system can increase dynamic range by using DAC's to control V_{REF} and by "focusing" on input ranges of interest. In digitizing "static" information (an image in a scanner), a first digitization would point to the input range in which most of the output codes fall. The system then would adjust the DACs to generate $V_{REF(+)}$ and $V_{REF(-)}$ to include just the range of interest for the second and final pass.

c) **Subranging; increasing resolution**. Where practical, multiple passes at different V_{REF} ranges can increase resolution without changing hardware. A system needs to make four passes to increase the resolution to 10 bits. The merging of the data from the four passes can create DNL errors at the borders of the ranges. One solution is to "overlap" the ranges and to use software methods to properly merge the ranges.

Digital Interfaces

The logic encodes the 255 bits into a binary code and latches the data in a D-type flip-flop for output. The inputs $\overline{\text{OE1}}$ and OE2 control the output buffers in an asynchronous mode.

$\overline{\text{OE1}}$	OE2	OFW	DB7 – DB0
X	0	High Z	High Z
1	1	Valid	High Z
0	1	Valid	Valid

Table 1. Output Enable Logic

If another DFF is to follow the ADC, it is recommended that the system latches the data at the negative going edge of the clock. This will work at any frequency. If the system must latch with the positive going edge, then care must be taken to avoid the overlay of the clock edge with the changing outputs.

If a latch follows the ADC, the positive half of the clock used as enable signal guarantees stable output at the end of the enable pulse.

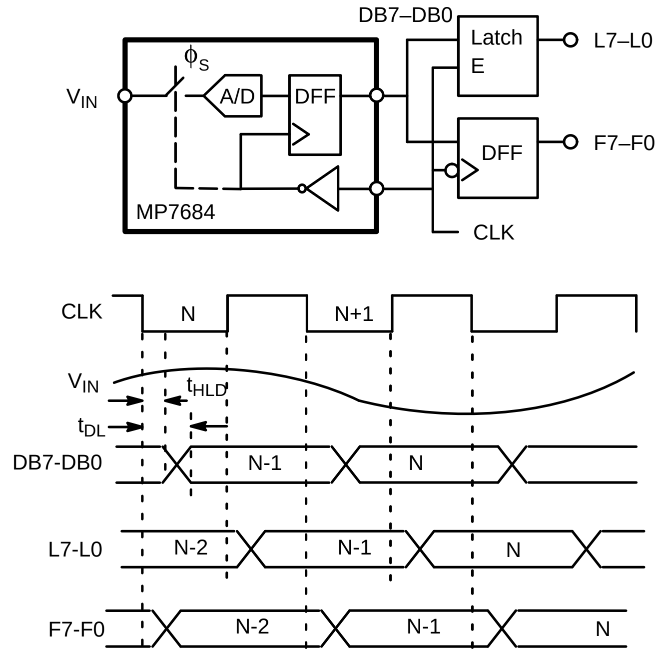


Figure 10. MP7684 Functional Equivalent Circuit and Interface Timing

APPLICATION NOTES

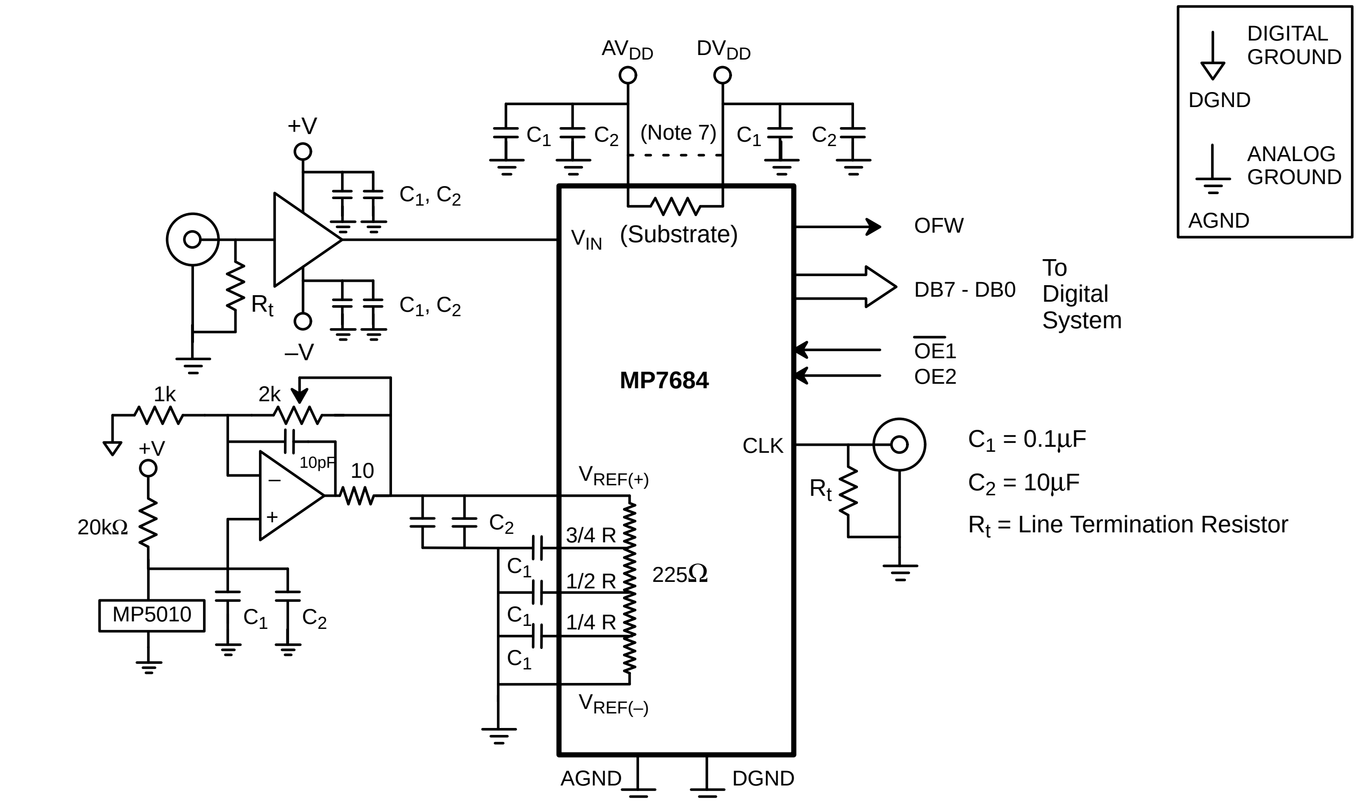
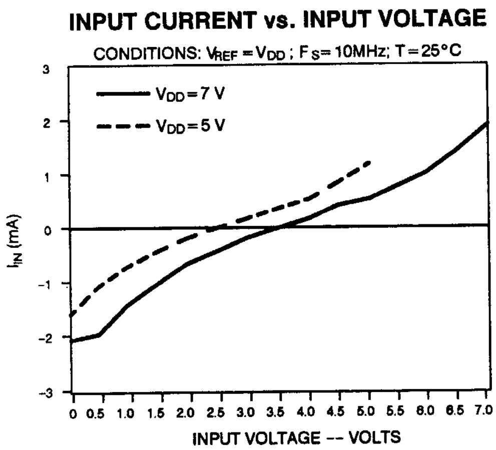
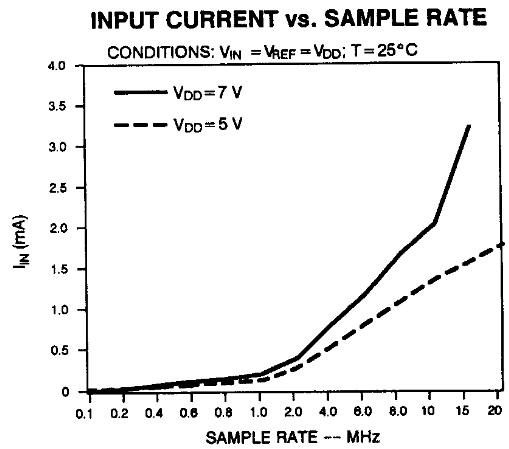
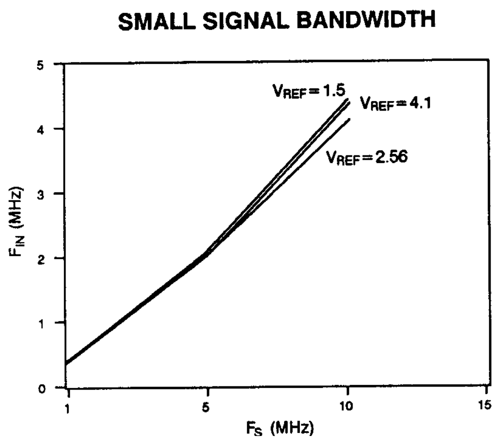


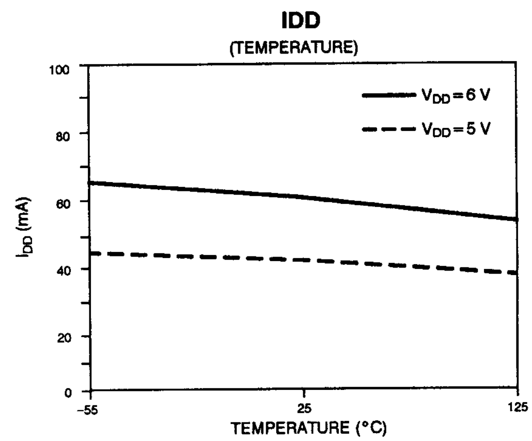
Figure 11. Typical Circuit Connections

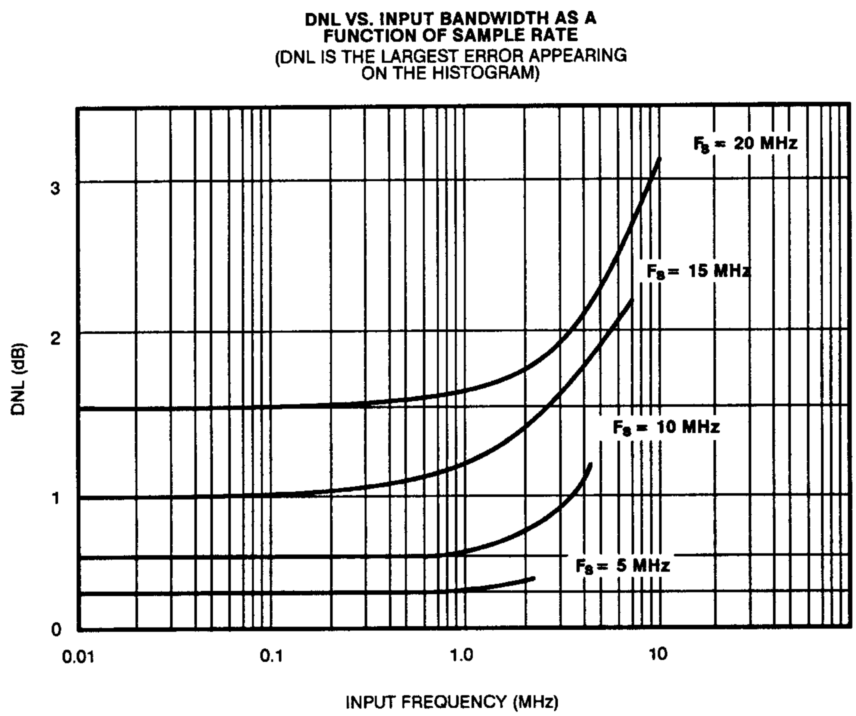
1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP7684A inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of MP7684. <u>Use of wire wrap is not recommended.</u>
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs to minimize cross coupling and noise pickup.
5. The analog input should be driven by a buffer op amp with as low output impedance as possible. The impedance should be less than 50Ω for clock frequencies above 10 MHz.
6. <u>Analog and digital ground planes should be substantial and common at one point only.</u> The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths.
7. DV_{DD} should not be shared with other digital circuitry. DV_{DD} for the MP7684 should be connected to AV_{DD} next to the MP7684.
8. DV_{DD} and AV_{DD} are connected inside the MP7684 through the N – doped silicon substrate. DC voltage differences between DV_{DD} and AV_{DD} will cause undesirable internal currents.
9. The power supplies and reference voltages should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used.


INPUT CURRENT vs. INPUT VOLTAGE
CONDITIONS: VREF = VDD ; FS = 10MHz; T = 25°C
VDD = 7 V
VDD = 5 V
IIN (mA)
INPUT VOLTAGE -- VOLTS

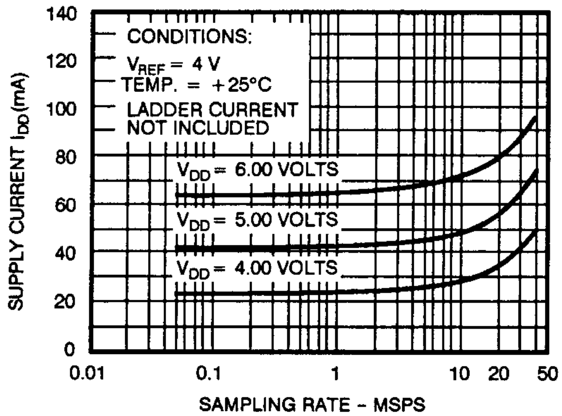

INPUT CURRENT vs. SAMPLE RATE
CONDITIONS: VIN = VREF = VDD; T = 25°C
VDD = 7 V
VDD = 5 V
IIN (mA)
SAMPLE RATE -- MHz


SMALL SIGNAL BANDWIDTH
VREF = 1.5
VREF = 4.1
VREF = 2.56
FIN (MHz)
FS (MHz)

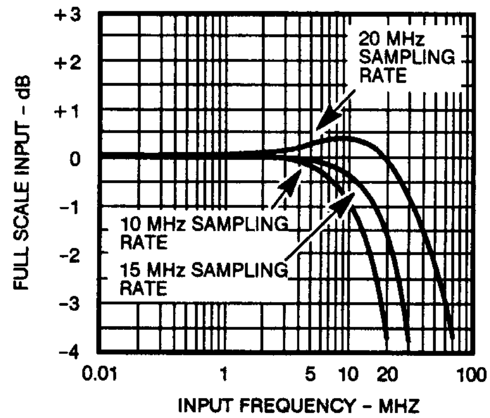

IDD
(TEMPERATURE)
VDD = 6 V
VDD = 5 V
IDD (mA)
TEMPERATURE (°C)


DNL VS. INPUT BANDWIDTH AS A
FUNCTION OF SAMPLE RATE
(DNL IS THE LARGEST ERROR APPEARING
ON THE HISTOGRAM)
FS = 20 MHz
FS = 15 MHz
FS = 10 MHz
FS = 5 MHz
DNL (dB)
INPUT FREQUENCY (MHz)

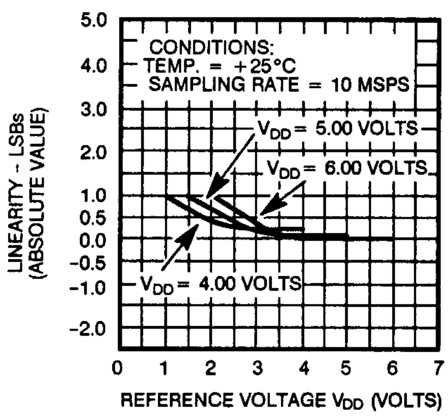
POWER CONSUMPTION VS. SAMPLING RATE



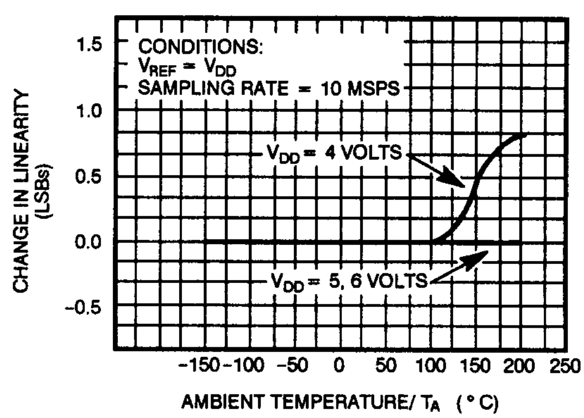
FULL SCALE INPUT VS. INPUT FREQUENCY AS A FUNCTION OF SAMPLING RATE



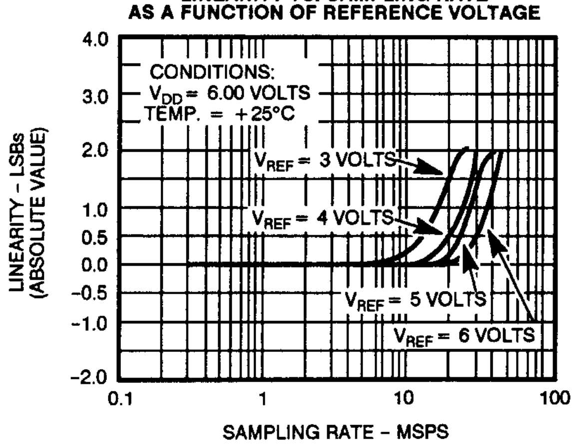
REFERENCE VOLTAGE VS. LINEARITY



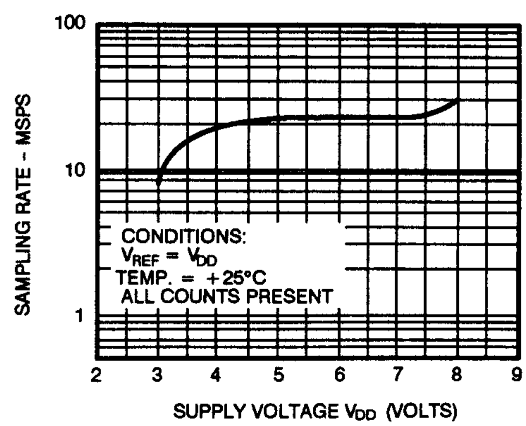
LINEARITY VS. TEMPERATURE AS A FUNCTION OF V_{DD}



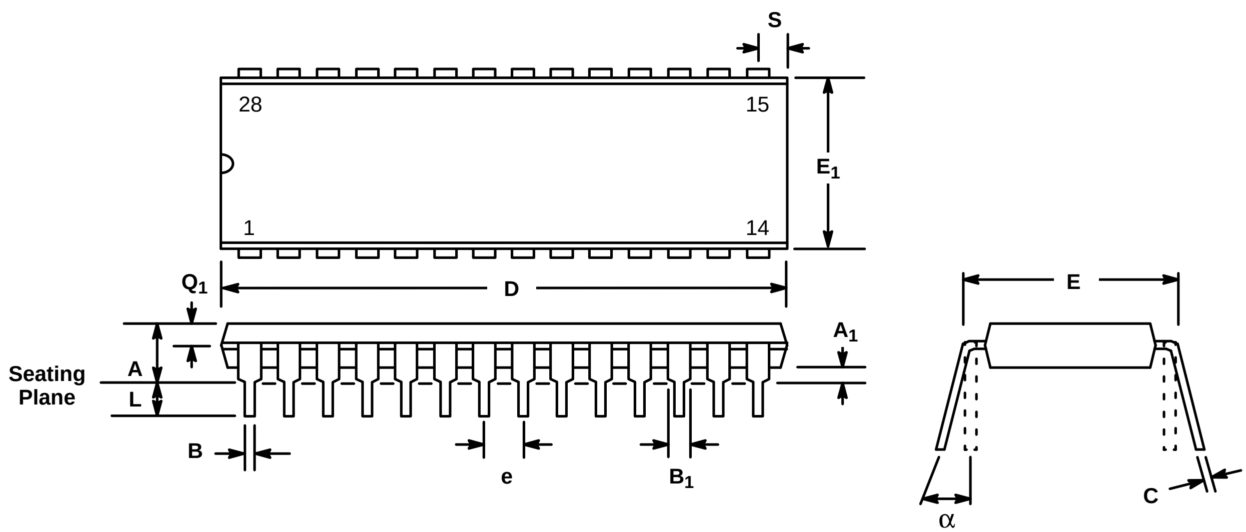
LINEARITY VS. SAMPLING RATE AS A FUNCTION OF REFERENCE VOLTAGE



SAMPLING RATE VS. SUPPLY VOLTAGE



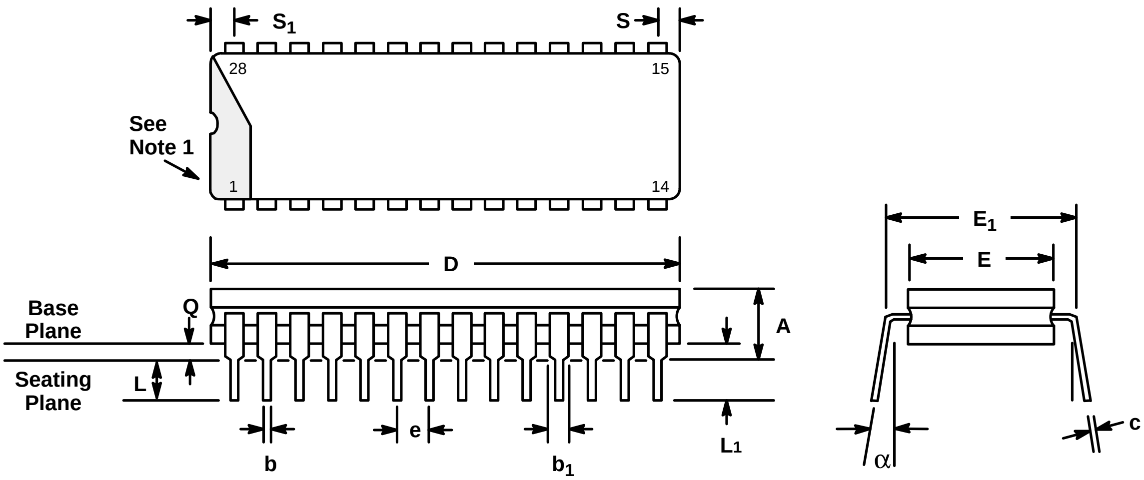
28 LEAD PLASTIC DUAL-IN-LINE
(600 MIL PDIP)
N28



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	—	0.232	—	5.893
A_1	0.015	—	0.381	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.380	1.490	35.05	37.85
E	0.585	0.625	14.86	15.88
E_1	0.500	0.610	12.70	15.49
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.020	0.100	1.508	2.54

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

28 LEAD CERAMIC DUAL-IN-LINE
(600 MIL CDIP)
D28

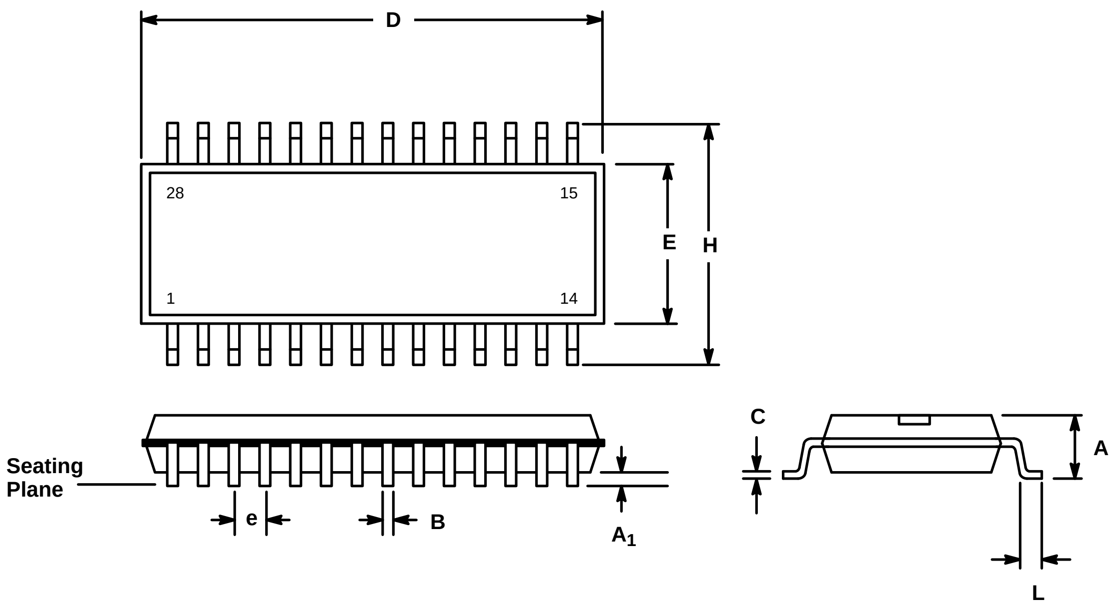


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.232	—	5.89	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	1.490	—	37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.060	0.381	1.52	3
S	—	0.100	—	2.54	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

28 LEAD SMALL OUTLINE
(335 MIL EIAJ SOIC)
R28



SYMBOL	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.60	2.80	0.102	0.110
A_1	0.2 (typ.)		0.008 (typ.)	
B	0.3	0.5	0.012	0.020
C	0.10	0.20	0.004	0.008
D	17.6	18.0	0.693	0.709
E	8.3	8.5	0.327	0.335
e	1.27 (typ.)		0.050 (typ.)	
H	11.5	12.1	0.453	0.477
L	0.8	1.2	0.031	0.047

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