MP7680

5 V CMOS 12-Bit
Quad Double-Buffered Multiplying
Digital-to-Analog Converter

FEATURES

- **MPS Pioneered Segmented DAC Approach**
- **Four Double-Buffered 12-bit DACs on a Single Chip**
- **Independent Reference Inputs**
- **Lowest Gain Error in a Multiple DAC Chip**
- **Guaranteed Monotonic - All Grades, All Temperatures**
- **TTL/5 V CMOS Compatible Inputs**
- **Industry Standard Digital Interface**
- **Four Quadrant Multiplication**
- **Latch-Up Free**

BENEFITS

- **Reduced Board Space; Lower System Cost.**
- **Independent Control of DACs**
- **Excellent DAC-to-DAC Matching and Tracking**

APPLICATIONS

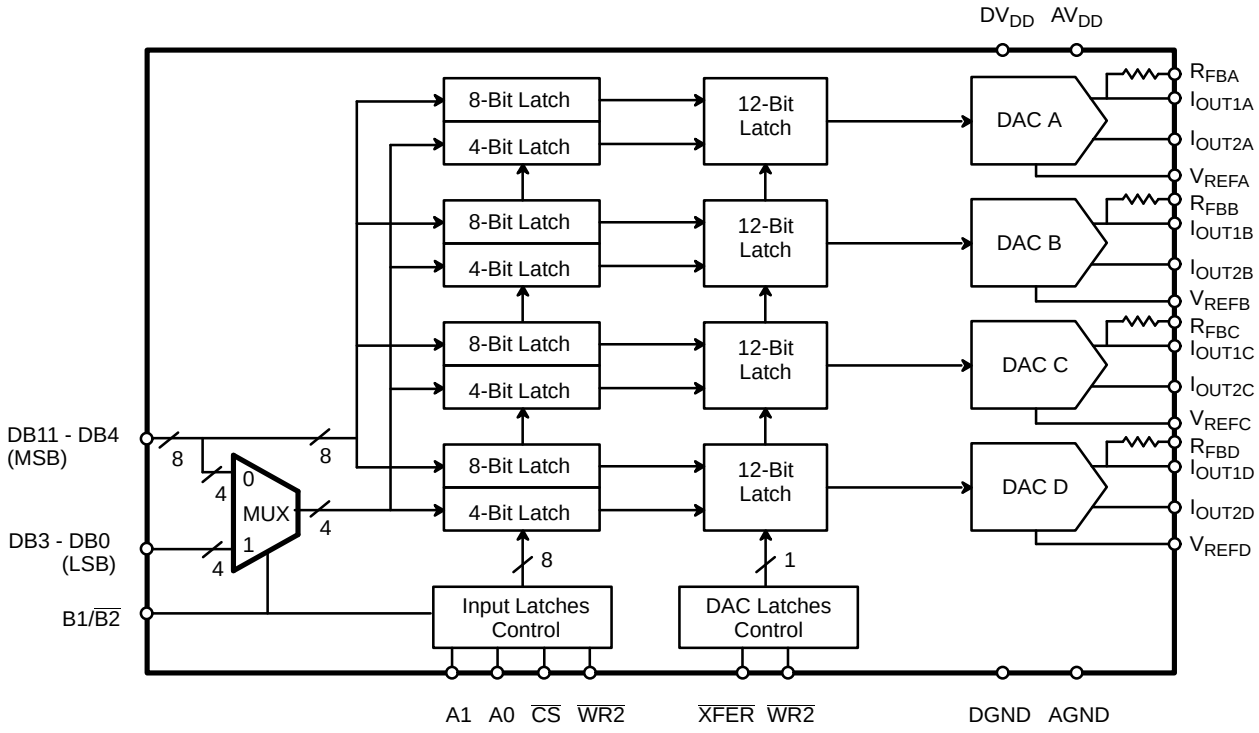
- **Function Generators**
- **Automatic Test Equipment**
- **Precision Process Controls**
- **Recording Studio Control Boards**

GENERAL DESCRIPTION

The MP7680 and the integrate four 12-bit four-quadrant-multiplying DACs with independent reference inputs and excellent matching characteristics. The MP7680 grades offer 1/2, 1 and 2 LSB of relative accuracy. The superior offers a low 2 LSB of gain error.

Each DAC has double-buffering (an 8 and 4-bit latch and a 12-bit latch) between the data bus (DB11 - DB0) and the DAC. The internal 4-bit mux allows the use of 8 or 16-bit buses. The flexible latch control logic allows to update one or more DACs simultaneously.

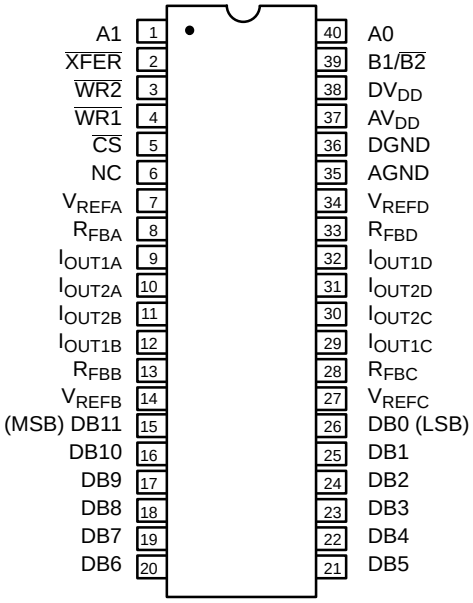
SIMPLIFIED BLOCK DIAGRAM



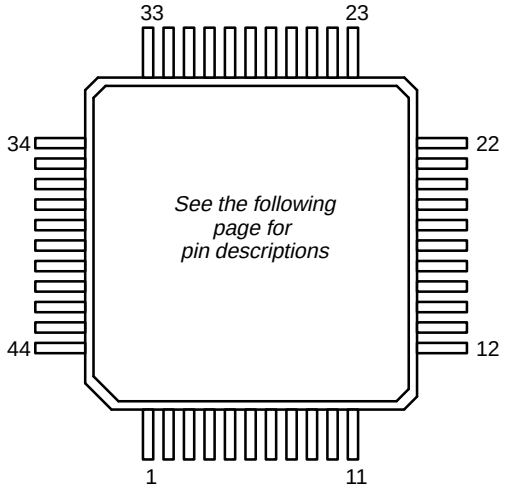
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	–40 to +85°C	MP7680JN	±2	±4	±16
Plastic Dip	–40 to +85°C	MP7680KN	±1	±2	±16
Ceramic Dip	–40 to +85°C	MP7680JD	±2	±4	±16
Ceramic Dip	–40 to +85°C	MP7680KD	±1	±2	±16
PQFP	–40 to +85°C	MP7680JE	±2	±4	±16
PQFP	–40 to +85°C	MP7680KE	±1	±2	±16
Ceramic Dip	–55 to +125°C	MP7680SD	±2	±4	±16

PIN CONFIGURATIONS



40 Pin PDIP, CDIP (0.600")
N40, D40



44 Pin PQFP
Q44

PIN OUT DEFINITIONS

40 Pin PDIP, CDIP

PIN NO.	NAME	DESCRIPTION
1	A1	DAC Address Bit 1
2	$\overline{XFER}$	Transfer: Updates all DAC's
3	$\overline{WR2}$	Write 2: Gates the $\overline{XFER}$ Function
4	$\overline{WR1}$	Write 1: Gates the DAC Selection
5	$\overline{CS}$	Chip Select
6	NC	No Connection
7	V_{REFA}	Reference Input for DAC A
8	R_{FBA}	Feedback Resistor for DAC A
9	I_{OUT1A}	Current Output A
10	I_{OUT2A}	Complement of Output A
11	I_{OUT2B}	Complement of Output B
12	I_{OUT1B}	Current Output B
13	R_{FBB}	Feedback Resistor for DAC B
14	V_{REFB}	Reference Input for DAC B
15 – 26	DB11 to DB0	Input Data Bits 11 (MSB) to 0 (LSB)
27	V_{REFC}	Reference input for DAC C
28	R_{FBC}	Feedback Resistor for DAC C
29	I_{OUT1C}	Current Output C
30	I_{OUT2C}	Complement of Output C
31	I_{OUT2D}	Complement of Output D
32	I_{OUT1D}	Current Output D
33	R_{FBD}	Feedback Resistor for DAC D
34	V_{REFD}	Reference input for DAC D
35	AGND	Analog Ground
36	DGND	Digital Ground
37	AV_{DD}	Analog Power Supply
38	DV_{DD}	Digital Power Supply
39	B1/$\overline{B2}$	Select Input Format (8/4 or 12 bits in)
40	A0	DAC Address Bit 0

44 Pin PQFP

PIN NO.	NAME	DESCRIPTION
1	NC	No Connection
2	V_{REFA}	Reference Input for DAC A
3	R_{FBA}	Feedback Resistor for DAC A
4	I_{OUT1A}	Current Output A
5	I_{OUT2A}	Complement of Output A
6	NC	No Connection
7	I_{OUT2B}	Complement of Output B
8	I_{OUT1B}	Current Output B
9	R_{FBB}	Feedback Resistor for DAC B
10	V_{REFB}	Reference Input for DAC B
11-16	DB11 to DB6	Input Data Bits 11 (MSB) to 6
17	NC	No Connection
18-23	DB5-DB0	Input Data Bits 5 to 0 (LSB)
24	V_{REFC}	Reference input for DAC C
25	R_{FBC}	Feedback Resistor for DAC C
26	I_{OUT1C}	Current Output C
27	I_{OUT2C}	Complement of Output C
28	NC	No Connection
29	I_{OUT2D}	Complement of Output D
30	I_{OUT1D}	Current Output D
31	R_{FBD}	Feedback Resistor for DAC D
32	V_{REFD}	Reference input for DAC D
33	AGND	Analog Ground
34	DGND	Digital Ground
35	AV_{DD}	Analog Power Supply
36	DV_{DD}	Digital Power Supply
37	B1/$\overline{B2}$	Select Input Format (8/4 or 12 bits in)
38	A0	DAC Address Bit 0
39	NC	No Connection
40	A1	DAC Address Bit 1
41	$\overline{XFER}$	Transfer: Updates all DAC's
42	$\overline{WR2}$	Write 2: Gates the $\overline{XFER}$ Function
43	$\overline{WR1}$	Write 1: Gates the DAC Selection
44	$\overline{CS}$	Chip Select

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 5 V, V_{REF} = +10 V, I_{OUT1} = I_{OUT2} = DGND = AGND = 0 V Unless Otherwise Noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
K				±1		±1		
J, S				±2		±2		
Differential Non-Linearity	DNL						LSB	
K				±1		±2.0		
J, S				±4		±4.0		
Gain Error	GE						LSB	Using Internal R_{FB}
K				±16		±16		
J, S				±16		±16		
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±50		±70	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}			±50		±200	nA	I_{OUT1} V_{IN} = 0 V I_{OUT2} V_{IN} = V_{DD}
DYNAMIC PERFORMANCE[2]								R_L=100Ω, C_{EXT}=13pF
Current Settling Time	t_S		1.0				µs	Full scale change to 1/2 LSB
REFERENCE INPUT								
Input Resistance	R_{IN}	3	5	7	3	7	kΩ	
Voltage Input Range[2]	V_{IN}		±10	±25			V	
DIGITAL INPUTS								
Input High Voltage	V_{IH}	2.4			2.4		V	
Input Low Voltage	V_{IL}			0.8		0.8	V	
Input Current	I_{LKG}			±1		±4	µA	V_{IN} = 0 V and V_{DD}
Input Capacitance[2]								
Data	C_{IN}		7.0				pF	
Control	C_{IN}		7.0				pF	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}		100				pF	DAC all 1's
	C_{OUT1}		50				pF	DAC all 0's
	C_{OUT2}		50				pF	DAC all 1's
	C_{OUT2}		100				pF	DAC all 0's

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLY[4]								
Functional Voltage Range	V_{DD}	4.5		5.5	4.5	5.5	V	
Supply Current	I_{DD}			2		2	mA	Digital inputs = V_{IL} or V_{IH}
				1		1	mA	Digital inputs = 0 or 5 V
TIMING CHARACTERISTICS[2, 3]								
Write Pulse Width	t_{WR}	75			85		ns	
Chip Select Set-Up Time	t_{CS}	100			120		ns	
Address Set-Up Time	t_{AS}	100			120		ns	
Chip Select and Address Hold Time	t_H	0			0		ns	
Latch Select Set-Up Time	t_{BS}	120			150		ns	
Latch Select Hold Time	t_{BH}	10			15		ns	
Data Valid Set-Up Time	t_{DS}	100			120		ns	
Data Valid Hold Time	t_{DH}	0			0		ns	
Transfer Pulse Width	t_{XFER}	65			75		ns	
Write Cycle (per DAC)	t_{WC}	175			200		ns	

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.

2 Guaranteed but not production tested.

3 See timing diagram (*Figure 1.*).

4 DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package. DC voltage differences will cause undesirable internal currents.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1, 2]

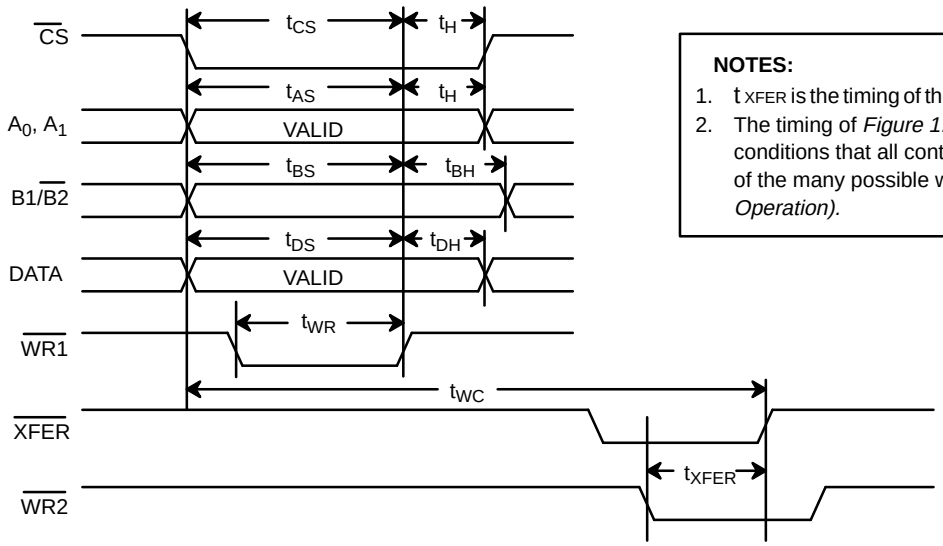
V_{DD} to AGND ..... –0.5 to +7 V
V_{DD} to DGND ..... –0.5 to +7 V
Digital Input Voltage to DGND ... GND –0.5 to V_{DD} +0.5 V
Any I_{OUT1}, I_{OUT2} to AGND ..... GND –0.5 to V_{DD} +0.5 V
Any V_{REF} to AGND ..... ±25 V
AGND to DGND ..... ±1 V
(Functionality Guaranteed ±0.5 V)

Any V_{RFB} to AGND ..... ±25 V
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, PQFP 800mW
Derates above 75°C ..... 11mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.



NOTES:

1. t_{XFER} is the timing of the condition $\overline{XFER}$ = $\overline{WR2}$ = Low.
2. The timing of *Figure 1.* reproduces graphically the conditions that all control signals must meet in any of the many possible writing cycles (*see Theory of Operation).*

Figure 1. Write Cycle Timing (Each DAC)

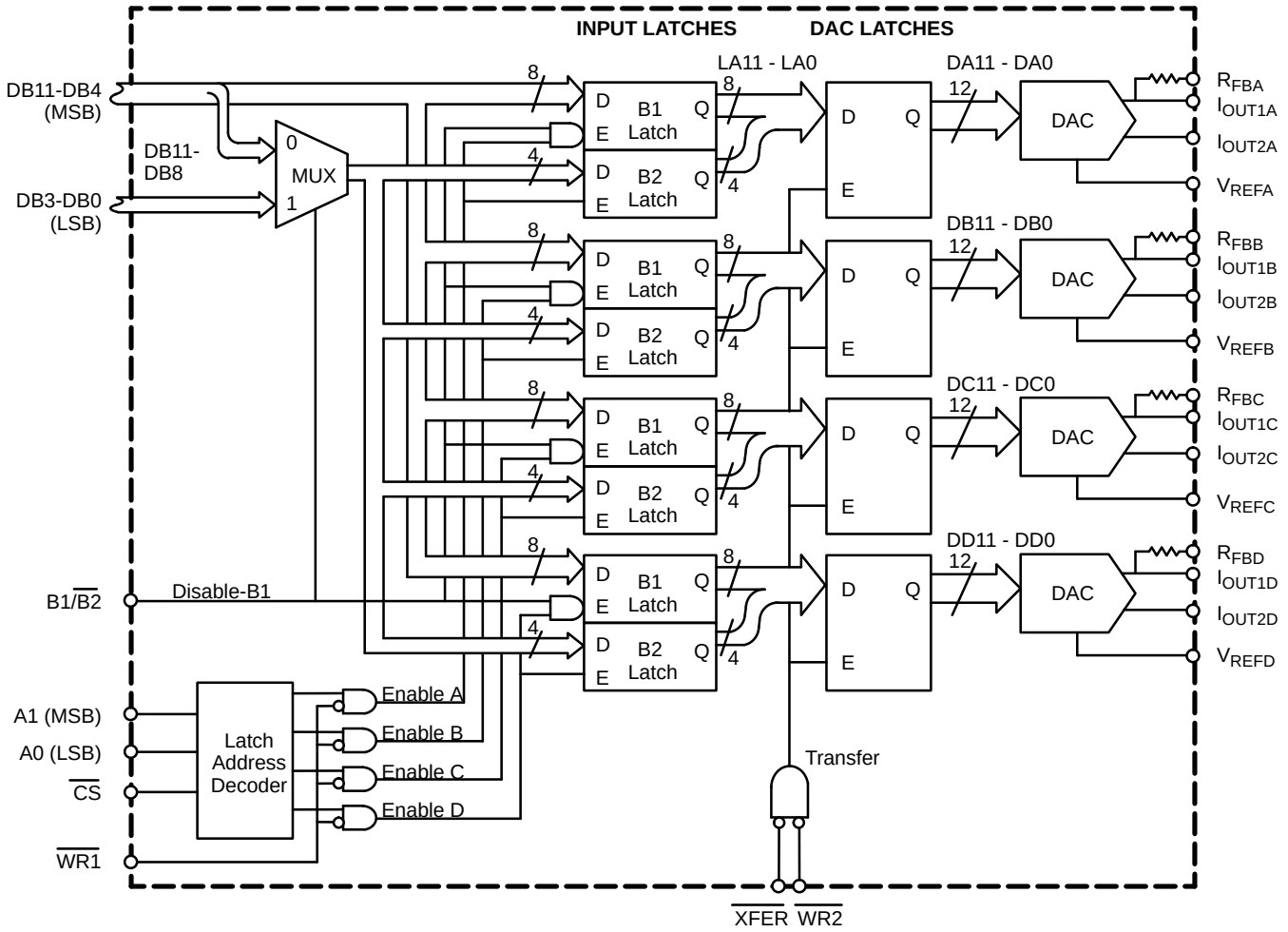


Figure 2. Latches Control Logic

THEORY OF OPERATION

Digital Interface

Figure 2. shows the internal control logic. The logic that controls the writing of the input latches and the one that controls the DAC latches are completely separated. It is easy to understand how the MP7680/80A works by understanding each basic operation.

Writing to Input Latches

By keeping B1/$\overline{B2}$ = high, a 12-bit bus has direct access to the 12 bits of the input latches. The condition $\overline{CS}$ = $\overline{WR1}$ = 0 loads the values contained in the data bus DB11-DB0 into the input latch addresses by A_1, A_0 (*Figure* 3a, *Table 1.*).

A_1	A_0	SELECTED DAC
0	0	A
0	1	B
1	0	C
1	1	D

Table 1. DAC Selection

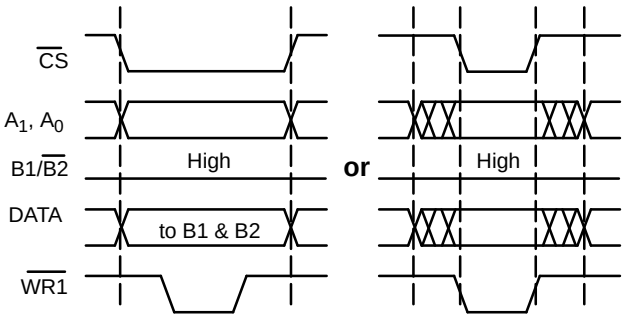


Figure 3a. 12 Bit Write Cycle

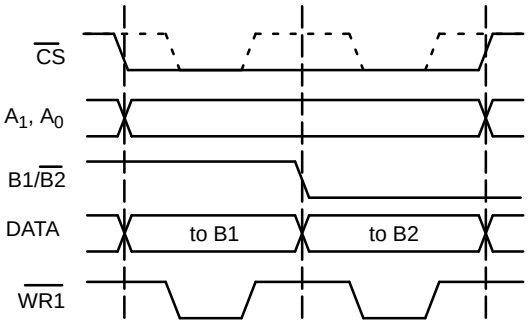


Figure 3b. 8-Bit Double Write Cycle

Figure 3. Write Cycles to Input Latches

An 8-bit bus must use two cycles. The second cycle is like the first one with the difference that B1/$\overline{B2}$ = low (*Figure 3b*). During the second cycle the condition B1/$\overline{B2}$ = low muxes DB11-DB8 to the B2 latches (*Figure 2.*).

Two important notes:

1) Timing diagrams show the inputs $\overline{CS}$, A_1, A_0, DB11-DB0 to be stable during the entire writing cycle. In reality all the above signals can change (*Figure 3a*) as long as they meet the timing conditions specified in the Electrical Characteristic Table.

2) Only 16-bit bus cycles are shown in the next few examples of interface timing. It is possible to generate an 8-bit interface timing by replacing a single 12-bit write cycle (*Figure 3a*) with a double 8-bit write cycles (*Figure 3b*). 8-bit applications should ground inputs DB3-DB0.

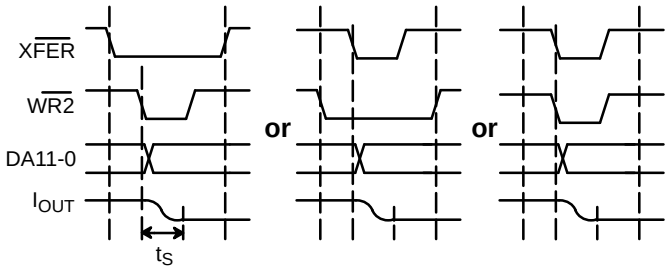


Figure 4. Transfer Cycles from Input Latches to DAC Latches

Transferring Data to the DAC Latches

Once one or all of the input latches have been loaded, the condition $\overline{XFER}$ = $\overline{WR2}$= low transfers the content of ALL the input latches in the DAC latches. The output of the DAC latches (DA11-DA0) changes and the DAC current (I_{OUT}) will reach a new stable value within the settling time t_S (*Figure 4.*).

Examples of DACs updating sequences:

1) Simultaneous updates of any number of DACs. The system uses from one (two) to four (eight) cycles to write from a 12 (8) bit bus into B1/$\overline{B2}$ latches. One transfer cycle updates the output of all DACs (*Figure 5.*)
2) Individual DAC update. The condition $\overline{WR2}$ = $\overline{XFER}$ = low makes the DAC latches transparent. A writing to the B1/$\overline{B2}$ latches updates the DAC outputs (*Figure 6.*).
3) Automatic transfer to DAC latches. An 8-bit bus can update any DAC with two cycles by connecting $\overline{WR1}$ = $\overline{WR2}$ and B1/$\overline{B2}$= $\overline{XFER}$. This is the correct individual DAC update for 8-bit busses (*Figure 7.*).
4) Transfer by a second device. A processor may load the input latches while the final $\overline{XFER}$ pulse is left to another device.

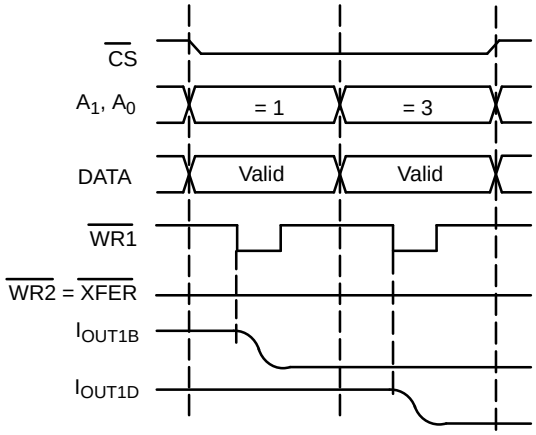


Figure 6. Individual DAC Update

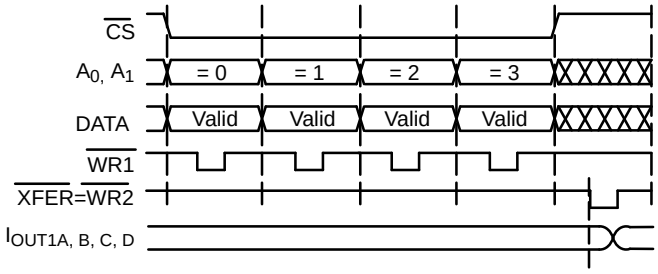


Figure 5. Simultaneous Updates of DACs

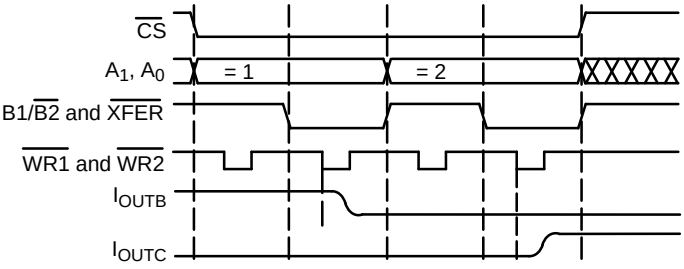


Figure 7. Automatic Transfer to DAC Latches

APPLICATION NOTES

Refer to Section 8 for Applications Information

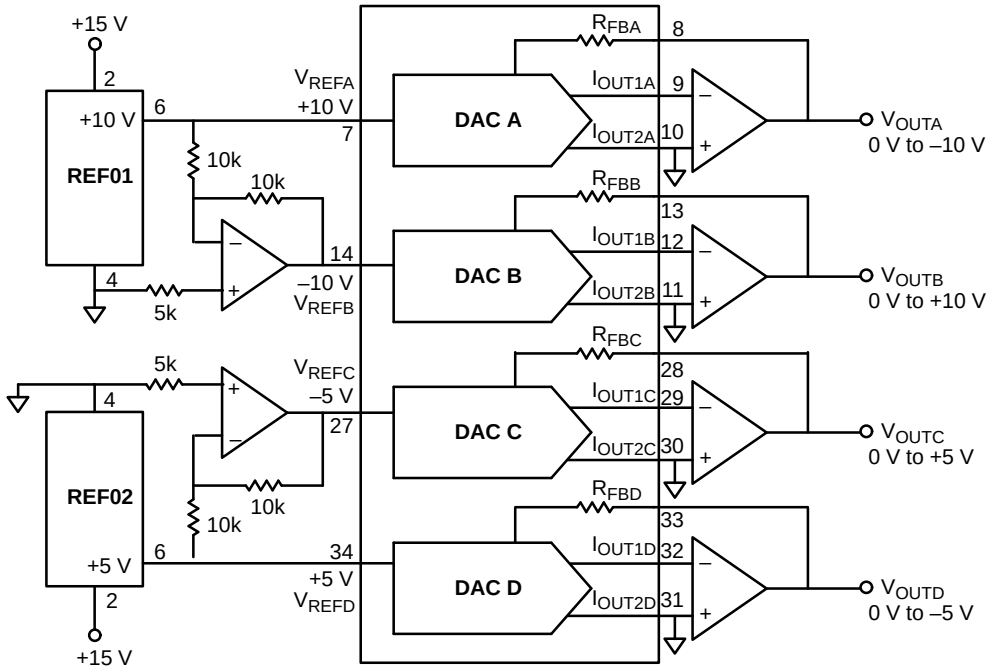


Figure 8. Digitally Programmable Quad Voltage Output ±10 V, ±5 V

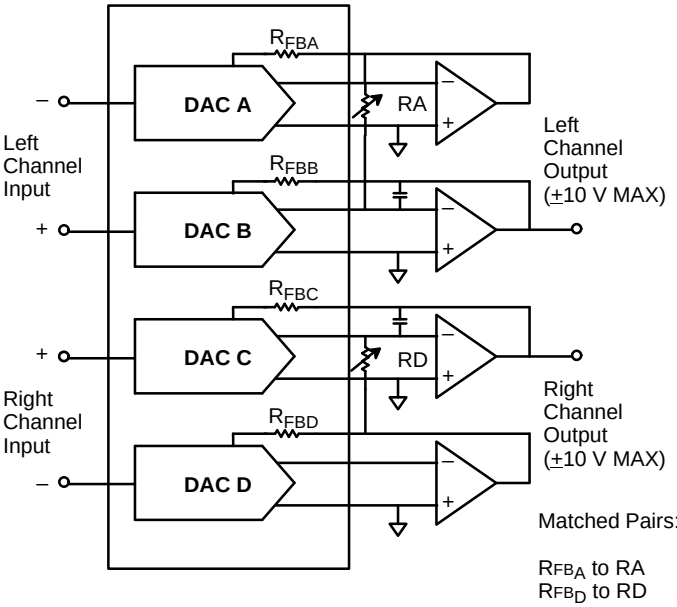


Figure 9. "Clickless" Audio Attenuator/Amplifier

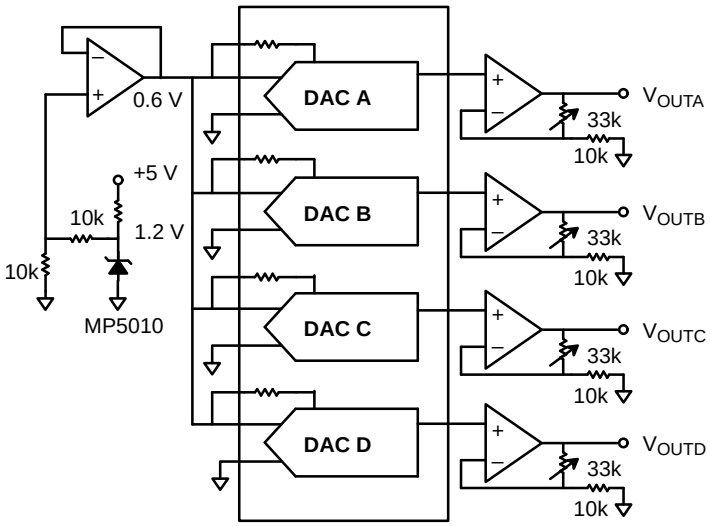
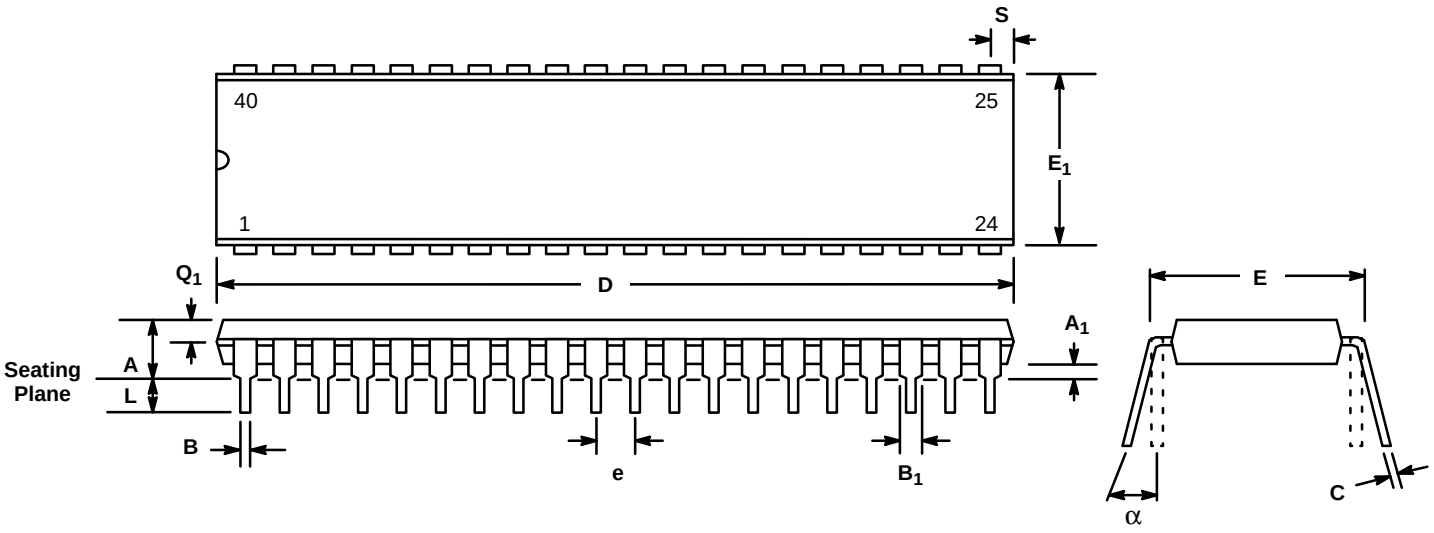


Figure 10. Quad DAC for Single +5 V Supply

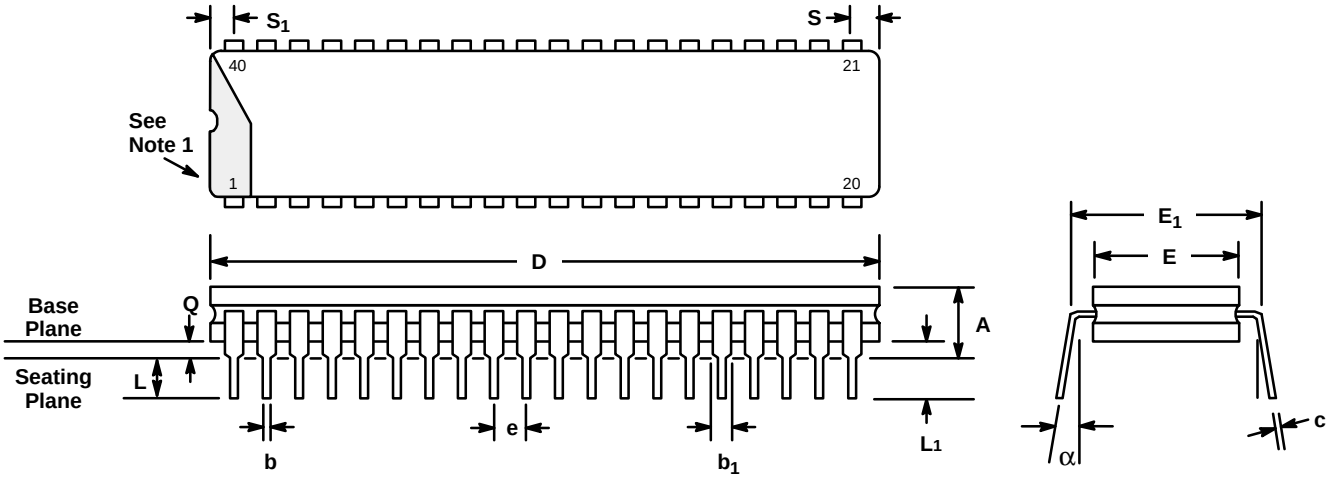
40 LEAD PLASTIC DUAL-IN-LINE
(600 MIL PDIP)
N40



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.225	—	5.72
A_1	0.015	—	0.381	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.980	2.095	50.3	53.2
E	0.585	0.625	14.86	15.88
E_1	0.510	0.620	12.95	15.75
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.020	0.098	0.508	2.49

Note: (1) The minimum limit for dimensions B1 may be 0.023” (0.58 mm) for all four corner leads only.

40 LEAD CERAMIC DUAL-IN-LINE
(600 MIL CDIP)
D40

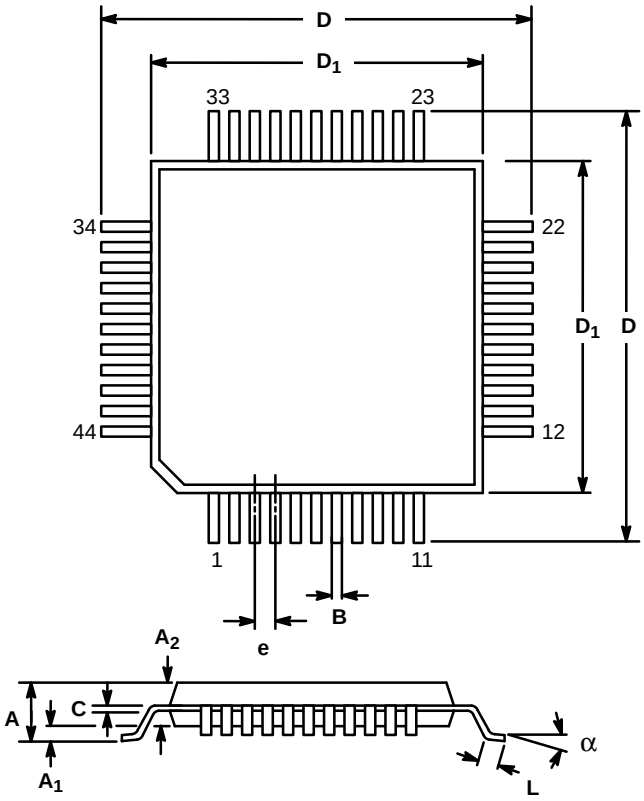


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.225	—	5.72	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	2.096	—	53.24	4
E	0.510	0.620	12.95	15.75	4
E_1	0.590	0.630	14.99	16.00	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.070	0.381	1.78	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

44 LEAD PLASTIC QUAD FLAT PACK
(14mm x 14mm PQFP, METRIC)
Q44



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	3.15	—	0.124
A_1	0.25	—	0.01	—
A_2	2.6	2.8	0.102	0.110
B	0.3	0.4	0.012	0.016
C	0.13	0.23	0.005	0.009
D	16.95	17.45	0.667	0.687
D_1	13.9	14.1	0.547	0.555
e	1.00 BSC		0.039 BSC	
L	0.65	1.03	0.026	0.040
α	0°	7°	0°	7°
Coplanarity = 4 mil max.				

Notes

Notes

Notes

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