



MP7670

8-Channel, Voltage Output,
5 MHz, 4 Quadrant Multiplying
8-Bit D/A Converter with
Serial Digital Data Port

FEATURES

- 8 Independent 4-Quadrant Multiplying 8-Bit DACs
- High Speed:
 - Settling Time: 2.5 μ s to ± 1 LSB (typ)
 - Slew Rate: 5 V/ μ s (typ)
 - Voltage Reference Input Bandwidth: 5 MHz ($V_{IN} = 100$ mV p-p)
- Low Power: 80 mW (typ)
- DACs Matched to $\pm 0.5\%$ (typ)
- Power on Preset to Zero Volts for All Outputs
- Midscale Preset, all DAC Outputs are Zero Volts
- Latch-Up Free
- Greater than 2000 V ESD Protection

APPLICATIONS

- Analog Multiplier Replacement
- High-Frequency Gain Control using DACs
- Convergence Adjustment for Displays and Monitors

GENERAL DESCRIPTION

The MP7670 is an 8-channel, 4 quadrant multiplying, 8-bit accurate digital-to-analog converter with a 5 MHz input bandwidth. It includes an output drive amplifier per channel capable of driving a ± 7 mA to a load. DNL of ± 0.25 LSB is achieved with a channel-to-channel matching of better than 0.5% (typ). Stability, matching, and precision of the DACs are achieved by using MPS' thin film technology.

The MP7670 is ideal for direct gain control of high frequency analog signals. The bipolar output amplifier has low noise which

produces a very sharp signal output particularly in display and monitor applications.

A proprietary subranging architecture provides wide signal bandwidth from V_{IN} to output up to 5 MHz (typ), fast output settling time, and V_{IN} feedthrough isolation of -60 dB (typ).

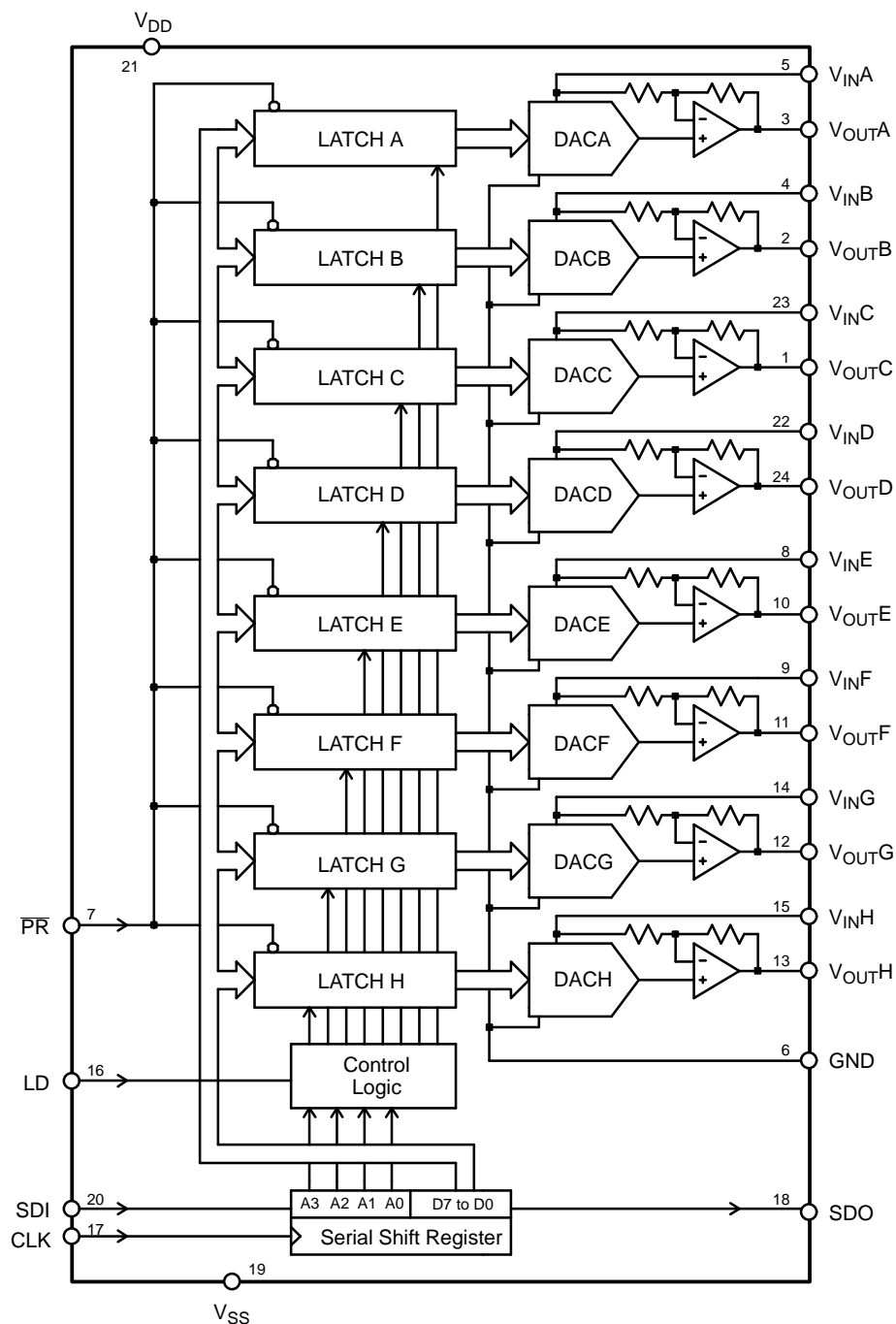
The MP7670 has a serial data 3-wire standard μ -processor logic interface to reduce pin count, package size, and board wire (space).

The MP7670 is fabricated on a junction isolated, high speed BiCMOS1TM process with thin film resistors.

ORDERING INFORMATION

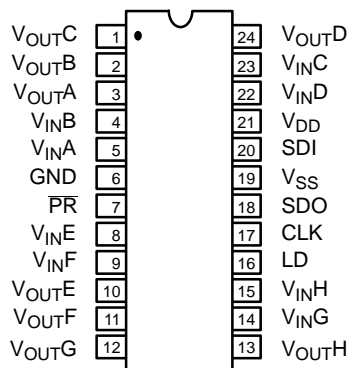
| Package Type | Temperature Range | Part No. |
|--------------|--------------------------------|----------|
| Plastic Dip | -40 to $+85^{\circ}\text{C}$ | MP7670AN |
| SOIC | -40 to $+85^{\circ}\text{C}$ | MP7670AS |

SIMPLIFIED BLOCK DIAGRAM

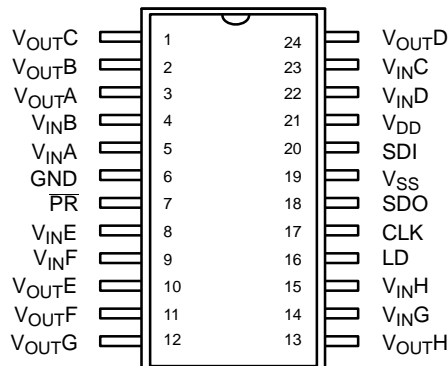


PIN CONFIGURATIONS

See Packaging Section for
Package Dimensions



**24 Pin PDIP (0.300")
NN24**



**24 Pin SOIC (Jedec, 0.300")
S24**

PIN OUT DEFINITIONS

| PIN NO. | NAME | DESCRIPTION |
|---------|-------------------|--------------------------|
| 1 | V _{OUTC} | DAC C Output |
| 2 | V _{OUTB} | DAC B Output |
| 3 | V _{OUTA} | DAC A Output |
| 4 | V _{INB} | DAC B Reference Input |
| 5 | V _{INA} | DAC A Reference Input |
| 6 | GND | Ground |
| 7 | PR | Preset Input, Active Low |
| 8 | V _{INE} | DAC E Reference Input |
| 9 | V _{INF} | DAC F Reference Input |
| 10 | V _{OUTE} | DAC E Output |
| 11 | V _{OUTF} | DAC F Output |
| 12 | V _{OUTG} | DAC G Output |

| PIN NO. | NAME | DESCRIPTION |
|---------|-------------------|---|
| 13 | V _{OUTH} | DAC H Output |
| 14 | V _{ING} | DAC G Reference Input |
| 15 | V _{INH} | DAC H Reference Input |
| 16 | LD | Load DAC Register Strobe, Active High Input |
| 17 | CLK | Serial Clock Input |
| 18 | SDO | Serial Data Output |
| 19 | V _{SS} | Negative Power Supply |
| 20 | SDI | Seral Data Input |
| 21 | V _{DD} | Positive Power Supply |
| 22 | V _{IND} | DAC D Reference Input |
| 23 | V _{INC} | DAC C Reference Input |
| 24 | V _{OUTD} | DAC D Output |

ELECTRICAL CHARACTERISTICS TABLE FOR DUAL SUPPLIES

Unless Otherwise Noted: $V_{DD} = 5\text{ V}$, $V_{SS} = -5\text{ V}$, $GND = 0\text{ V}$, $V_{INX} = 3\text{ V}$

| Parameter | Symbol | Min | 25°C Typ | Max | Units | Test Conditions/Comments |
|--|-----------|-----|-------------|---------|--------------------------------|--|
| DC CHARACTERISTICS | | | | | | |
| Resolution (All Grades) | N | 8 | | | Bits | |
| Differential Non-Linearity | DNL | | $\pm 1/4$ | ± 1 | LSB | |
| Integral Non-Linearity | INL | | | ± 1 | LSB | |
| Monotonicity | | | Guaranteed | | | |
| Gain Error | GE | | $\pm 1/2$ | | LSB | |
| DAC OUTPUT | | | | | | |
| Output Offset | V_{BZE} | | 3 | 25 | mV | $\overline{PR} = 0$, Sets Code = 80 _H |
| Voltage Range | OVR | -3 | | 3 | V | |
| Output Current | I_{OUT} | | ± 10 | | mA | $\Delta V_{OUT} < 1\text{ LSB}$ |
| Capacitive Load | CL | | | 200 | pF | No oscillations |
| REFERENCE INPUTS | | | | | | |
| Input Resistance of one DAC | R_{IN} | 5 | | | K Ω | R_{IN} (typ) = 15K Ω /R _x R _x = 20K Ω /(1-Code/256) |
| Input Capacitance ² | C_{IN} | | 15 | 25 | pF | |
| Voltage Range ¹ | IVR | -3 | | 3 | V | |
| DYNAMIC CHARACTERISTICS² | | | | | | |
| Input to Output Bandwidth Small Signal | BWS | 2 | 5 | | MHz | Code = FS, $V_{INX} = 100\text{ mVp-p}$ |
| Input to Output Bandwidth Large Signal | BWL | | 3 | | MHz | Code = FS, $V_{INX} = 1\text{ Vp-p}$ |
| Slew Rate | SR | | 5 | | V/ μ s | Measured 10% to 90%, $\Delta V_{OUTX} = \pm 6\text{ V}$ |
| V_{IN} Feedthrough | F_{DT} | | -60 | | dB | Code = HS, up to $f = 100\text{ kHz}$ |
| Total Harmonic Distortion | T_{HD} | | 0.02 | | % | $V_{INX} = 4\text{ V p-p}$, Code = FS $f = 1\text{ kHz}$, $f_{LP} = 80\text{ kHz}$ |
| Spot Noise Voltage | e_N | | 0.17 | | $\mu\text{V}/\sqrt{\text{Hz}}$ | $f = 1\text{ kHz}$ |
| Output Settling Time | t_S | | 2.5 | 5.0 | μ s | $\pm 1\text{ LSB}$, Code = 0 to FS |
| Channel-to-Channel Crosstalk | C_T | 60 | | | dB | Measured between adjacent channels, $f = 100\text{ kHz}$ |
| Digital Feedthrough | Q | | 6 | | nVs | $V_{INX} = 0\text{ V}$, Code = 0 to FS |
| DIGITAL INPUTS | | | | | | |
| Logic High ³ | V_{IH} | 2.4 | | | V | |
| Logic Low ³ | V_{IL} | | | 0.8 | V | |
| Input Current | I_L | | | ± 1 | μ A | |
| Input Capacitance ² | C_L | | | 8 | pF | |
| DIGITAL OUTPUTS | | | | | | |
| Logic High | V_{OH} | 3.5 | | | V | $I_{OH} = -0.4\text{ mA}$ |
| Logic Low | V_{OL} | | | 0.4 | V | $I_{OL} = 1.6\text{ mA}$ |

ELECTRICAL CHARACTERISTICS TABLE

| Description | Symbol | Min | 25°C Typ | Max | Units | Conditions |
|---|-----------------------------------|------|-------------|------|-------|----------------------------------|
| POWER SUPPLIES | | | | | | |
| Power Supply Range | V _{DD} | 4.5 | | 5.5 | V | |
| | V _{SS} | −5.5 | | −4.5 | V | |
| Power Supply Rejection Ratio | | | | | | |
| Positive | PSRR+ | | 0.0002 | 0.01 | %/% | PR = 0 V, ΔV _{DD} = ±5% |
| Negative | PSRR− | | 0.0002 | 0.01 | %/% | PR = 0 V, ΔV _{SS} = ±5% |
| Power Dissipation | P _{DISS} | | 80 | 130 | mW | PR = 0 V |
| Power Supply Current | I _{DD} | | 8 | 13 | mA | PR = 0 V |
| Negative Supply Current | I _{SS} | | 8 | 13 | mA | PR = 0 V |
| DIGITAL TIMING SPECIFICATIONS ^{2, 4} | | | | | | |
| Input Clock Pulse Width | t _{CH} , t _{CL} | 80 | | | ns | |
| Data Setup Time | t _{DS} | 40 | | | ns | |
| Data Hold Time | t _{DH} | 20 | | | ns | |
| CLK to SDO Propagation Delay | t _{PD} | | | 120 | ns | |
| Load Pulse Width | t _{LD} | 70 | | | ns | |
| Preset Pulse Width | t _{PR} | 50 | | | ns | |
| Clock Edge to Load | t _{CKLD} | 30 | | | ns | |
| Load Edge to Next Clk Edge | t _{LDCK} | 60 | | | ns | |

NOTES

- ¹ Maximum input voltage is 2 V less than V_{DD} .
- ² Guaranteed but not production tested.
- ³ Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
- ⁴ See timing diagram.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)^{1, 2}

| | | | |
|---------------------------------------|-------------------------|---|-----------------|
| V_{DD} to GND | +6.5 V | Maximum Junction Temperature | -65°C to +150°C |
| V_{SS} to GND | -6.5 V | Storage Temperature | 150°C |
| V_{INA-H} to GND | V_{DD} to V_{SS} | Lead Temperature (Soldering 10 seconds) | +300°C |
| V_{OUTA-H} to GND | V_{DD} to V_{SS} | Package Power Dissipation Rating @ 75°C | |
| Digital Input & Output Voltage to GND | -0.5 to V_{DD} +0.5 V | PDIP, SOIC | 1000mW |
| Operating Temperature Range | | Derates above 75°C | 14mW/°C |
| Extended Industrial | -40°C to +85°C | | |

NOTES:

- ¹ Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- ² Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100μs.

THEORY OF OPERATION

The MP7670 contains 8 independent 4-quadrant multiplying D/A converters with output amplifiers. The design has incorporated a novel approach that provides fast, accurate, low noise, low distortion, small size, and low power in the same device. This device is particularly useful in applications where multipliers are used to perform the gain adjustment function for high frequency analog signal conditioning. Also note that typical multipliers tend to increase noise particularly for low gain settings and have high offsets. The MP7670 design delivers a very low, constant noise, and low offset with digital control through the entire gain ranges of the D/A converter.

Linearity Characteristics

Each D/A converter in the MP7670 achieves $DNL \leq \pm 0.25$ LSB (typ), and gain error $\leq \pm 0.2\%$ (typ). Since all 8 channels of MP7670 are fabricated in the same IC, the linearity, gain matching, and input-output characteristics of all 8 channels match extremely well.

The Logic Interface and Serial Port

The MP7670 is equipped with a serial data 3-wire standard μ -processor logic interface to reduce pin count, package size, and board wire (small size). This interface consists of LD which controls the transfer of data to the selected DAC channels that are fed through the SDI (serial digital data and address bits) with

the CLK (digital input shift register clock). Please refer to the following timing diagrams and truth tables for logic details.

A SDO (serial digital data output driver) is connected to the other side of the input shift register and would save SDI bus space by allowing the daisy chaining of several MP7670s (connecting SDI of device 2 to SDO of device 1).

When the LD signal is low, CLK signal loads the digital input bits (SDI) into the 12-bit shift register. The LD signal going high loads this data into the selected DACs. Also, when the \overline{PR} signal is low, the output of all DACs would be reset to 0 volts.

Power Supplies and Input Voltage Ranges

The MP7670 is capable of functioning with $\pm 5V$ and $\pm 3V$ supplies. The output and input DC ranges are limited to within $\pm 2V$ from each positive and negative supplies. For example, with supplies at $\pm 5V$, the recommended output range is $\pm 3V$.

The MP7670 design eliminates any code dependent current change into its GND, hence easing the board level design by eliminating the stringent need for other types of DACs for low GND impedance wiring considerations at board level.

Each output of the MP7670 DAC has an output amplifier driver delivering less than 0.05Ω of output impedance through a push-pull linear output stage. Each output and input characteristics parameter match extremely well, given that all channels are fabricated in the same IC.

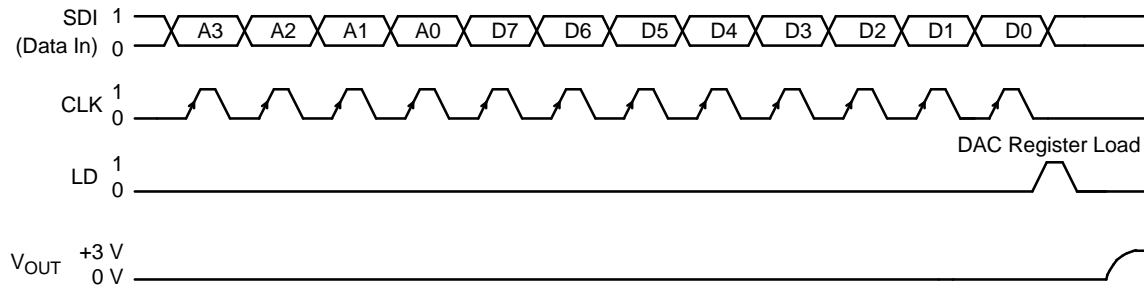


Figure 1. Serial Data Timing and Loading

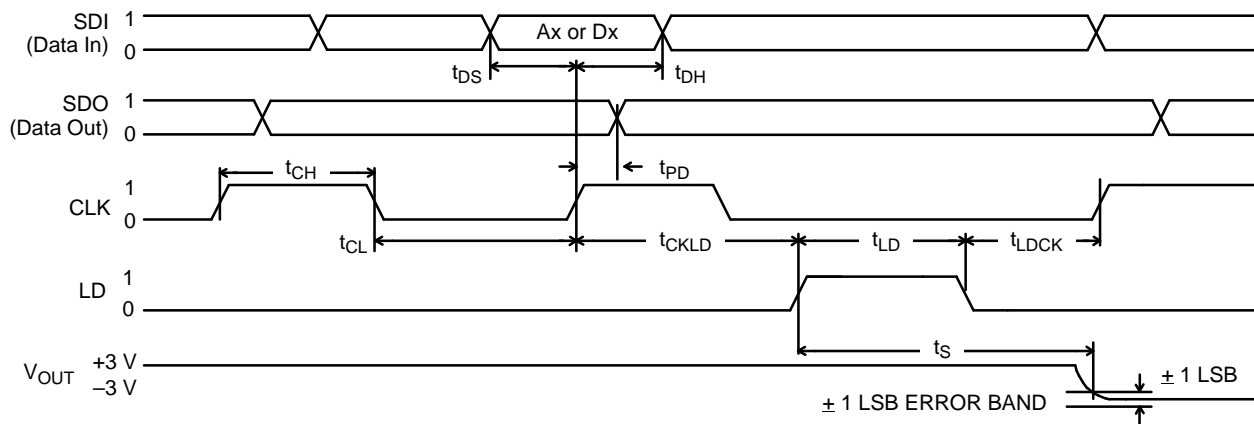


Figure 2. Detail Serial Data Input Timing (PR = "1")

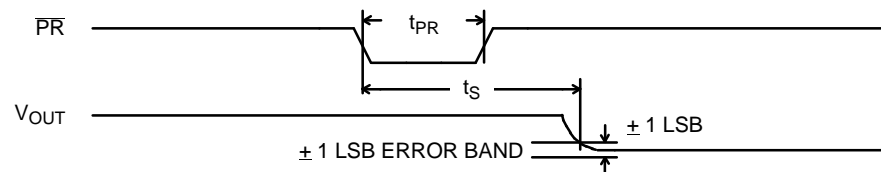


Figure 3. PRESET Timing

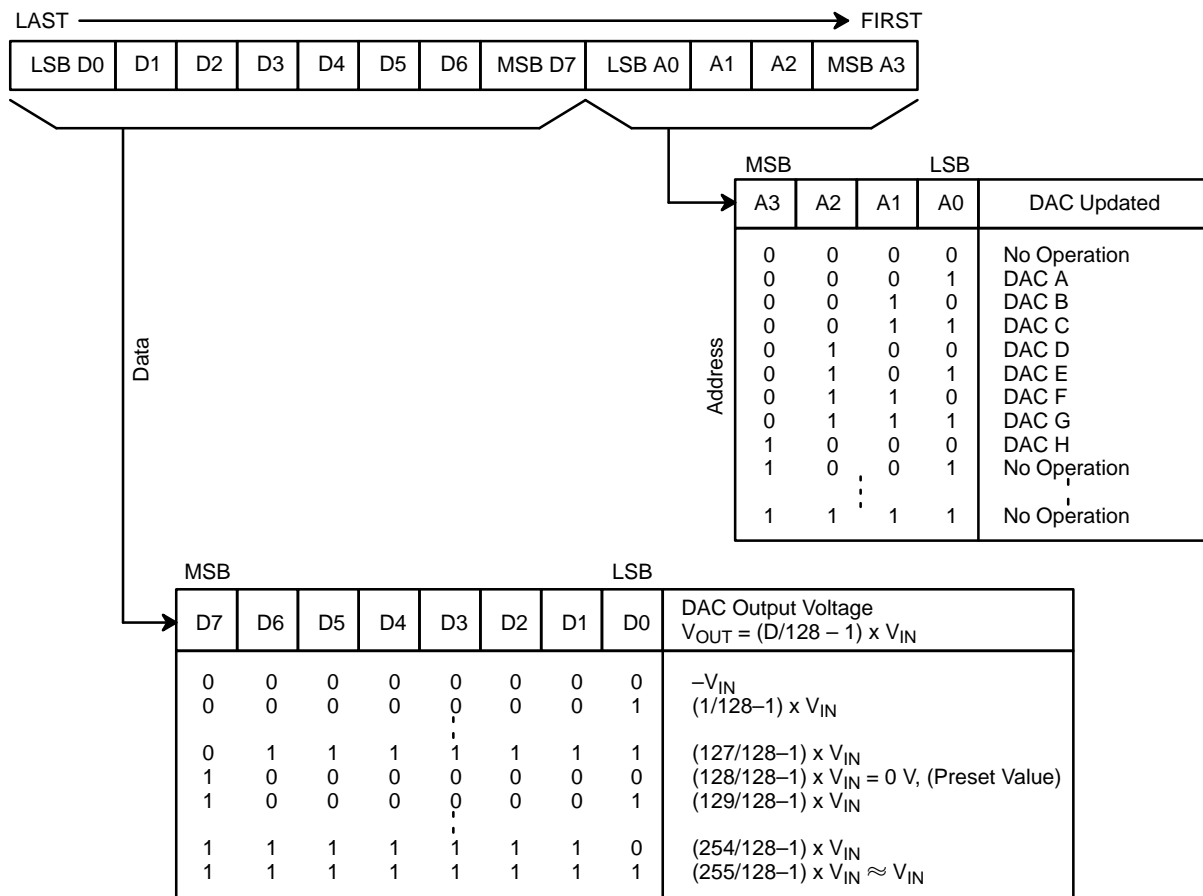


Table 1. Serial Input Format

| SDI | CLK | LD | \overline{PR} | Input Shift Register Operation |
|-----|------------|----|-----------------|---|
| X | L | L | H | No Operation |
| X | \uparrow | L | H | Shift One Bit In from SDI (Pin 20), Shift One Bit* Out from SDO (Pin 18) |
| X | X | L | L | All DAC Registers = 80 _H |
| X | L | H | H | Load Serial Register Data into DAC(X) Register |

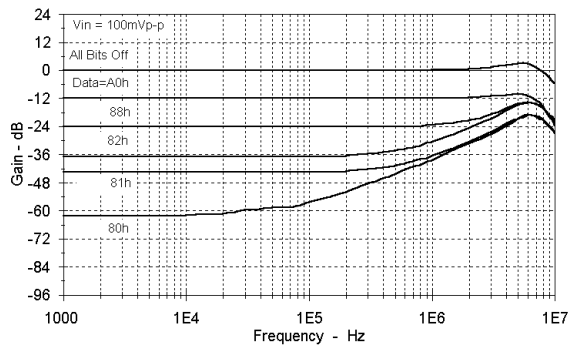
*Data shifted into the SDI pin appears twelve clocks later at the SDO pin.

Table 2. Control Logic Truth Table

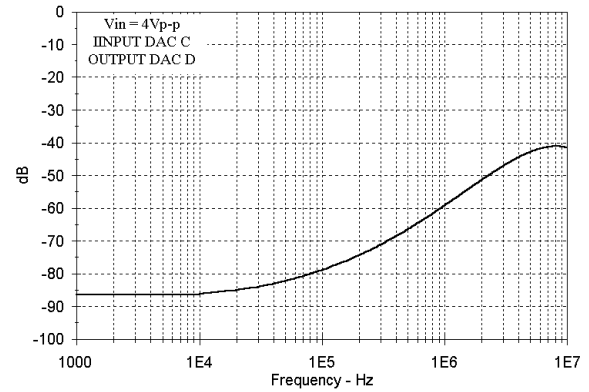
| Decimal Input (D) | V_{OUT} (D) | Comments ($V_{IN} = 3 \text{ V}$) |
|-------------------|---------------|-------------------------------------|
| 0 | -3.00 V | Inverted FS |
| 1 | -2.98 | |
| 127 | -0.02 | |
| 128 | 0.00 | Zero Output |
| 129 | 0.02 | |
| 254 | 2.95 | Full Scale (FS) |
| 255 | 2.98 | |

Table 3. DAC Transfer Function

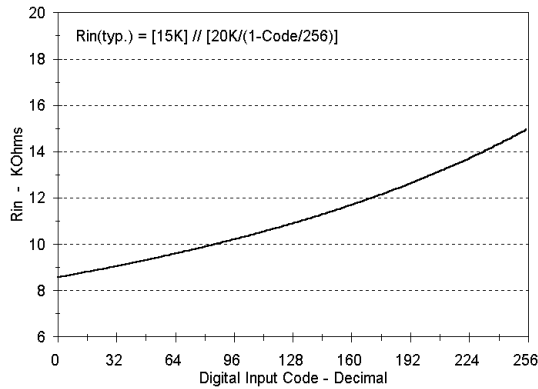
PERFORMANCE CHARACTERISTICS



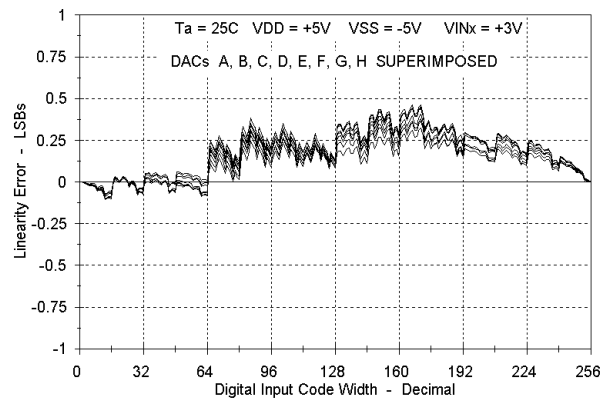
Graph 1. Gain (V_{OUT}/V_{IN}) and Feedthrough vs. Frequency



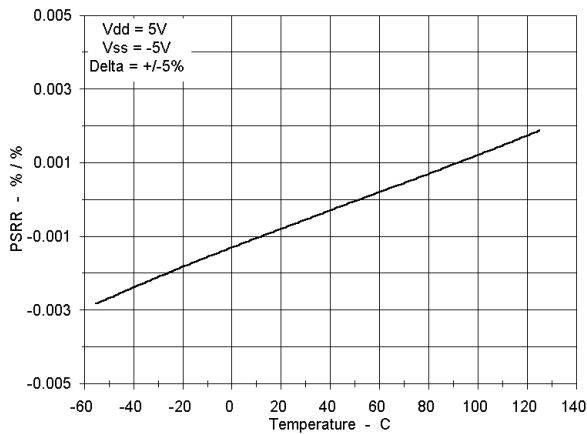
Graph 2. DAC Crosstalk vs. Frequency



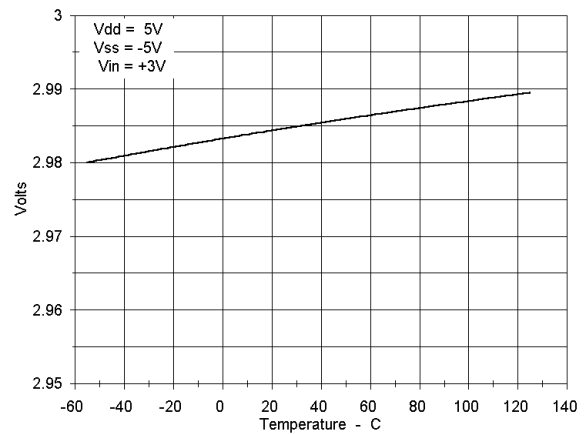
Graph 3. DAC Input Resistance vs. Digital Input Code



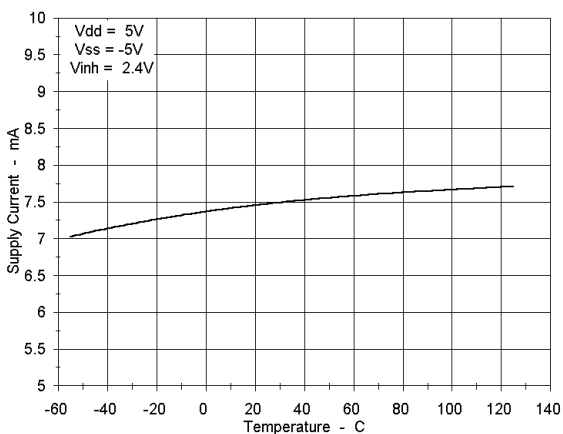
Graph 4. Linearity Error vs. Digital Input Code



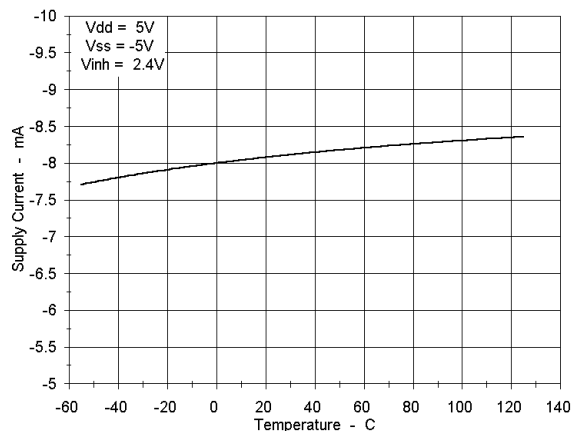
Graph 5. PSRR (DC) vs. Temperature



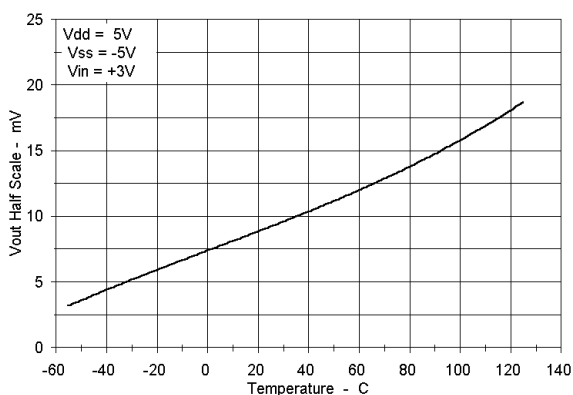
Graph 6. V_{OUT} Full Scale vs. Temperature



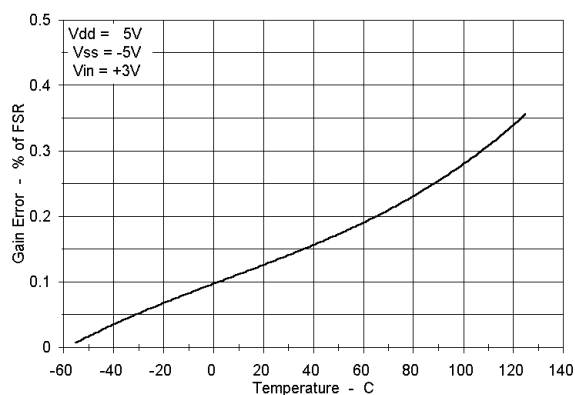
Graph 7. Supply Current (I_{DD}) vs. Temperature



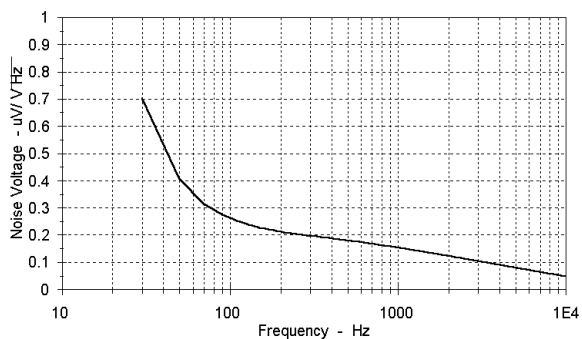
Graph 8. Supply Current (I_{SS}) vs. Temperature



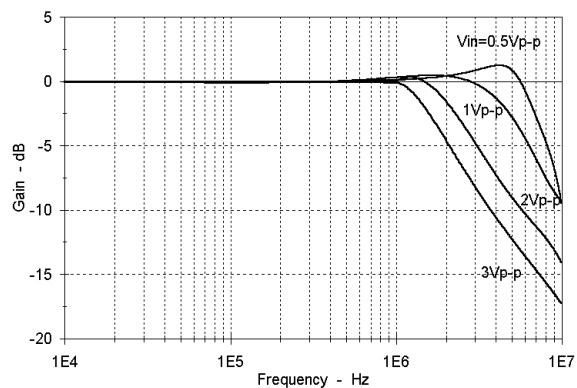
Graph 9. V_{OUT} Offset Error vs. Temperature



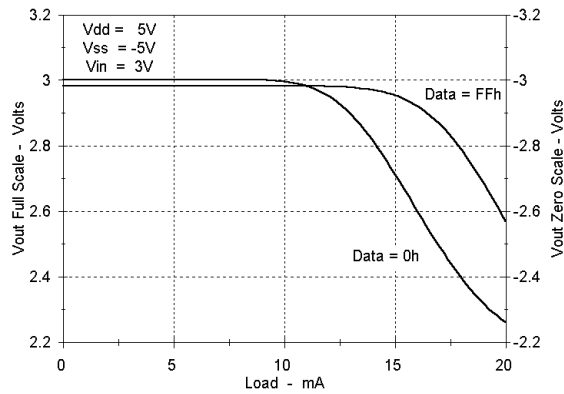
Graph 10. Gain Error vs. Temperature



Graph 11. Voltage Noise Density vs. Frequency



Graph 12. Varying Reference Input DAC Gain vs. Frequency

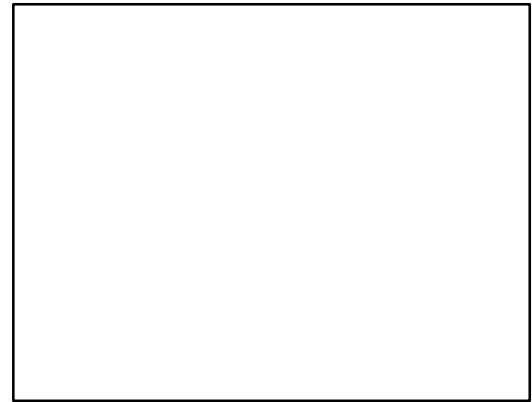


Graph 13. V_{OUT} Output Drive Capability

V_{IN}
(2 V/Div)

Digital Code=
All ones

V_{OUT}
(2 V/Div)



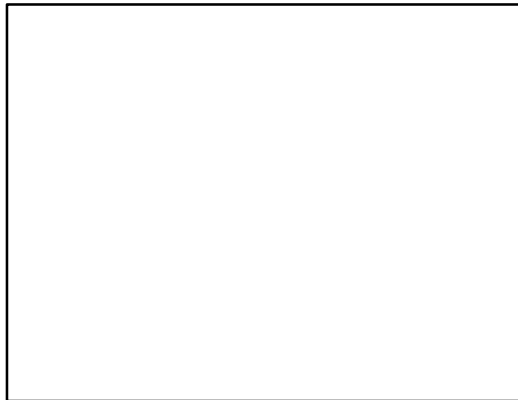
1 μ s/Div

Graph 14. Pulse Response

LD
(5 V/Div)

Digital Code=
128 \rightarrow 127

V_{OUT}
(200 mV/Div)



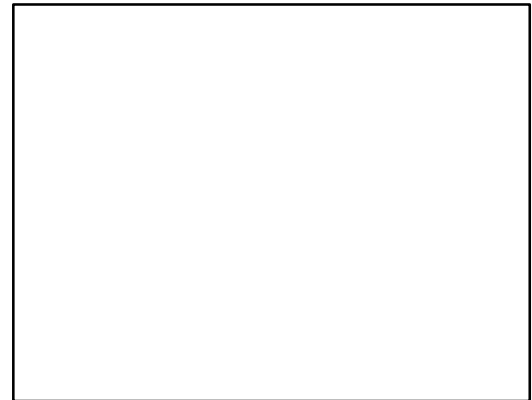
1 μ s/Div

Graph 15. 1 LSB Digital Step Change

LD
(5 V/Div)

Digital Code=
255 \rightarrow 0 \rightarrow 255

V_{OUT}
(2 V/Div)



5 μ s/Div

Graph 16. Settling Time

V_{IN}
(2 V/Div)

V_{OUT}
(2 V/Div)



2 μ s/Div

Graph 17. 128kHz Sawtooth Waveform Response

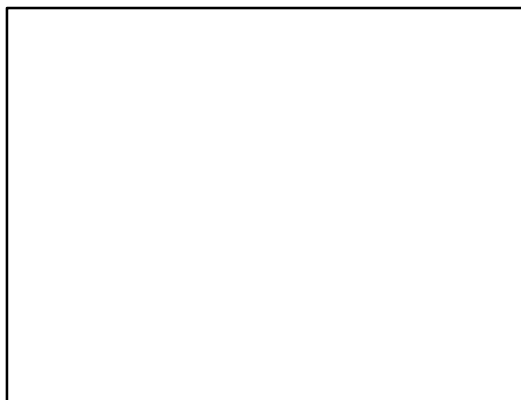
V_{OUT}
(10 mV/Div)



1 μ s/Div

Graph 18. Clock Feedthrough

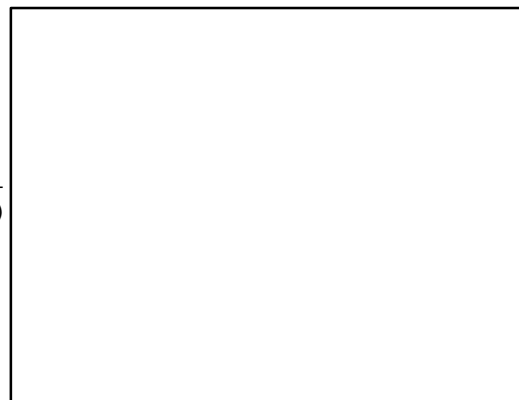
V_{OUT}
(20 mV/Div)



50 ns/Div

Graph 19. Digital Crosstalk

V_{OUT}
(5 dB/Div)



kHz

Graph 20. PSRR vs. Frequency

Gain
(5 dB/Div)

Phase
20°/Div



MHz

Graph 21. Gain & Phase vs. Frequency

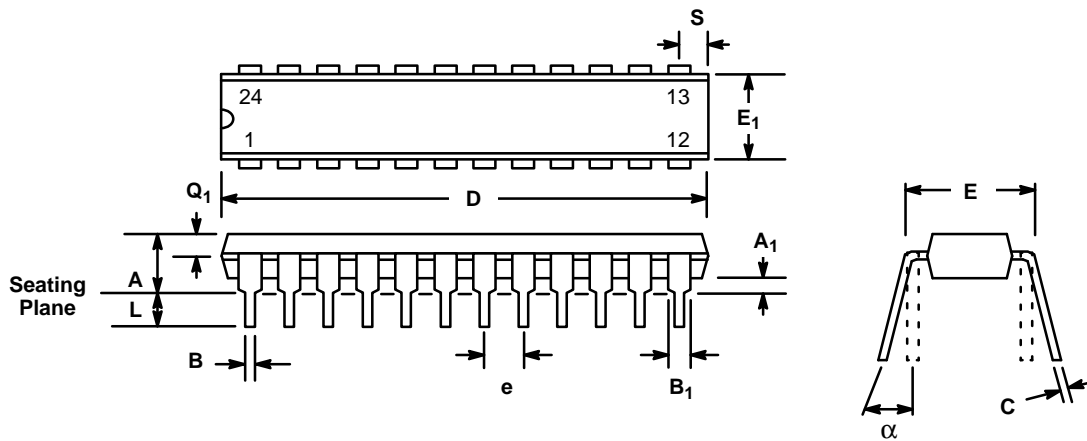
V_{OUT}
(20 mV/Div)



50 ns/Div

Graph 22. Digital Feedthrough

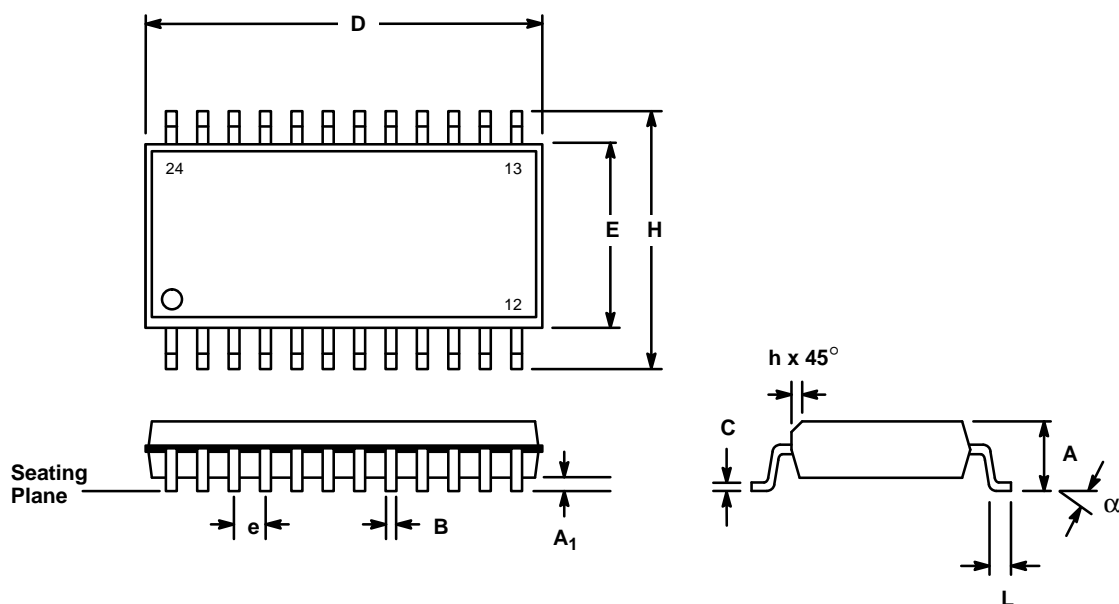
**24 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
NN24**



| SYMBOL | INCHES | | MILLIMETERS | |
|--------------------|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | — | 0.200 | — | 5.08 |
| A ₁ | 0.015 | — | 0.38 | — |
| B | 0.014 | 0.023 | 0.356 | 0.584 |
| B ₁ (1) | 0.038 | 0.065 | 0.965 | 1.65 |
| C | 0.008 | 0.015 | 0.203 | 0.381 |
| D | 1.16 | 1.280 | 29.46 | 32.51 |
| E | 0.295 | 0.325 | 7.49 | 8.26 |
| E ₁ | 0.220 | 0.310 | 5.59 | 7.87 |
| e | 0.100 BSC | | 2.54 BSC | |
| L | 0.115 | 0.150 | 2.92 | 3.81 |
| α | 0° | 15° | 0° | 15° |
| Q ₁ | 0.055 | 0.070 | 1.40 | 1.78 |
| S | 0.028 | 0.098 | 0.711 | 2.49 |

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

24 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC) S24



| SYMBOL | INCHES | | MILLIMETERS | |
|--------|-----------|--------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.097 | 0.104 | 2.464 | 2.642 |
| A1 | 0.0050 | 0.0115 | 0.127 | 0.292 |
| B | 0.014 | 0.019 | 0.356 | 0.483 |
| C | 0.0091 | 0.0125 | 0.231 | 0.318 |
| D | 0.602 | 0.612 | 15.29 | 15.54 |
| E | 0.292 | 0.299 | 7.42 | 7.59 |
| e | 0.050 BSC | | 1.27 BSC | |
| H | 0.400 | 0.410 | 10.16 | 10.41 |
| h | 0.010 | 0.016 | 0.254 | 0.406 |
| L | 0.016 | 0.035 | 0.406 | 0.889 |
| α | 0° | 8° | 0° | 8° |

Notes

NOTICE

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