MP7645B

CMOS
Buffered Multiplying 12-Bit
Digital-to-Analog Converter

FEATURES

- **Greater than 2000 V ESD Protection**
- **Differential Linearity ±1/2 LSB Tmin to Tmax**
- **Microprocessor Compatible**
- **Low Glitch Energy**
- **Gain Error Tempco (2 ppm/°C max)**
- **Low Sensitivity to Amplifier Offset**
- **Four Quadrant Multiplication**
- **Latch-Up Free**
- **TTL/5 V CMOS Compatible**
- **Guaranteed Monotonic**

GENERAL DESCRIPTION

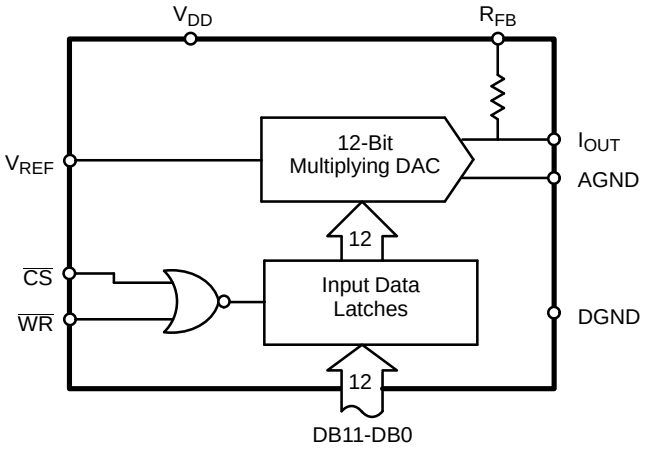
The MP7645B is an improved precision, monolithic 12-bit CMOS 4-quadrant multiplying DAC with an on-board data latch. The latch is loaded by a single 12-bit wide word. Data is loaded into the input latch under the control of $\overline{CS}$ and $\overline{WR}$ inputs. These control inputs are level triggered; tying these inputs low makes the input latch transparent allowing direct unbuffered operation of the DAC.

– Stability – The MP7645B incorporates a unique decoding technique yielding excellent accuracy and stability over temperature. Monotonicity is guaranteed over the entire temperature range including the industrial and military ranges. The gain error specification of 2 ppm/°C over a 100°C temperature range equals 0.8 LSB of error.

– Digital Feedthrough – The MP7645B has 5 to 8 times less digital feedthrough than similar buffered DACs.

– Low Sensitivity to Output Amplifier Offset – The additional linearity error incurred by amplifier offset is reduced by a factor of at least 3 in the MP7645B over conventional DACs. High latch-up resistance and high ESD protection make this a rugged, reliable attenuator!

SIMPLIFIED BLOCK DIAGRAM

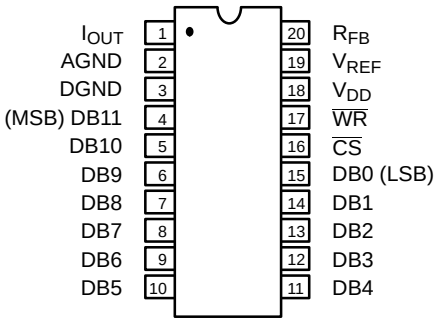


ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP7645BKN	±1	±1	±0.2
Plastic Dip	–40 to +85°C	MP7645BLN	±1/2	±1/2	±0.2
Ceramic Dip	–40 to +85°C	MP7645BBD	±1	±1	±0.2
Ceramic Dip	–40 to +85°C	MP7645BCD	±1/2	±1/2	±0.2

PIN CONFIGURATION

See Packaging Section for Package Dimensions



20 Pin CDIP, PDIP (0.300")
D20, N20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I_{OUT}	Current Output Port
2	AGND	Analog Ground
3	DGND	Digital Ground
4	DB11	Data Input Bit 11 (MSB)
5	DB10	Data Input Bit 10
6	DB9	Data Input Bit 9
7	DB8	Data Input Bit 8
8	DB7	Data Input Bit 7
9	DB6	Data Input Bit 6
10	DB5	Data Input Bit 5

PIN NO.	NAME	DESCRIPTION
11	DB4	Data Input Bit 4
12	DB3	Data Input Bit 3
13	DB2	Data Input Bit 2
14	DB1	Data Input Bit 1
15	DB0	Data Input Bit 0 (LSB)
16	$\overline{CS}$	Chip Select Input (Active Low)
17	$\overline{WR}$	Write Input (Active Low)
18	V_{DD}	Positive Voltage Power Supply
19	V_{REF}	Reference Voltage Input
20	R_{FB}	Feedback Resistor Input

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity
K, B				±1		±1		
L, C				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	
K, B				±1		±1		
L, C				±1/2		±1/2		
Gain Error	GE						% FSR	Using Internal R_{FB}
K, B				±0.2		±0.2		
L, C				±0.2		±0.2		
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Monotonicity			Guaranteed		Guaranteed			
K, L								12-Bit Monotonic Tmin to Tmax
Power Supply Rejection Ratio	PSRR			±50		±50	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}						nA	
K, L, B, C				±10		±200		
DYNAMIC PERFORMANCE[2]								
Current Settling Time	t_S		1			2 typ	µs	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT}	F_T		5			5	mV p-p	V_{REF} = 10kHz, 20 Vp-p, sinewave
Propagation Delay	t_{PD}		50				ns	From digital input change to 90% of final value
REFERENCE INPUT								
Input Resistance	R_{IN}	7	11	25	7	25	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	3			3.0		V	
Logical "0" Voltage	V_{IL}			+0.8		+0.8	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	
Input Capacitance[2]								
Data	C_{IN}			5		5	pF	DB0-DB11
Control	C_{IN}			20		20	pF	$\overline{WR}$, $\overline{CS}$
ANALOG OUTPUTS								
Output Capacitance[2]								
	C_{OUT}		50				pF	DAC Inputs all 0's
	C_{OUT}		100				pF	DAC Inputs all 1's

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLY								
Functional Voltage Range[5]	V_{DD}	5		15	5	15	V	
Supply Current	I_{DD}			1		1	mA	All digital inputs = 0 V or all = 5 V
SWITCHING CHARACTERISTICS[2, 4]								
Chip Select to Write Set-Up Time	t_{CS}	180					ns	
Chip Select to Write Hold Time	t_{CH}	0					ns	
Write Pulse Width	t_{WR}	100					ns	
Data Valid to Write Set-Up Time	t_{DS}	100					ns	
Data Valid to Write Hold Time	t_{DH}	10					ns	

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND . . . . . +17 V
Digital Input Voltage to GND (2) . GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND . . . . . GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND (2) . . . . . ±25 V
V_{RFB} to GND (2) . . . . . ±25 V
AGND to DGND . . . . . ±0.5 V
(Functionality Guaranteed ±0.5 V)

Storage Temperature . . . . . –65°C to +150°C

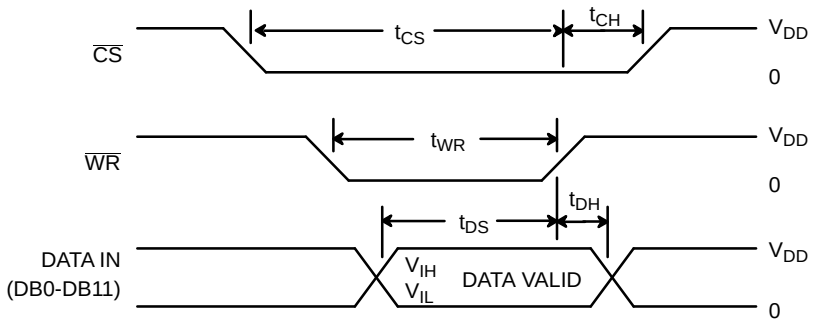
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C

Package Power Dissipation Rating to 75°C
CDIP, PDIP 950mW
Derates above 75°C . . . . . 13mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.
3 GND refers to AGND and DGND.

WRITE CYCLE TIMING DIAGRAM



APPLICATION NOTES

Refer to Section 8 for Applications Information

MICROPROCESSOR INTERFACING OF THE MP7645B

The MP7645B can interface directly to both 8- and 16-bit microprocessors via its 12-bit wide data latch using standard $\overline{CS}$ and $\overline{WR}$ control signals.

A typical interface circuit for an 8-bit processor is shown (*Figure 1.*) This arrangement uses two memory addresses, one for the lower 8 bits of data to the DAC and one for the upper 4 bits of data into the DAC via the latch.

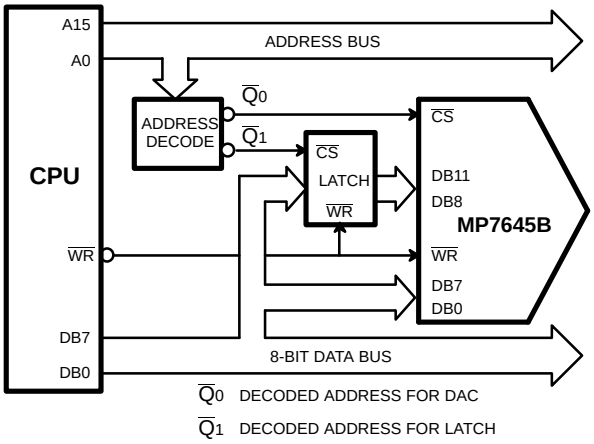


Figure 1. 8-Bit Processor to MP7645B Interface

Figure 2. shows an alternative approach for use with 8-bit processors which have a full 16-bit wide address bus such as 6800, 8080 and Z80. This technique uses the 12 lower address lines of the processor addresses bus to supply data to the DAC, thus each MP7645B connected in this way uses 4k bytes of address locations. Data is written to the DAC using a single memory write instruction. The address field of the instruction is organized so that the lower 12 bits contain the data for the DAC and the upper 4 bits contain the address of the 4k block at which the DAC resides.

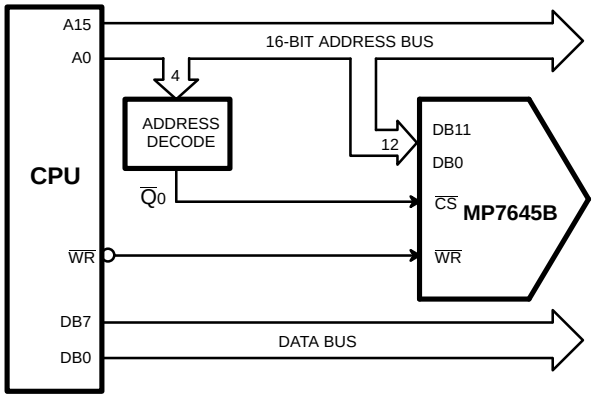
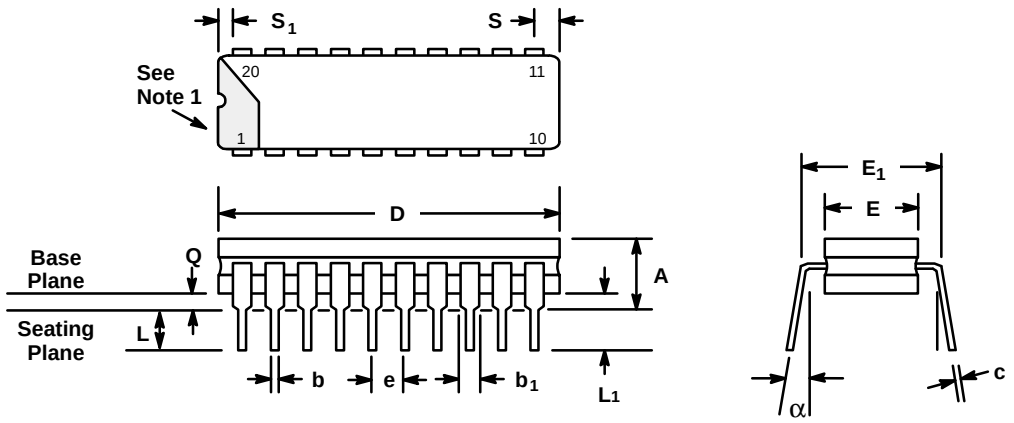


Figure 2. Connecting the MP7645B to 8-Bit Processors via the Address Bus

20 LEAD CERAMIC DUAL-IN-LINE
(300 MIL CDIP)
D20

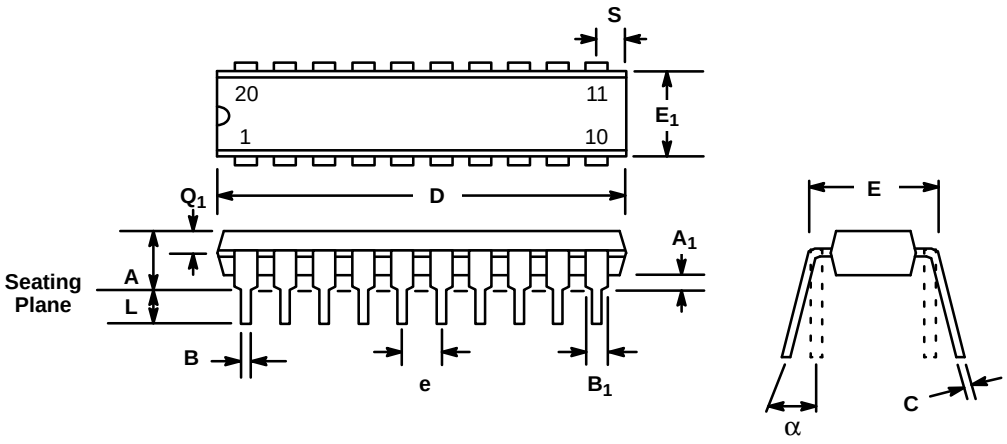


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	1.060	—	26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.070	0.381	1.78	3
S	—	0.080	—	2.03	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

20 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.945	1.060	24.0	26.92
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.080	1.02	2.03

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

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