MP7613

Octal 12-Bit DAC Array™
D/A Converter with Output Amplifier
and Parallel Data/Address µP Control Logic

FEATURES

- Eight Independent Channel 12-Bit DACs with Output Amplifiers
- Low Power 320 mW (typ.)
- Parallel Digital Data and Address Port
- Double Buffered Data Interface
- Readback of DAC Latches
- Zero Volt Output Preset (Data = 10 .. 00)
- 12-Bit Resolution, 11-Bit Accuracy
- Extremely Well Matched DACs
- Extremely Low Analog Ground Current (<60µA/Channel)
- ±10 V Output Swing with ±11.4 V Supplies
- Rugged Construction – Latch-Up Proof
- Serial Version: MP7612

APPLICATIONS

- Data Acquisition Systems
- ATE
- Process Control
- Self-Diagnostic Systems
- Logic Analyzers
- Digital Storage Scopes
- PC Based Controller/DAS

GENERAL DESCRIPTION

The MP7613 provides eight independent 12-bit resolution Digital-to-Analog Converters with voltage output amplifiers and a parallel digital address and data port.

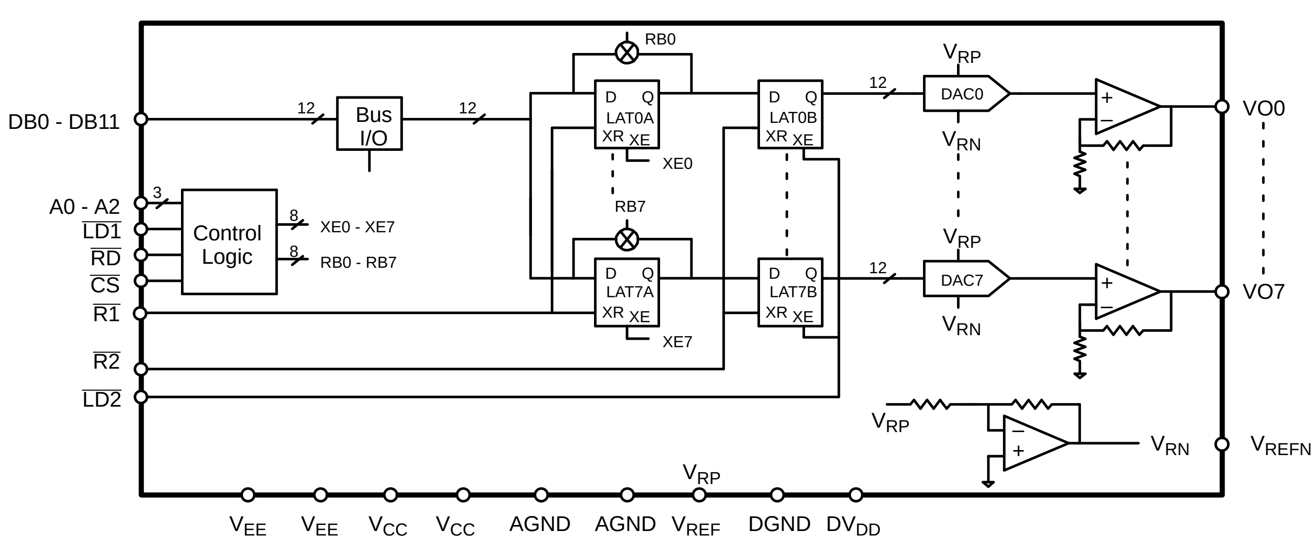
Built on using an advanced linear BiCMOS, these devices offer rugged solutions that are latch-up free, and take advantage of EXAR's patented thin-film resistor process which exhibits excellent long term stability and reliability.

A standard µ-processor and TTL/CMOS compatible 12-bit input data port loads the data into the pre-selected DACS.

This device can easily be interfaced to a data bus, and digital readback of each channel is available.

Typical DAC matching is 0.7 LSB across all codes. Accuracy of ±0.75 LSB for DNL and ±1 LSB for INL is achieved for B grade versions. The output amplifier is capable of sinking and sourcing 5mA, and the output voltage settles to 12-bits in less than 30µs (typ.).

SIMPLIFIED BLOCK DIAGRAM

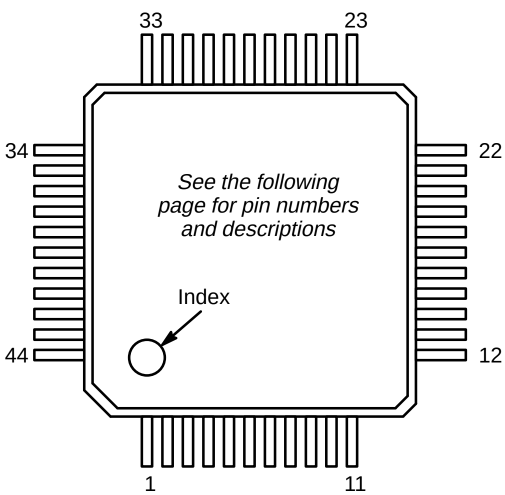


ORDERING INFORMATION

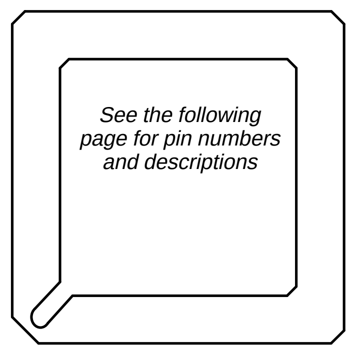
Package Type	Temperature Range	Part No.	Res. (Bits)	INL (LSB)	DNL (LSB)	FSE (LSB)
PQFP	–40 to +85°C	MP7613BE	12	±1	±0.75	±6
PQFP	–40 to +85°C	MP7613AE	12	±2	±1	±8
PGA	–40 to +85°C	MP7613BG	12	±1	±0.75	±6
PGA	–40 to +85°C	MP7613AG	12	±2	±1	±8
PLCC	–40 to +85°C	MP7613BP	12	±1	±0.75	±6
PLCC	–40 to +85°C	MP7613AP	12	±2	±1	±8

PIN CONFIGURATIONS

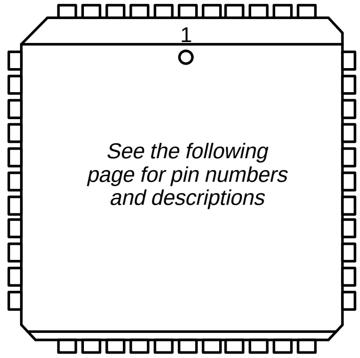
See Packaging Section for Package Dimensions



44-Pin PQFP (14 mm x 14 mm)
Q44



44-Pin PGA
G44



44-Pin PLCC
P44

PIN OUT DEFINITIONS

PLCC PIN NO.	PQFP & PGA PIN NO.	NAME	DESCRIPTION
29	1	N/C	No Connection
30	2	VO3	DAC 3 Output
31	3	V_{EE}	Analog Negative Power Supply (–12 V)
32	4	V_{CC}	Analog Positive Power Supply (+12 V)
33	5	DGND	Digital Ground (0 V)
34	6	V_{REF}	Analog Positive Voltage Reference Input (+5 V)
35	7	V_{REFN}	Analog Negative Voltage Reference Output (–2.5 V)
36	8	V_{CC}	Analog Positive Power Supply (+12 V)
37	9	V_{EE}	Analog Negative Power Supply (–12 V)
38	10	VO4	DAC 4 Output
39	11	N/C	No Connection
40	12	VO5	DAC 5 Output
41	13	VO6	DAC 6 Output
42	14	VO7	DAC 7 Output
43	15	AGND	Analog Ground (0 V)
44	16	$\overline{CS}$	Chip Select Enable
1	17	$\overline{RD}$	Read Back Enable
2	18	$\overline{R2}$	Second–Latch-Bank Reset Enable
3	19	$\overline{R1}$	First–Latch-Bank Reset Enable
4	20	$\overline{LD2}$	Second–Latch-Bank Load Enable
5	21	$\overline{LD1}$	First–Latch-Bank Load Enable
6	22	A2	Digital Address Bit 2
7	23	A1	Digital Address Bit 1
8	24	A0	Digital Address Bit 0
9	25	N/C	No Connection
10	26	N/C	No Connection
11	27	DB0	Digital Input Data Bit 0 (LSB)
12	28	DB1	Digital Input Data Bit 1
13	29	DB2	Digital Input Data Bit 2
14	30	DB3	Digital Input Data Bit 3
15	31	DB4	Digital Input Data Bit 4
16	32	DB5	Digital Input Data Bit 5
17	33	DB6	Digital Input Data Bit 6
18	34	DB7	Digital Input Data Bit 7
19	35	DB8	Digital Input Data Bit 8
20	36	DB9	Digital Input Data Bit 9
21	37	DB10	Digital Input Data Bit 10
22	38	DB11	Digital Input Data Bit 11 (MSB)
23	39	DV_{DD}	Digital Positive Power Supply (+5 V)
24	40	DGND	Digital Ground (0 V)
25	41	AGND	Analog Ground (0 V)
26	42	VO0	DAC 0 Output
27	43	VO1	DAC 1 Output
28	44	VO2	DAC 2 Output

ELECTRICAL CHARACTERISTICS

V_{CC} = +12 V, V_{EE} = –12 V, V_{REF} = 5 V, DV_{DD} = 5.0 V, T = 25°C, Output Load = 5kΩ (unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE								
Resolution (All Grades)	N	12					Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity Spec
A				±2		±2		
B				±1		±1		
Differential Non-Linearity	DNL						LSB	
A				±1		±1		
B				±0.75		±0.75		
Positive Full Scale Error	+FSE						LSB	
A			6	±8		±8		
B			4	±6		±6		
Negative Full Scale Error	–FSE						LSB	
A			6	±8		±8		
B			4	±6		±6		
Bipolar Zero Offset	ZOFS						LSB	
A				±4		±4		
B				±3		±3		
INL Matching	ΔINL						LSB	
A				±2		±2		
B				±1.5		±1.5		
All Channels Maximum Error with DAC 0 adjusted to minimum error	ME						LSB	
A				±4		±4		
B				±2		±2		
Bipolar Zero Matching	ΔZUFS						LSB	
A				±4		±4		
B				±3		±3		
Full Scale Error Matching	ΔFSE						LSB	
A				±4		±4		
B				±3		±3		
DYNAMIC PERFORMANCE								
Voltage Settling from $\overline{LD}$ to VDAC Out[1]	t_{sd}		30	50		50	µs	ZS to FS (20 V Step)
Channel-to-Channel Crosstalk[1, 6]	CT		0.04				LSB	DC
Digital Feedthrough[1, 6]	Q		–70				dB	CLK and Data to V_{OUTi}
Power Supply Rejection Ratio	PSRR			5			ppm/%	ΔV_{EE} & ΔV_{CC} = ±5%, ppm of FS
REFERENCE INPUTS								
Impedance of V_{REF}	REF	350	700	1.05k	350	1.05k	Ω	See Application Hints for driving the reference input
V_{REF} Voltage[1, 2]	V_{REF}	3.5		6			V	

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL INPUTS[3]								
Logic High	V_{IH}	2.4					V	
Logic Low	V_{IL}			0.8			V	
Input Current	I_L			±10			µA	
Input Capacitance[1]	C_L			8			pF	
ANALOG OUTPUTS								
Output Swing		$-V_{EE}$ +1.4		V_{CC} –1.4			V	
Output Drive Current		–5		5			mA	
V_{REFN} Output Drive Current		–10		+10			µA	For test purposes only
Output Impedance	R_O		1				Ω	
Output Short Circuit Current	I_{SC}		25				mA	+FS to AGND
			30				mA	+FS to V_{EE}
			40				mA	–FS to AGND
			55				mA	–FS to V_{CC}
DIGITAL OUTPUTS								
Output High Voltage	V_{OH}		4.5				V	
Output Low Voltage	V_{OL}		0.5				V	
POWER SUPPLIES								
V_{CC} Voltage[5]	V_{CC}	V_{REF}+1.5	12	12.75	V_{REF}+1.5	12.75	V	
V_{EE} Voltage[5]	V_{EE}	–12.75	–12	–5	–12.75	–5	V	
DV_{DD} Voltage	DV_{DD}	4.5	5	5.5	4.5	5.5	V	
Positive Supply Current	I_{CC}		8	10		10	mA	Bipolar zero
Negative Supply Current	I_{EE}		15	20		20	mA	Bipolar zero
Digital Supply Current	I_{DD}			2		2	mA	Bipolar zero
Power Dissipation	PD_{ISS}		320	420		450	mW	Bipolar zero
ANALOG GROUND CURRENT								
Per Channel[1]	I_{AGND}		±60				µA	See Application Notes
DIGITAL TIMING SPECIFICATIONS[1,4]								V_{IL} = 0 V, V_{IH} = 5 V, CL = 20 pF
Data Setup Time	t_{DS}	20					ns	
Data Hold Time	t_{DH}	20					ns	
Address Set-up Time	t_{AS}	100					ns	
Address Hold Time	t_{AH}	0					ns	
Chip Select to $\overline{LD1}$ Set-up Time	t_{CS1}	6					ns	
Chip Select to $\overline{LD1}$ Hold Time	t_{CH1}	0					ns	
$\overline{LD1}$ Pulse Width	t_{LD1W}	50					ns	
$\overline{LD1}$ Negative Edge to $\overline{LD2}$ Positive Edge	t_{LD1LD2}	60					ns	
$\overline{LD2}$ Pulse Width	t_{LD2W}	60					ns	
Chip Select to $\overline{RD}$ Set-Up Time	t_{CS2}	6					ns	
Chip Select to $\overline{RD}$ Hold Time	t_{CH2}	0					ns	
$\overline{RD}$ Pulse Width	t_{RD}	600					ns	
High Z to Data Valid for Readback	t_{DA}	600					ns	
Data Valid for Readback to High Z	t_{DR}	200					ns	
$\overline{R1}$ Pulse Width	R1W	100					ns	
$\overline{R2}$ Pulse Width	R2W	100					ns	

Specifications are subject to change without notice

ELECTRICAL CHARACTERISTICS (CONT'D)

NOTES:

1 Guaranteed; not tested.
2 Specified values guarantee functionality.
3 Digital inputs should not go below digital GND or exceed DV_{DD} supply voltage.
4 *See Figures 1, 2, and 3.* All digital input signals are specified with $t_R = t_F$ = 10 ns 10% to 90% and timed from a 50% voltage level.
5 For power supply values < $\pm 2 * V_{REF}$, the output swing is limited as specified in Analog Outputs.
6 Digital feedthrough and channel-to-channel crosstalk are heavily dependent on the board layout and environment.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1, 2]

V_{CC} to AGND . . . . +16.5 V
V_{EE} to AGND . . . . –16.5 V
DV_{DD} to DGND . . . . +6.5 V
V_{REF} to DGND . . . . +7.0 V
Analog Outputs & Inputs
Infinite Shorts to V_{CC}, V_{EE}, DV_{DD}, AGND and DGND (provided that power dissipation of the package spec is not exceeded)
AGND to DGND . . . . ±1 V
(Functionality guaranteed for ±0.5 V only)

Digital Input & Digital Output Voltage to:
DV_{DD} . . . . +.5 V
DGND . . . . –.5 V
Operating Temperature Range . . . . –40°C to +85°C
Maximum Junction Temperature . . . . 150°C
Storage Temperature Range . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . +300°C
Package Power Dissipation Rating to 75°C
PQFP, PGA, PLCC 800mW
Derates above 75°C . . . . 11mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

APPLICATION NOTES
Refer to Section 8 for Applications Information

NOTE: When using these DACs to drive remote devices, the accuracy of the output can be improved by utilizing a remote analog ground connection. The difference between the DGND and AGND should be limited to ±300 mV to assure normal operation. If there is any chance that the AGND to DGND can be greater than ±1 V, we recommend two back-to-back diodes be used between DGND and AGND to clamp the voltage and prevent damage to the DAC. Using a buffer between the remote ground location and AGND may help reduce noise induced from long lead or trace lengths.

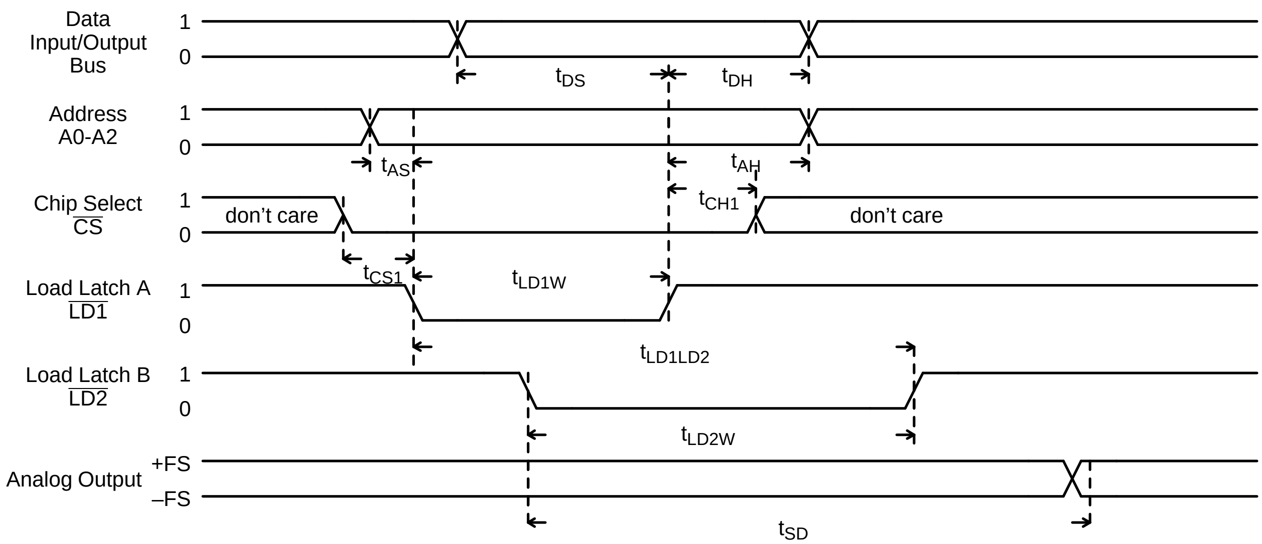


Figure 1. Loading Latch A and Updating Latch B

Notes
(1) Chip Select ($\overline{CS}$) and Load LATCHA ($\overline{LD1}$) Signals follow the same timing constraints and are interchangeable in the above diagram.
(2) $\overline{R1}$ = $\overline{R2}$ = 1.
(3) For the case where $\overline{LD2}$ is in the low state, analog output would respond to the falling edge of $\overline{LD1}$ (transparent mode).

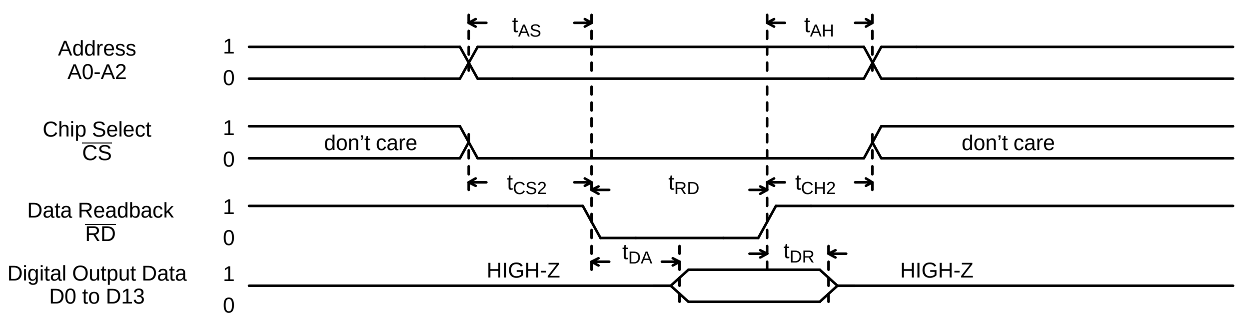


Figure 2. Read Back First Latch Bank of One DAC

Notes
(1) Chip Select ($\overline{CS}$) and Data Readback ($\overline{RD}$) Signals follow the same timing constraints and are interchangeable in the above diagram.
(2) $\overline{R1}$ = $\overline{R2}$ = 1.

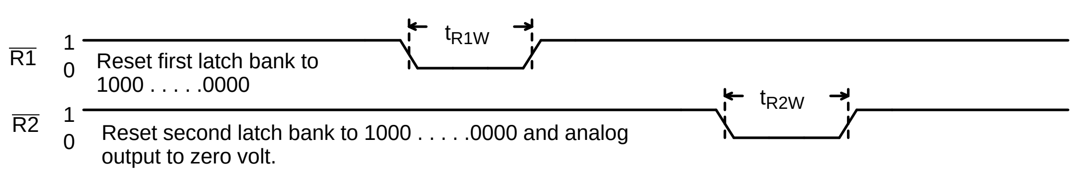


Figure 3. Reset Operations

A standard μ-processor and TTL/CMOS compatible input data port loads the data into the pre-selected DACS. If $\overline{CS}$ = 0, the chip accesses digital data on the bus. Then address bits A0 to A2 select the appropriate DAC and $\overline{LD1}$ loads the data into the first-latch-bank. When all 8-channels first-latch-banks are loaded, then $\overline{LD2}$ enables the second-latch-bank and updates all 8-channels simultaneously. The selected DAC becomes transparent (activity on the digital inputs appear at the analog output) when both $\overline{LD1}$ = $\overline{LD2}$ = 0.

$\overline{R1}$ = 0 resets the first-latch-bank. $\overline{R2}$ = 0 resets the second-latch-bank which sets the analog output to zero volts (data = 100...00), regardless of digital inputs.

Function	A2	A1	A0	$\overline{RD}$	$\overline{LD1}$	$\overline{LD2}$	$\overline{CS}$	$\overline{R1}$	$\overline{R2}$
Load Latch 1 of DAC1	0	0	0	1	0→1	1	0	1	1
Load Latch 1 of DAC2	0	0	1	1	0→1	1	0	1	1
Load Latch 1 of DAC3	0	1	0	1	0→1	1	0	1	1
Load Latch 1 of DAC4	0	1	1	1	0→1	1	0	1	1
Load Latch 1 of DAC5	1	0	0	1	0→1	1	0	1	1
Load Latch 1 of DAC6	1	0	1	1	0→1	1	0	1	1
Load Latch 1 of DAC7	1	1	0	1	0→1	1	0	1	1
Load Latch 1 of DAC8	1	1	1	1	0→1	1	0	1	1
Load Latch 2 of DAC1→8	X	X	X	1	1	0→1	0	1	1
Read Latch 1 of DAC1	0	0	0	0	1	1	0	1	1
Read Latch 1 of DAC2	0	0	1	0	1	1	0	1	1
Read Latch 1 of DAC3	0	1	0	0	1	1	0	1	1
Read Latch 1 of DAC4	0	1	1	0	1	1	0	1	1
Read Latch 1 of DAC5	1	0	0	0	1	1	0	1	1
Read Latch 1 of DAC6	1	0	1	0	1	1	0	1	1
Read Latch 1 of DAC7	1	1	0	0	1	1	0	1	1
Read Latch 1 of DAC8	1	1	1	0	1	1	0	1	1
Reset Latch 1 of DAC1→8	X	X	X	X	X	X	X	0	1
Reset Latch 2 of DAC1→8	X	X	X	X	X	X	X	1	0

Note: 1: High, 0: Low, X: Don't Care

Table 1. Octal Parallel Data Input 14-Bit DAC Truth Table

Note: For timing information see Electrical Characteristics

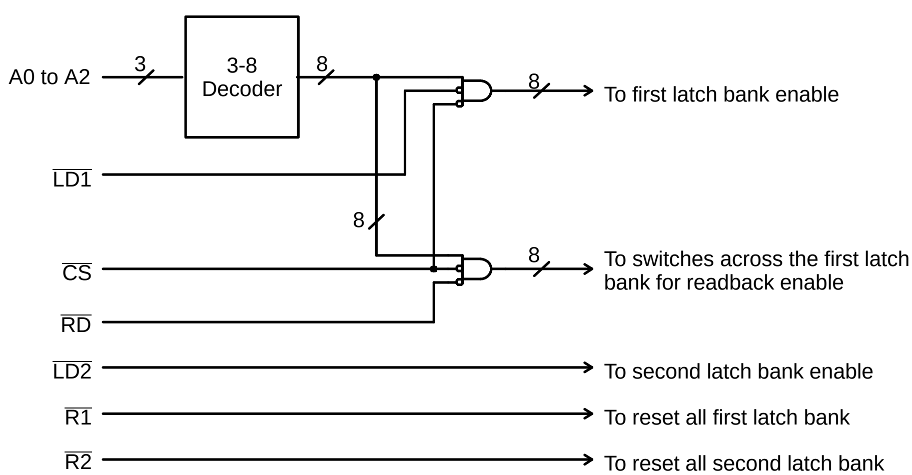


Figure 4. Simplified Parallel Logic Port

Hex Code	Binary Code	Output Voltage = 2 • Vr (–1 + $\frac{2 \bullet D}{4096}$) (Vr = +5 V)
0 0 0	000000000000	10 • (–1 + 0) = –10
⋮	⋮	⋮
7 F F	011111111111	10 • (–1 + $\frac{4094}{4096}$) = –4.88 mV
8 0 0	100000000000	10 • (–1 + $\frac{4096}{4096}$) = 0
8 0 1	100000000001	10 • (–1 + $\frac{4098}{4096}$) = 4.88 mV
⋮ F F F	⋮ 111111111111	⋮ 10 • (–1 + $\frac{8190}{4096}$) = 9.99512

Table 2. MP7613
Ideal DAC Output vs. Input Code

Note: See Electrical Characteristics on pages 28-30 for real system accuracy

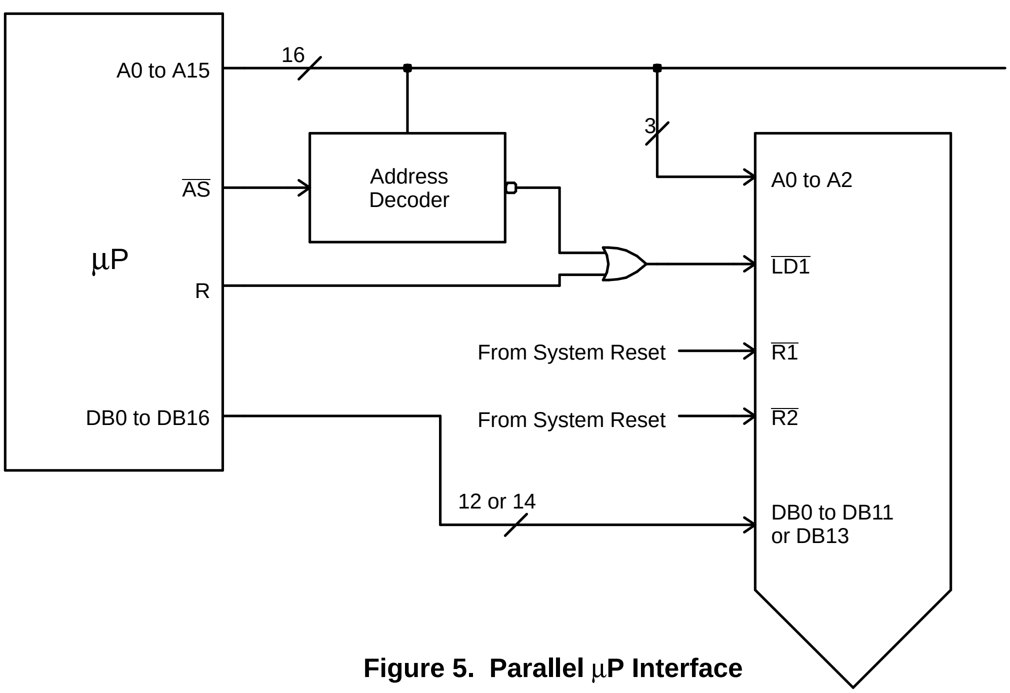
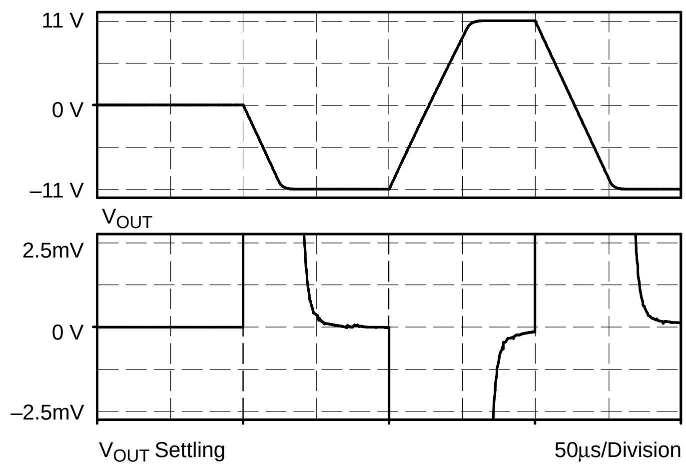
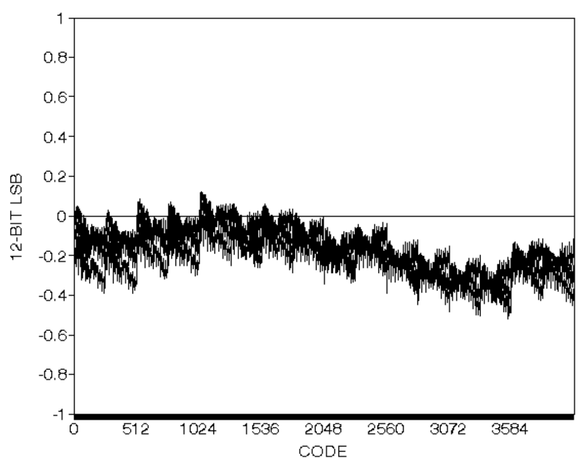


Figure 5. Parallel μP Interface

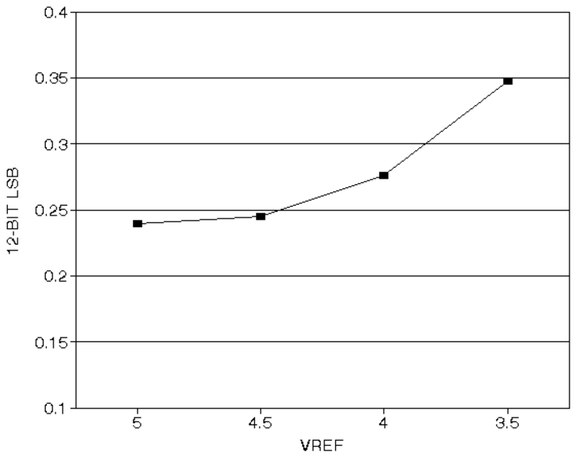


Graph 1. Typical Output Settling Characteristic
V_{REF} = 5 V, R_L = 5K, C_L = 500pF

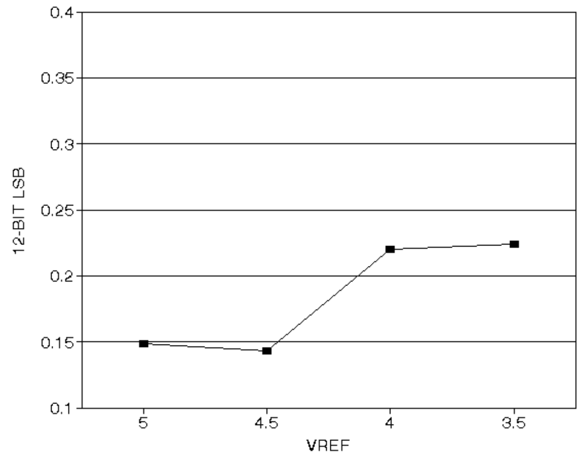
Graph 1 shows the typical output settling characteristic of the MP7610 Family for a RESET →ZS→FS→ZS series of code transitions. The top graph shows the output voltage transients, while the bottom graph shows the difference between the output and the ideal output.



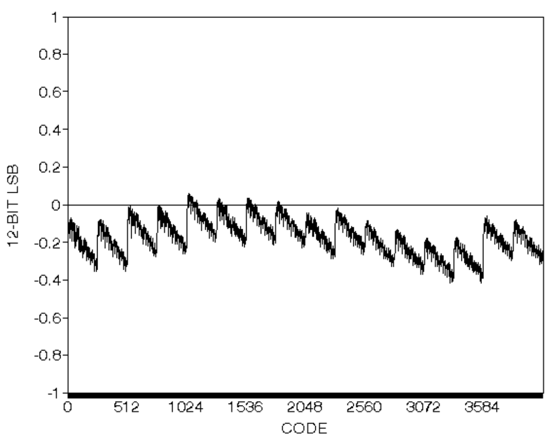
Graph 2. Linearity with
V_{REF} = 5 V, All DACs, All Codes



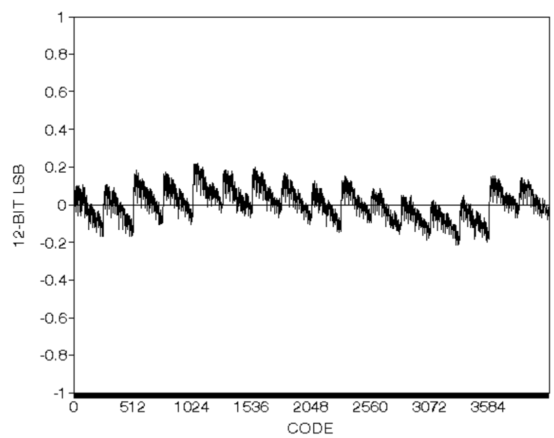
Graph 3. DAC 0 INL vs. V_{REF}



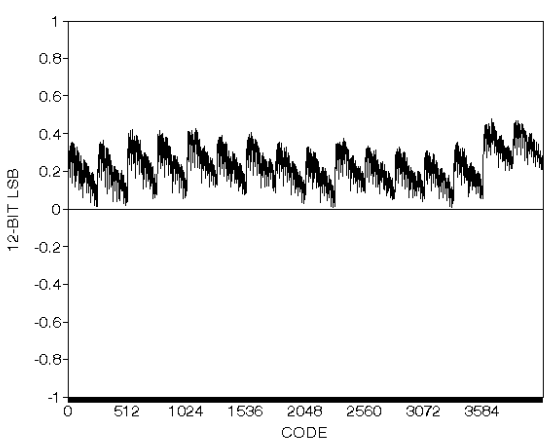
Graph 4. DAC 0 DNL vs. V_{REF}



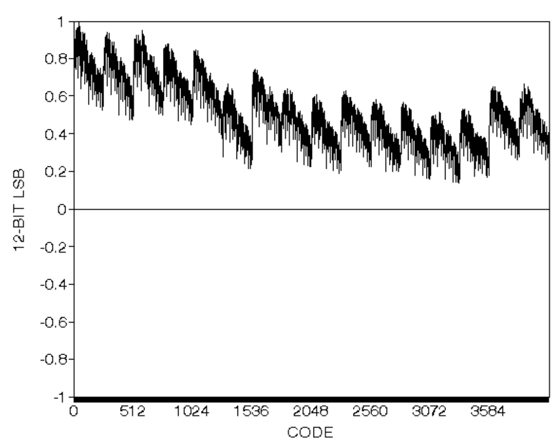
Graph 5. DAC 0 Linearity with V_{REF} = 5 V, V_{OUT} = ±10



Graph 6. DAC 0 Linearity with V_{REF} = 4.5 V, V_{OUT} = ±9



Graph 7. DAC 0 Linearity with V_{REF} = 4 V, V_{OUT} = ±8



Graph 8. DAC 0 Linearity with V_{REF} = 3.5 V, V_{OUT} = ±7

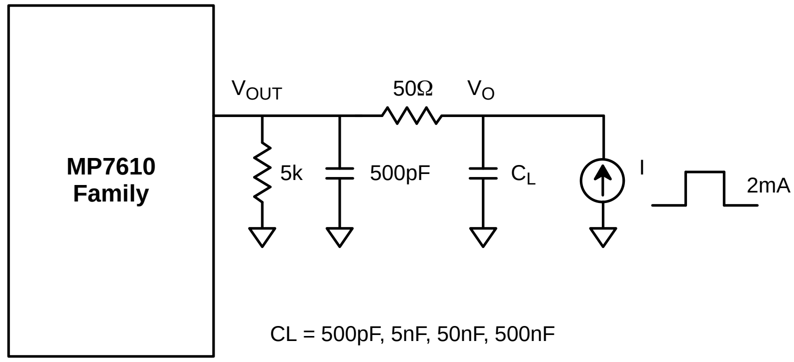
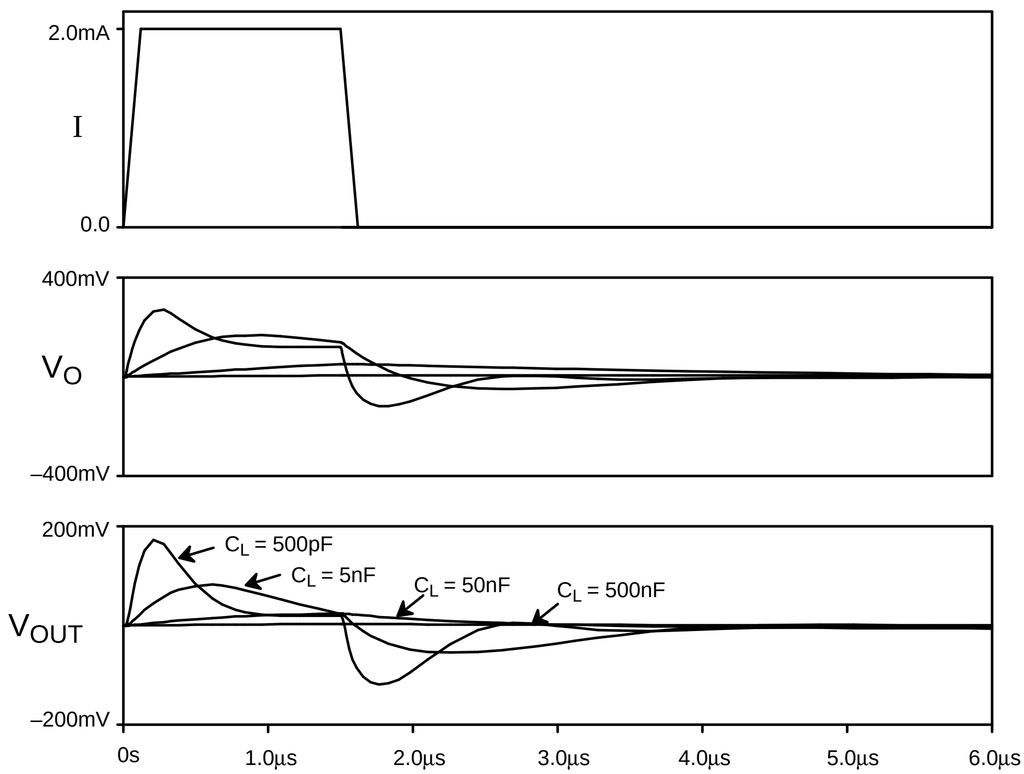
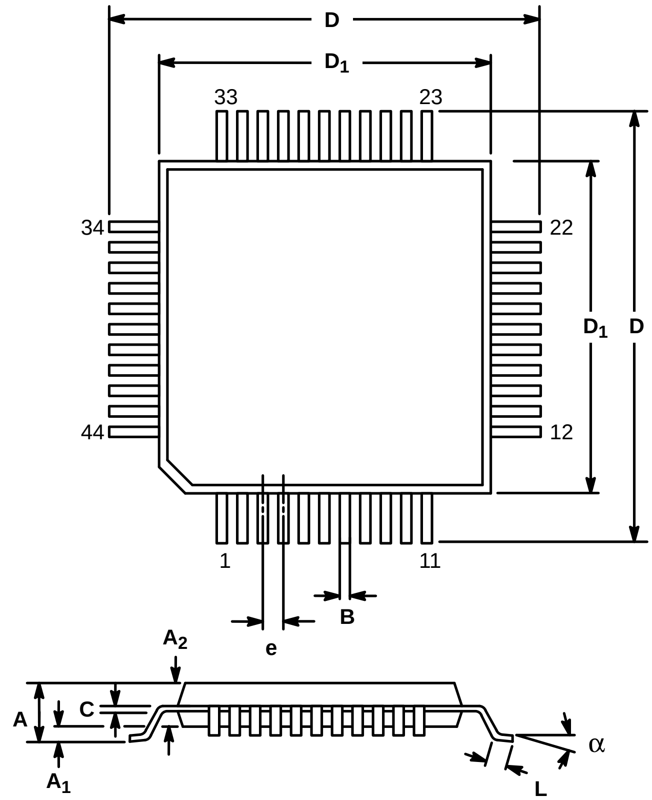


Figure 6. Circuit for Determining Typical Analog Output Pulse Response



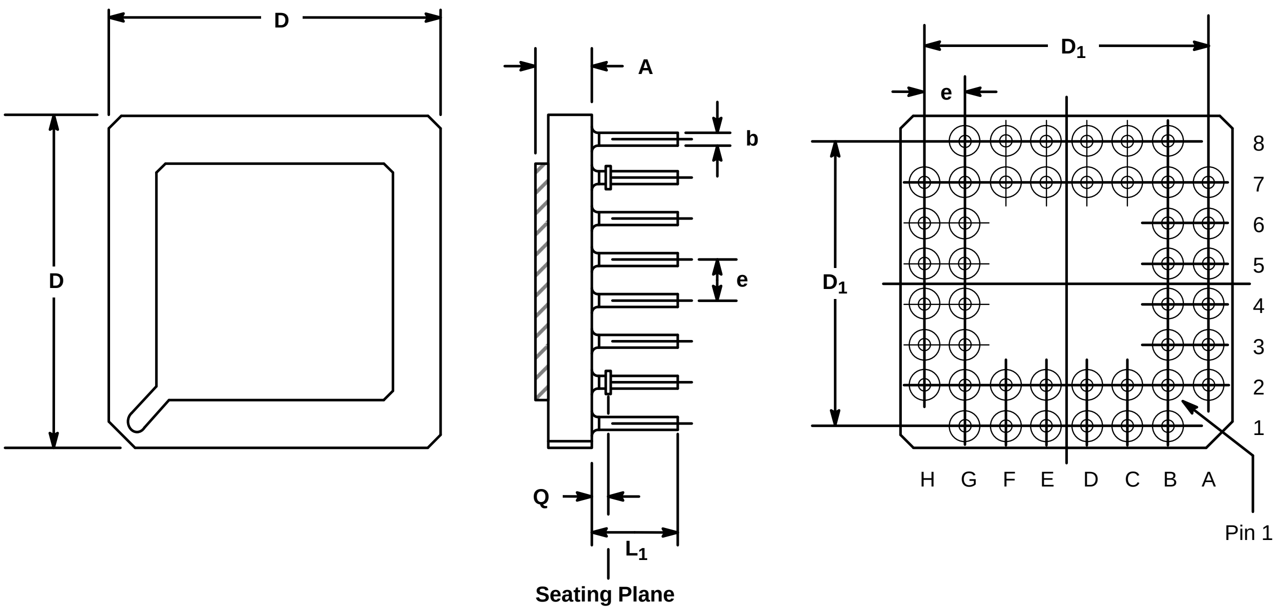
Graph 9. Typical Response of the MP7610 Family Analog Output to a Current Pulse with CL=500pF, 5nF, 50nF, 500nF (*See NO TAG above*)

44 LEAD PLASTIC QUAD FLAT PACK (14mm x 14mm PQFP, METRIC) Q44



SYMBOL	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	3.15	—	0.124
A_1	0.25	—	0.01	—
A_2	2.6	2.8	0.102	0.110
B	0.3	0.4	0.012	0.016
C	0.13	0.23	0.005	0.009
D	16.95	17.45	0.667	0.687
D_1	13.9	14.1	0.547	0.555
e	1.00 BSC		0.039 BSC	
L	0.65	1.03	0.026	0.040
α	0°	7°	0°	7°
Coplanarity = 4 mil max.				

44 LEAD PIN GRID ARRAY
(PGA)
G44



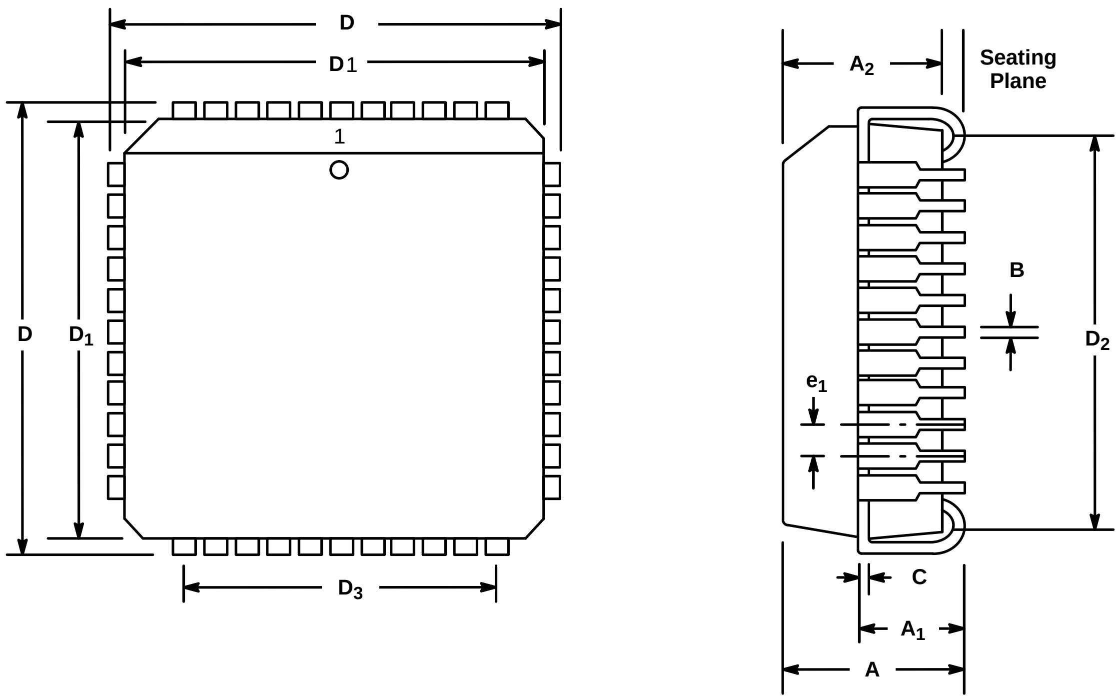
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.082	0.10	2.08	2.54
b	0.016	0.020	0.406	0.508
D	0.841	0.859	21.4	21.8
D_1	0.688	0.712	17.5	18.1
e	0.100 typ.		2.54 typ.	
L_1	0.170	0.190	4.32	4.83
Q	0.050 typ.		1.27 typ.	

CONNECTION TABLE

PAD	PIN	PAD	PIN	PAD	PIN
1	B2	16	G4	31	C8
2	B1	17	H4	32	C7
3	C2	18	H5	33	B8
4	C1	19	G5	34	B7
5	D2	20	H6	35	A7
6	D1	21	G6	36	B6
7	E1	22	H7	37	A6
8	E2	23	G7	38	B5
9	F1	24	G8	39	A5
10	F2	25	F7	40	A4
11	G1	26	F8	41	B4
12	G2	27	E7	42	A3
13	H2	28	E8	43	B3
14	G3	29	D8	44	A2
15	H3	30	D7		

Note: The letters A-H and numbers 1-8 are the coordinates of a grid. For example, pin 1 is at the intersections of the "B" vertical line and the "2" horizontal line.

44 LEAD PLASTIC LEADED CHIP CARRIER (PLCC) P44



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.165	0.180	4.19	4.57
A_1	0.100	0.110	2.54	2.79
A_2	0.148	0.156	3.76	3.96
B	0.013	0.021	0.330	0.553
C	0.097	0.0103	0.246	0.261
D	0.685	0.695	17.40	17.65
D_1 (1)	0.650	0.654	16.51	16.61
D_2	0590	0.630	14.99	16.00
D_3	0.500 Ref		12.70 Ref.	
e_1	0.050 BSC		1.27 BSC	

Note: (1) Dimension D_1 does not include mold protrusion. Allowed mold protrusion is 0.254 mm/0.010 in.

NOTICE