MP75L45

Low Voltage CMOS
Buffered Multiplying 12-Bit
Digital-to-Analog Converter

FEATURES

- **3.3 V Operation**
- **Full Four Quadrant Multiplication**
- **12-Bit Resolution**
- **Latch-Up Free**
- **Extremely Low Power CMOS: 0.3 mW (typ.)**

APPLICATIONS

- **Disk Drive Servo Systems**
- **Digital/Synchro Conversion**
- **Programmable Gain Amplifiers**
- **Ratiometric A/D Conversion**
- **Function Generation**
- **Digitally Controlled Filters**

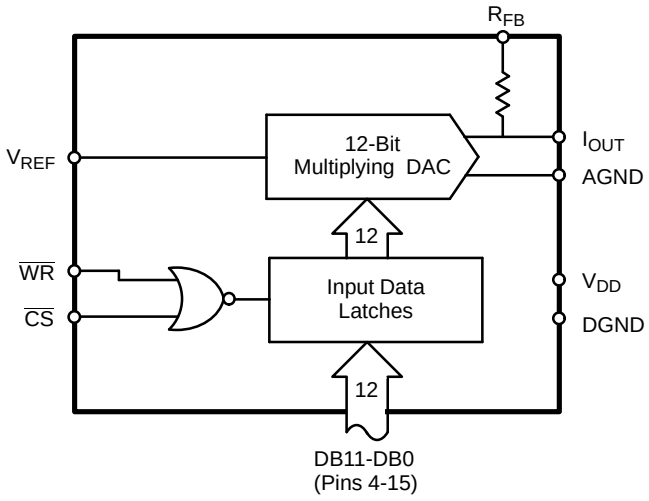
GENERAL DESCRIPTION

The MP75L45 is a 12-bit CMOS multiplying Digital-to-Analog Converter with on-board data latches. It is loaded by a single 12-bit wide word and interfaces directly to most 12- and 16-bit bus systems. Data is loaded into the input latches under the control of the $\overline{CS}$ and $\overline{WR}$ inputs; tying these control inputs low makes the input latches transparent, allowing direct unbuffered operation of the DAC.

The MP75L45 is particularly suitable for single supply operation and applications with wide temperature variations.

Specified for operation over the commercial / industrial (–40 to +85°C) temperature range, the MP75L45 is available in Plastic dual-in-line (PDIP), Surface Mount (SOIC), and Shrunk Small (SSOP) outline packages.

SIMPLIFIED BLOCK DIAGRAM

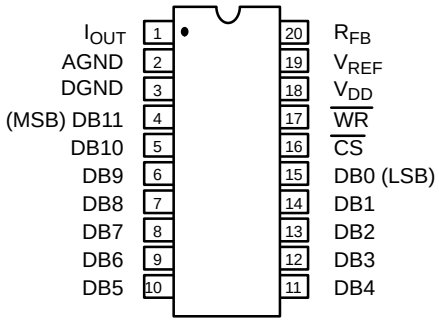


ORDERING INFORMATION

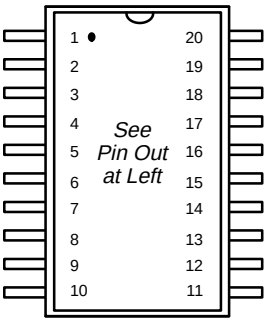
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	–40 to +85°C	MP75L45KN	1	±1	±10
SOIC	–40 to +85°C	MP75L45KS	1	±1	±10
SSOP	–40 to +85°C	MP75L45KQ	1	±1	±10

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



20 Pin PDIP (0.300")
N20



20 Pin SOIC (Jedec, 0.300") – S20
20 Pin SSOP – A20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I_{OUT}	Output Current
2	AGND	Analog Ground
3	DGND	Digital Ground
4	DB11	Data Input Bit 11 (MSB)
5	DB10	Data Input Bit 10
6	DB9	Data Input Bit 9
7	DB8	Data Input Bit 8
8	DB7	Data Input Bit 7
9	DB6	Data Input Bit 6
10	DB5	Data Input Bit 5

PIN NO.	NAME	DESCRIPTION
11	DB4	Data Input Bit 4
12	DB3	Data Input Bit 3
13	DB2	Data Input Bit 2
14	DB1	Data Input Bit 1
15	DB0	Data Input Bit 0 (LSB)
16	$\overline{CS}$	Chip Select (Active Low)
17	$\overline{WR}$	Write (Active Low)
18	V_{DD}	Digital Supply Voltage
19	V_{REF}	Reference Input
20	R_{FB}	Feedback Resistor

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 3 V, V_{REF} = +3 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]						
Resolution (All Grades)	N	12			Bits	
Integral Non-Linearity (Relative Accuracy)	INL			±1	LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
Differential Non-Linearity	DNL			±1	LSB	
Gain Error	GE		±5	±10	LSB	Using Internal R_{FB}
Gain Temperature Coefficient[2]	TC_{GE}		10		ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR		±50		ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}			±10	nA	
REFERENCE INPUT						
Input Resistance	R_{IN}	7		25	KΩ	
DIGITAL INPUTS[3]						
Logical "1" Voltage	V_{IH}	2.5			V	
Logical "0" Voltage	V_{IL}			0.5	V	
Input Leakage Current	I_{LKG}			±1	µA	
Input Capacitance[2]						
Data	C_{IN}			5	pF	
Control	C_{IN}			20	pF	
POWER SUPPLY[5]						
Functional Voltage Range	V_{DD}	3	3.3	3.6	V	
Supply Current	I_{DD}		10	100	µA	All digital inputs = 0 V or V_{DD}
SWITCHING CHARACTERISTICS[4]						
Chip Select to Write Set-Up Time	t_{CS}		200		ns	
Chip Select to Write Hold Time	t_{CH}		10		ns	
Data Valid to Write Set-Up Time	t_{DS}		100		ns	
Data Valid to Write Hold Time	t_{DH}		10		ns	
Write Pulse Width	t_{WR}		175		ns	

NOTES:

1 Full Scale Range (FSR) is 3 V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 0 to +5 V
Digital Input Voltage to GND .... GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND (2) ..... ±25 V
V_{RFB} to GND (2) ..... ±25 V

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
PDIP, SOIC, SSOP 900mW
Derates above 75°C ..... 12mW/°C

NOTES:
1 Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

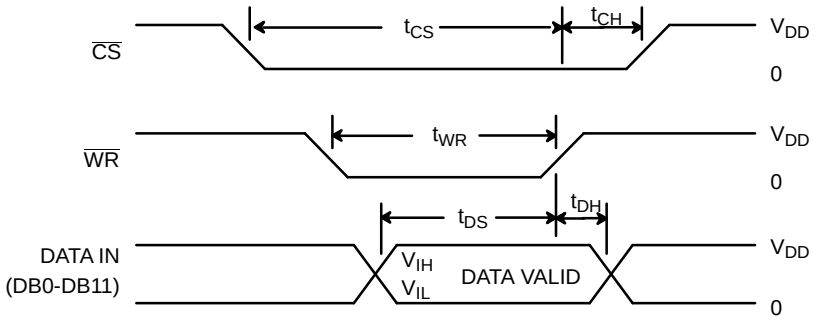
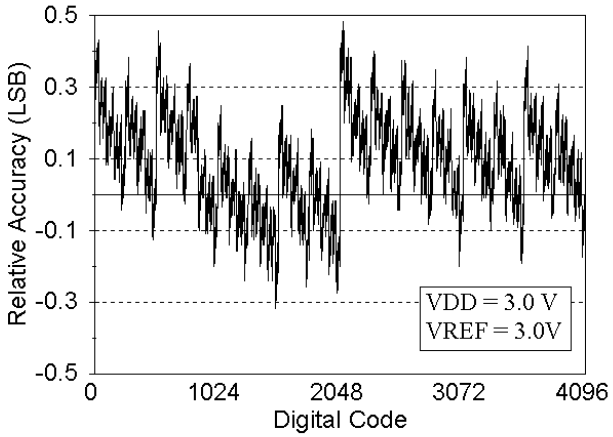
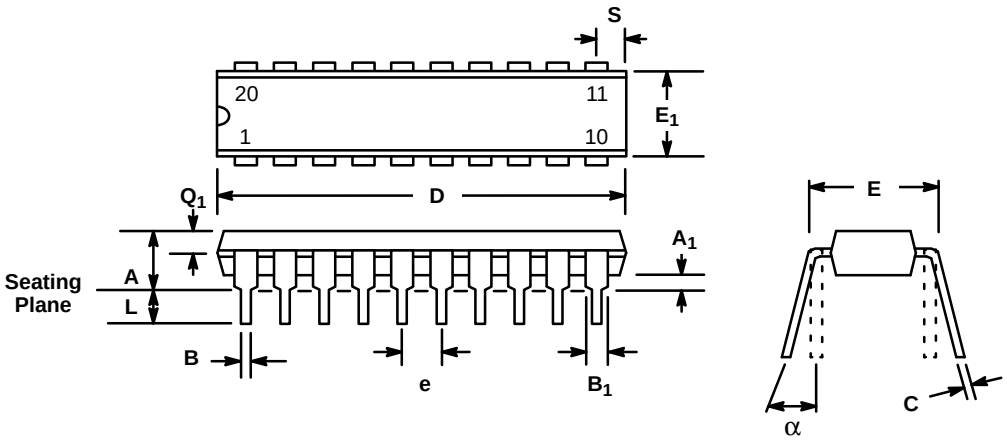


Figure 1. Write Cycle Timing Diagram



Graph 1. Relative Accuracy vs. Digital Code

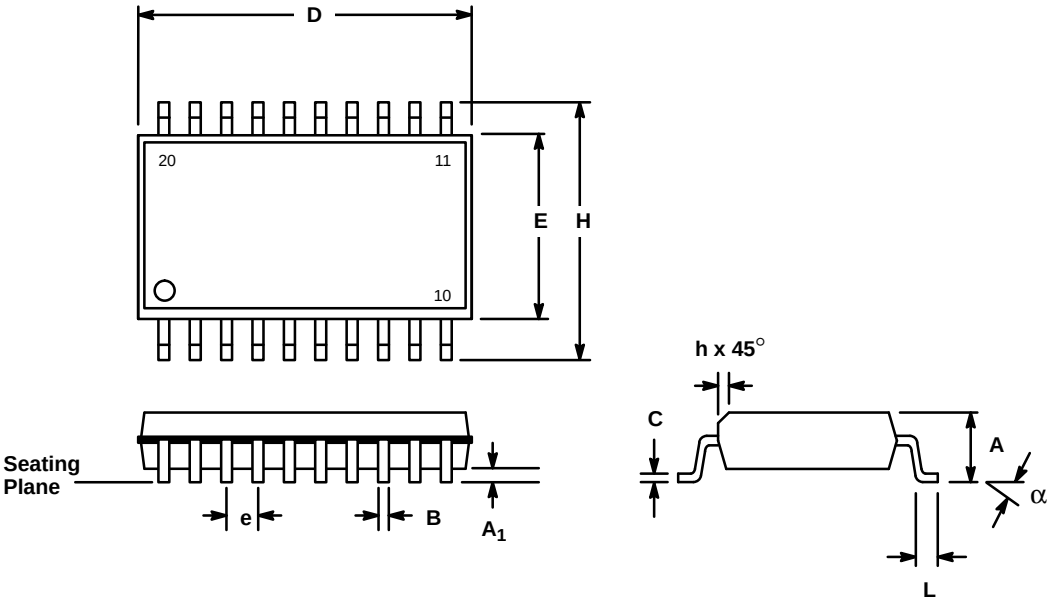
20 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.945	1.060	24.0	26.92
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.080	1.02	2.03

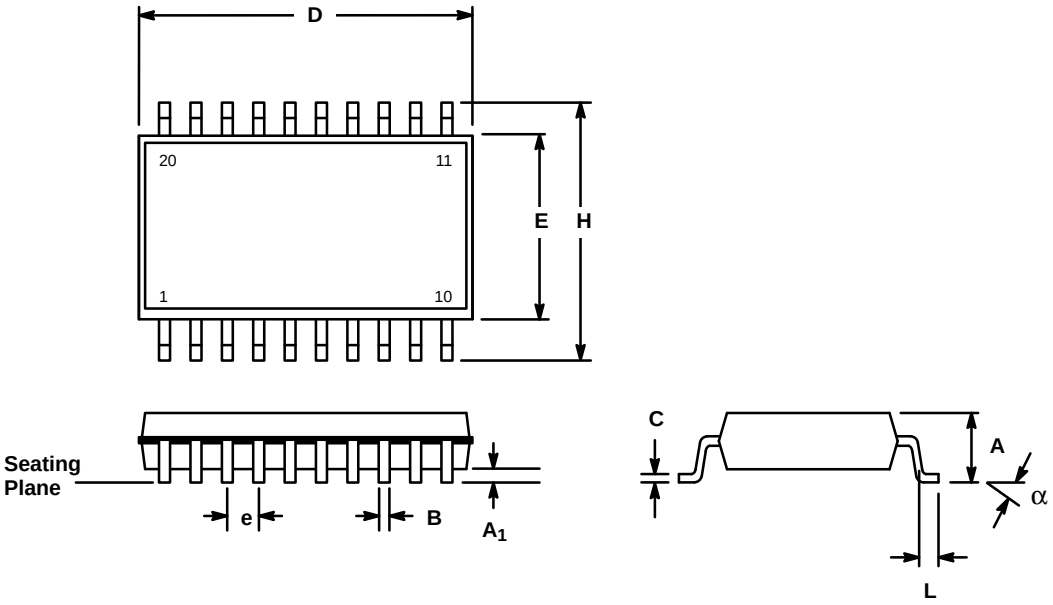
Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

20 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.642
A_1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.500	0.510	12.70	12.95
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

20 LEAD SHRINK SMALL OUTLINE PACKAGE (SSOP) A20



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.73	2.05	0.068	0.081
A_1	0.05	0.21	0.002	0.008
B	0.20	0.40	0.008	0.016
C	0.13	0.25	0.005	0.010
D	7.07	7.40	0.278	0.291
E	5.20	5.38	0.205	0.212
e	0.65 BSC		0.0256 BSC	
H	7.65	8.1	0.301	0.319
L	0.45	0.95	0.018	0.037
α	0°	8°	0°	8°

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contains here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Datasheet April 1995