MP7545

CMOS
Buffered Multiplying 12-Bit
Digital-to-Analog Converter

FEATURES

- **Full Four Quadrant Multiplication**
- **12-Bit Resolution**
- **Gain Error Tempco (2 ppm/C max.)**
- **Latch-Up Free**
- **Single +5 V to +15 V Supply**
- **Use MP7545B for New Designs**
- **TTL/15 V VMOS Compatible**

APPLICATIONS

- **Industrial Automation**
- **Automatic Test Equipment**
- **Disk Drive Servo Systems**
- **Digital/Synchro Conversion**
- **Programmable Gain Amplifiers**
- **Ratiometric A/D Conversion**
- **Function Generation**
- **Digitally Controlled Filters**

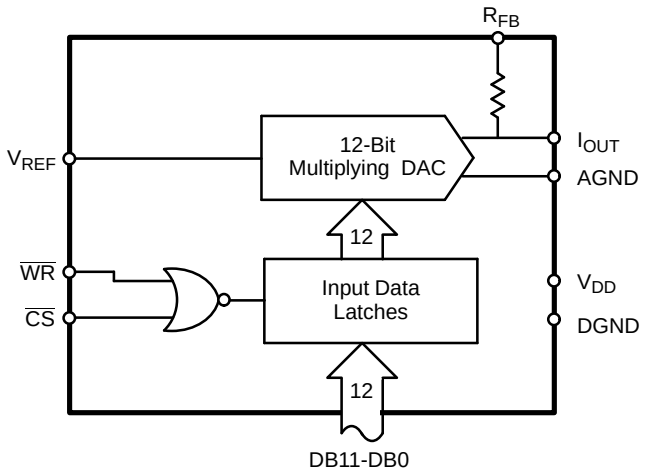
GENERAL DESCRIPTION

The MP7545 is a 12-bit CMOS multiplying Digital-to-Analog Converter with on-board data latches. It is loaded by a single 12-bit wide word and interfaces directly to most 12- and 16-bit bus systems. Data is loaded into the input latches under the control of the $\overline{CS}$ and $\overline{WR}$ inputs; tying these control inputs low makes the input latches transparent allowing direct unbuffered operation of the DAC.

The MP7545 is particularly suitable for single supply operation and applications with wide temperature variations.

The MP7545 can be used with any supply voltage from +5 V to +15 V. With CMOS logic levels at the inputs the device dissipates less than 0.5 mW for V_{DD} = +5 V.

SIMPLIFIED BLOCK DIAGRAM



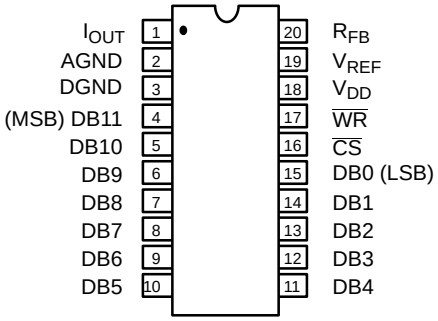
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	–40 to +85°C	MP7545JN	±2	±4	±20
Plastic Dip	–40 to +85°C	MP7545KN	±1	±1	±10
Plastic Dip	–40 to +85°C	MP7545LN	±1/2	±1	±5
SOIC	–40 to +85°C	MP7545JS	±2	±4	±20
SOIC	–40 to +85°C	MP7545KS	±1	±1	±10
SOIC	–40 to +85°C	MP7545LS	±1/2	±1	±5
PLCC	–40 to +85°C	MP7545JP	±2	±4	±20
PLCC	–40 to +85°C	MP7545KP	±1	±1	±10
PLCC	–40 to +85°C	MP7545LP	±1/2	±1	±5
Ceramic Dip	–40 to +85°C	MP7545AD	±2	±4	±20
Ceramic Dip	–40 to +85°C	MP7545BD	±1	±1	±10
Ceramic Dip	–40 to +85°C	MP7545CD	±1/2	±1	±5
Ceramic Dip	–55 to +125°C	MP7545SD*	±2	±4	±20
Ceramic Dip	–55 to +125°C	MP7545TD*	±1	±1	±10

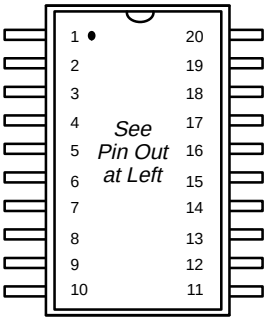
*Contact factory for non-compliant military processing

PIN CONFIGURATIONS

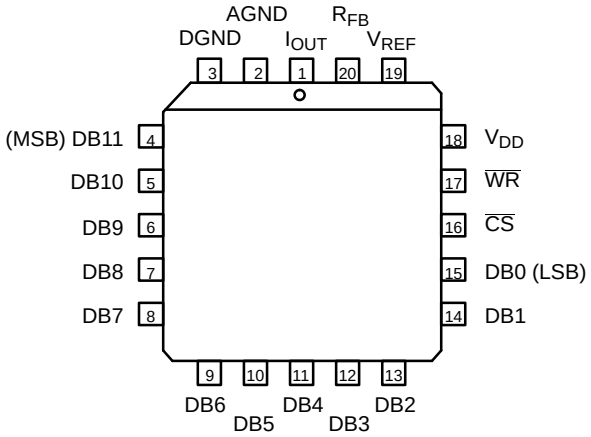
See Packaging Section for Package Dimensions



20 Pin CDIP, PDIP (0.300")
D20, N20



20 Pin SOIC (Jedec, 0.300") – S20
20 Pin SSOP – A20



20 Pin PLCC
P20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I_{OUT}	Output Current
2	AGND	Analog Ground
3	DGND	Digital Ground
4	DB11	Data Input Bit 11 (MSB)
5	DB10	Data Input Bit 10
6	DB9	Data Input Bit 9
7	DB8	Data Input Bit 8
8	DB7	Data Input Bit 7
9	DB6	Data Input Bit 6
10	DB5	Data Input Bit 5
11	DB4	Data Input Bit 4
12	DB3	Data Input Bit 3
13	DB2	Data Input Bit 2
14	DB1	Data Input Bit 1
15	DB0	Data Input Bit 0 (LSB)
16	$\overline{CS}$	Chip Select (Active Low)
17	$\overline{WR}$	Write (Active Low)
18	V_{DD}	Digital Supply Voltage
19	V_{REF}	Reference Input
20	R_{FB}	Feedback Resistor

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 5 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
J, A, S				±2		±2		
K, B, T				±1		±1		
L, C				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	
J, A, S				±4		±4		
K, B, T				±1		±1		
L, C				±1		±1		
Gain Error	GE						LSB	Using Internal R_{FB}
J, A, S				±20		±20		
K, B, T				±10		±10		
L, C				±5		±5		
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±50		±100	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}						nA	
J, K, L				±10		±50		
A, B, C				±10		±50		
S, T				±10		±200		
DYNAMIC PERFORMANCE[2]								R_L=100Ω, C_L=13pF
Current Settling Time	t_S			2		2	µs	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT}	F_T		5				mV p-p	V_{REF} = 10kHz, 20 Vp-p sinewave.
Propagation Delay	t_{PD}			300			ns	From 50% of digital input to 90% of final analog output current
REFERENCE INPUT								
Input Resistance	R_{IN}	7		25	7	25	kΩ	
DIGITAL INPUTS[3]								
Logical “1” Voltage	V_{IH}	2.4			2.4		V	
Logical “0” Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	
Input Capacitance[2]								
Data	C_{IN}			5		5	pF	
Control	C_{IN}			20		20	pF	

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
ANALOG OUTPUTS								
Output Capacitance[2]								
	C_{OUT}			200		200	pF	DAC Inputs all 1's
	C_{OUT}			70		70	pF	DAC Inputs all 0's
POWER SUPPLY[5]								
Functional Voltage Range	V_{DD}	5		15	5	15	V	
Supply Current	I_{DD}			2		2	mA	All digital inputs = 0 V or V_{DD}
SWITCHING CHARACTERISTICS[2, 4]								
Chip Select to Write Set-Up Time	t_{CS}	280	200		380	270 typ	ns	
Chip Select to Write Hold Time	t_{CH}	0			0		ns	
Data Valid to Write Set-Up Time	t_{DS}	140	100		210	150 typ	ns	
Data Valid to Write Hold Time	t_{DH}	10			10		ns	
Write Pulse Width	t_{WR}	250	175		400	280 typ	ns	

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
J, A, S				±2		±2		
K, B, T				±1		±1		
L, C				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	
J, A, S				±4		±4		
K, B, T				±1		±1		
L, C				±1		±1		
Gain Error	GE						LSB	Using Internal R_{FB}
J, A, S				±25		±25		
K, B, T				±15		±15		
L, C				±10		±10		
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±50		±100	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}						nA	
J, K, L				±10		±50		
A, B, C				±10		±50		
S, T				±10		±200		
DYNAMIC PERFORMANCE[2]								R_L=100Ω, C_L=13pF
Current Settling Time	t_S			2		2	µs	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT}	F_T		5				mV p-p	V_{REF} = 10kHz, 20 Vp-p sinewave.
Glitch Energy	Egl		250				nVs	V_{REF} = AGND
Propagation Delay	t_{PD}			250			ns	From 50% of digital input to 90% of final analog output current
REFERENCE INPUT								
Input Resistance	R_{IN}	7		25	7	25	kΩ	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	13.5			13.5		V	
Logical "0" Voltage	V_{IL}			1.5		1.5	V	
Input Leakage Current	I_{LKG}			±1		±10	µA	V_{IN} = 0 or V_{DD}
Input Capacitance[2]								
DB0-DB11	C_{IN}			5		5	pF	V_{IN} = 0
$\overline{WR}$, $\overline{CS}$	C_{IN}			20		20	pF	V_{IN} = 0

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
ANALOG OUTPUTS								
Output Capacitance[2]								
	C_{OUT}			200		200	pF	DAC Inputs all 1's
	C_{OUT}			70		70	pF	DAC Inputs all 0's
POWER SUPPLY[5]								
Functional Voltage Range	V_{DD}	5		15	5	15	V	
Supply Current	I_{DD}			2		2	mA	All digital inputs = 0 or V_{DD}
SWITCHING CHARACTERISTICS[2, 4]								
Chip Select to Write Set-Up Time	t_{CS}	180	120		200	150 typ	ns	
Chip Select to Write Hold Time	t_{CH}	0			0		ns	
Data Valid to Write Set-Up Time	t_{DS}	90	60		120	80 typ	ns	
Data Valid to Write Hold Time	t_{DH}	10			10		ns	
Write Pulse Width	t_{WR}	160	100		240	170 typ	ns	

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 0 to +17 V
Digital Input Voltage to GND .... GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND (2) ..... ±25 V
V_{RFB} to GND (2) ..... ±25 V
AGND to DGND ..... ±0.5 V

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC, PLCC 900mW
Derates above 75°C ..... 12mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3 GND refers to AGND and DGND.

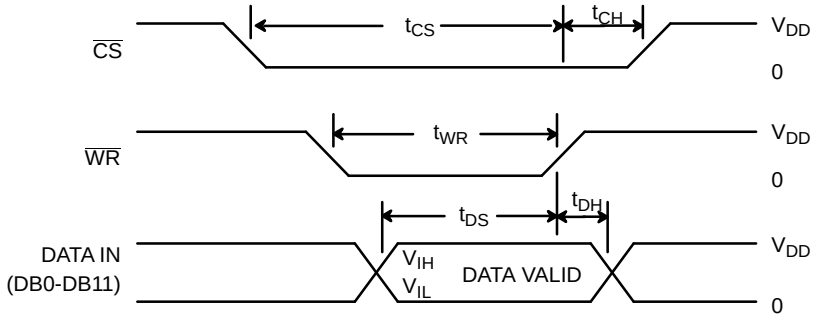


Figure 1. Write Cycle Timing Diagram

APPLICATION NOTES
Refer to Section 8 for Applications Information

Digital Section

Figure 2. shows the digital structure for one bit.

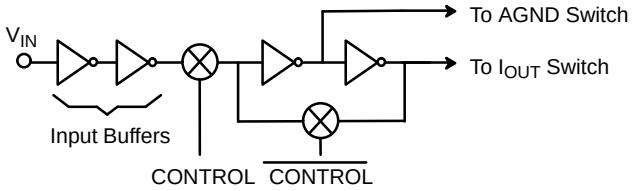


Figure 2. Digital Input Structure

The digital signals CONTROL and $\overline{CONTROL}$ are generated from $\overline{CS}$ and $\overline{WR}$.

The input buffers are simple CMOS inverters designed such that when the MP7545 is operated with V_{DD} = 5 V, the buffers convert TTL input levels (2.4 V and 0.8 V) into CMOS logic levels. When V_{IN} is in the region of 2.0 V to 3.5 V, the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The MP7545 may be operated with any supply voltage in the range $5 \leq V_{DD} \leq 15$ volts. With V_{DD} = +15 V the input logic levels are CMOS compatible only, i.e., 1.5 V and 13.5 V.

MICROPROCESSOR INTERFACING OF THE MP7545

The MP7545 can interface directly to both 8- and 16-bit microprocessors via its 12-bit wide data latch using standard $\overline{CS}$ and $\overline{WR}$ control signals.

A typical interface circuit for an 8-bit processor is shown in *Figure 3.* This arrangement uses two memory addresses, one for the lower 8 bits of data to the DAC and one for the upper 4 bits of data into the DAC via the latch.

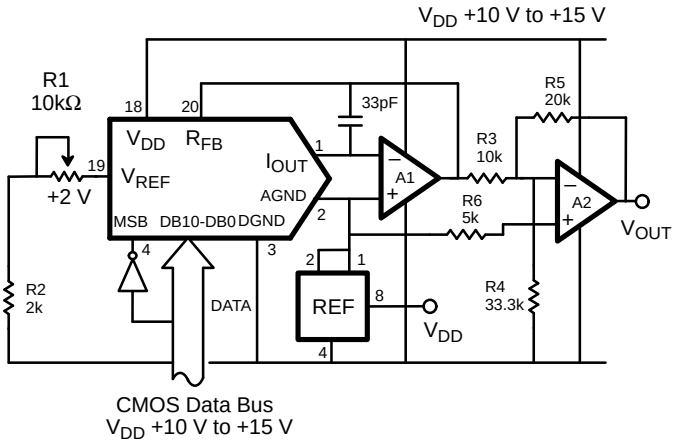


Figure 3. Single Supply "Bipolar" 2's Complement D/A Converter

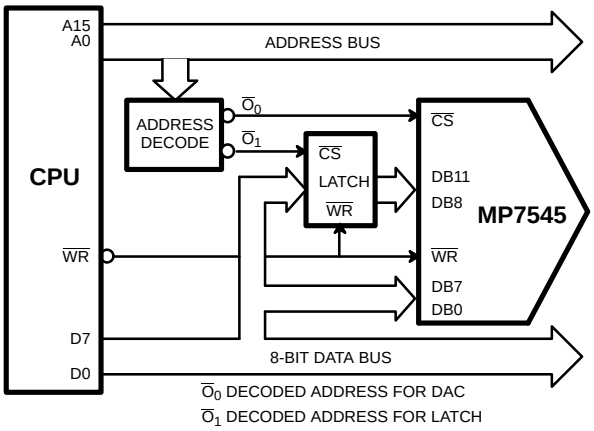


Figure 4. 8-Bit Processor to MP7545 Interface

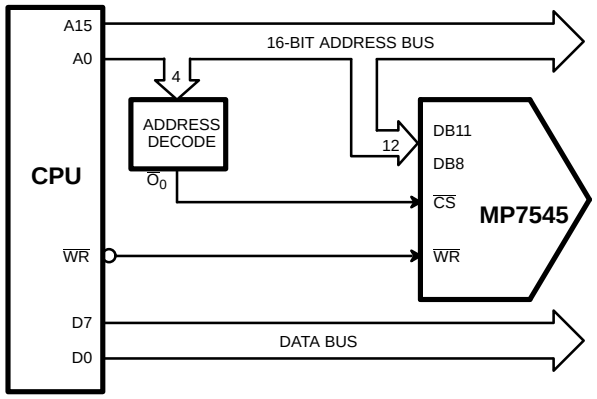
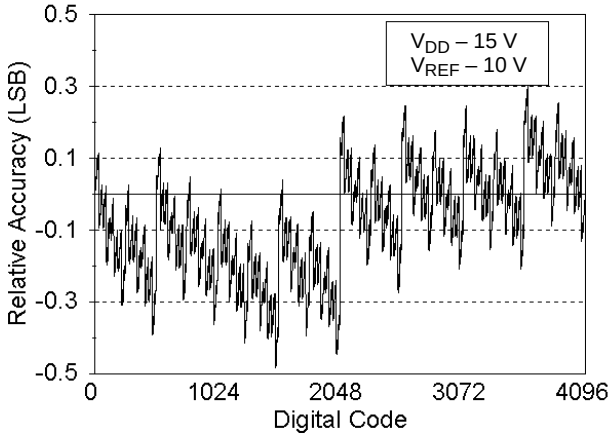


Figure 5. Connecting the MP7545 to 8-Bit Processors via the Address Bus

Figure 4. shows an alternative approach for use with 8-bit processors which have a full 16-bit wide address bus such as 6800, 8080, Z80. This technique uses the 12 lower address lines of the processor address bus to supply data to the DAC, thus each MP7545 connected in this way uses 4k bytes of address locations. Data is written to the DAC using a single memory write instruction. The address field of the instruction is organized so that the lower 12 bits contain the data for the DAC and the upper 4 bits contain the address of the 4k block at which the DAC resides.



Graph 1. Relative Accuracy vs. Digital Code

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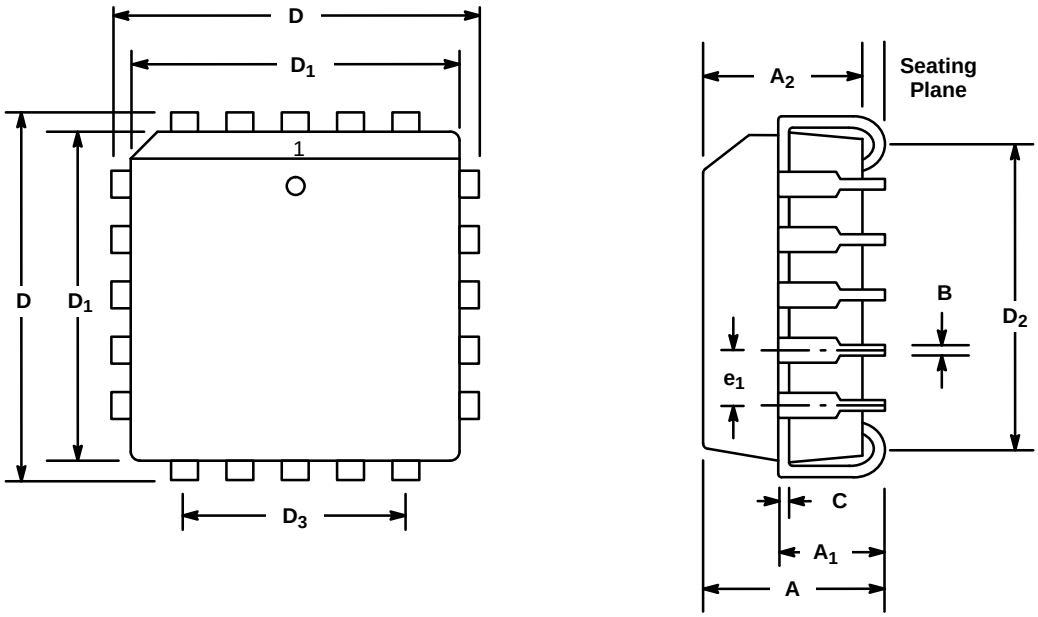
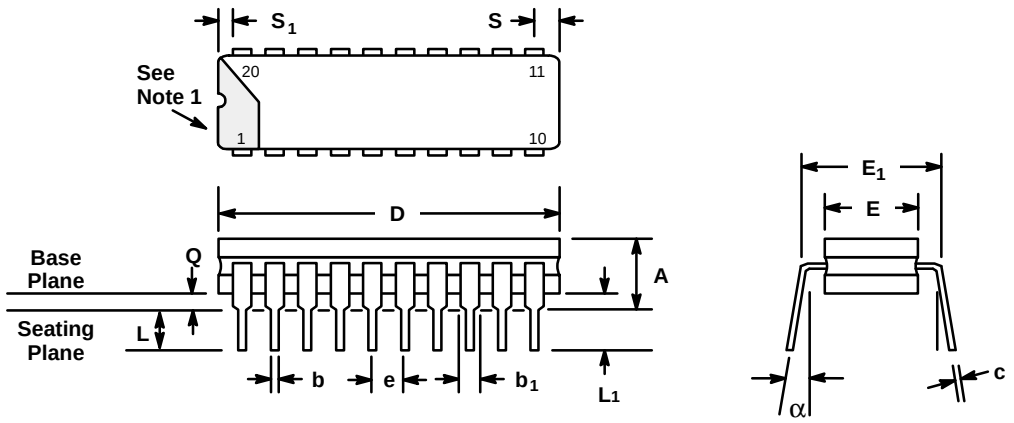
20 LEAD PLASTIC LEADED CHIP CARRIER (PLCC) P20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A_1	0.100	0.110	2.54	2.79
A_2	0.148	0.156	3.76	3.96
B	0.013	0.021	0.330	0.533
C	0.008	0.012	0.203	0.305
D	0.385	0.395	9.78	10.03
D_1 (1)	0.350	0.354	8.89	8.99
D_2	0.290	0.330	7.37	8.38
D_3	0.200 Ref		5.08 Ref.	
e_1	0.050 BSC		1.27 BSC	

Note: (1) Dimension D_1 does not include mold protrusion. Allowed mold protrusion is 0.254 mm/0.010 in.

20 LEAD CERAMIC DUAL-IN-LINE
(300 MIL CDIP)
D20

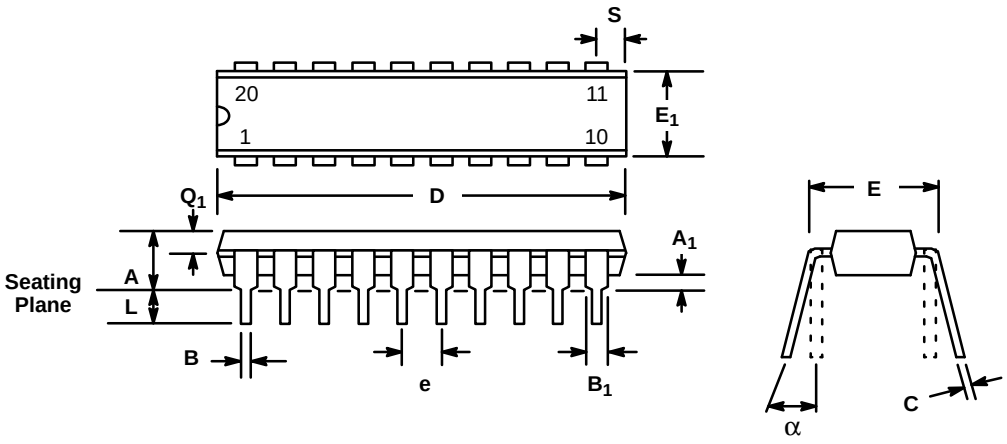


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	1.060	—	26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.070	0.381	1.78	3
S	—	0.080	—	2.03	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

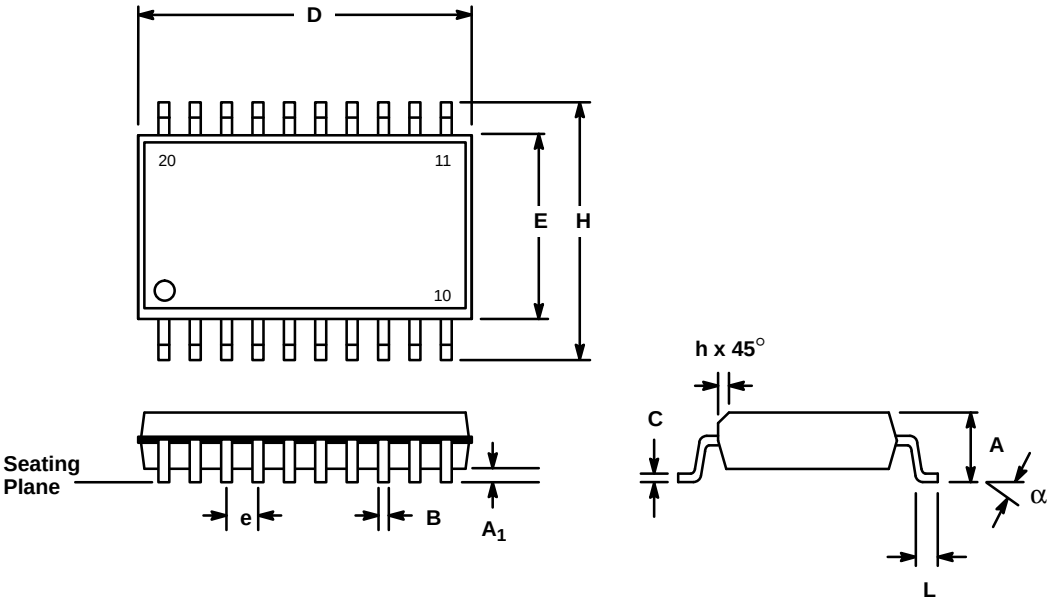
20 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.945	1.060	24.0	26.92
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.080	1.02	2.03

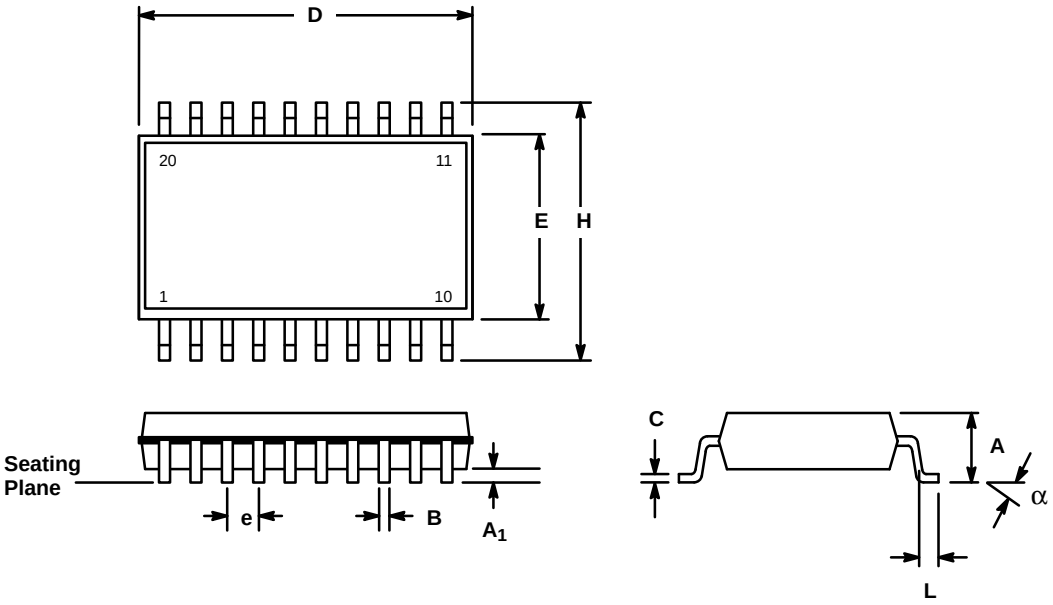
Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

20 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.642
A_1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.500	0.510	12.70	12.95
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

20 LEAD SHRINK SMALL OUTLINE PACKAGE (SSOP) A20



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.73	2.05	0.068	0.081
A_1	0.05	0.21	0.002	0.008
B	0.20	0.40	0.008	0.016
C	0.13	0.25	0.005	0.010
D	7.07	7.40	0.278	0.291
E	5.20	5.38	0.205	0.212
e	0.65 BSC		0.0256 BSC	
H	7.65	8.1	0.301	0.319
L	0.45	0.95	0.018	0.037
α	0°	8°	0°	8°

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