EXAR

FEATURES

- **Very Low Total Harmonic Distortion**
- **Lower Glitch Energy**
- **Four Quadrant Multiplication**
- **On-Chip Latches for Both DACs**
- **+10.8 V to +15.75 V Operation**
- **Low Power Consumption**
- **TTL/5V CMOS Compatible**
- **Latch-Up Free**
- **Second Source to AD7628**
- **5 V Operation: MP7529B**

BENEFITS

- **Quiet Operation in Audio Applications**
- **Easy Interface to Microprocessors**

GENERAL DESCRIPTION

The MP7529A is a dual 8-bit Digital-to-Analog Converter featuring excellent DAC-to-DAC matching, tracking and specifically optimized for applications requiring low total harmonic distortion. The MP7529A is manufactured using advanced thin film resistors on a double metal CMOS process. The MP7529A incorporates a unique decoding technique yielding lower glitch energy, higher speed and excellent accuracy over temperature and time.

Data is transferred to either of the two D/A Converter latches via a common 8-bit TTL/5 V CMOS compatible input port. The control input $\overline{DAC\ A}$/DAC B determines which DAC is to be loaded.

The device is specified for operation from +10.8 V to +15.75 V power supply, and is TTL-compatible over this range. Power dissipation is only 20 mW. Both DACs offer excellent four quadrant multiplication characteristics, and include separate reference inputs and feedback resistors. An improved latch-up resistant design eliminates the need for external protective Schottky diodes in most applications.

## SIMPLIFIED BLOCK AND TIMING DIAGRAM

MP7529A

EXAR
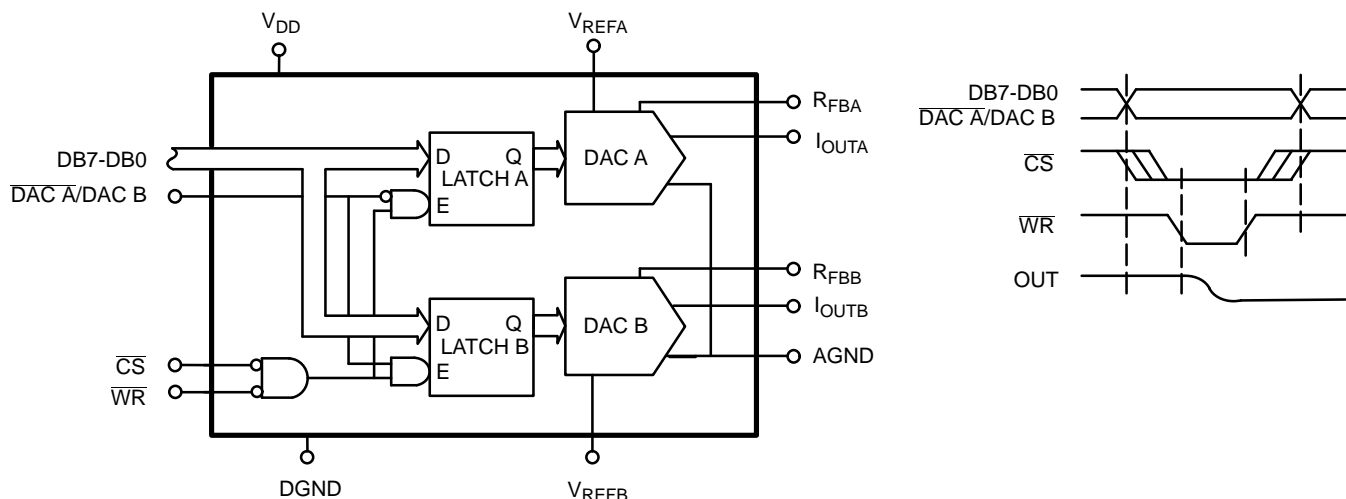
ORDERING INFORMATION

| Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	−40 to +85°C	MP7529AJN	±1	±1	±5
Plastic Dip	−40 to +85°C	MP7529AKN	±1/2	±1	±3
SOIC	−40 to +85°C	MP7529AJS	±1	±1	±5
SOIC	−40 to +85°C	MP7529AKS	±1/2	±1	±3
PLCC	−40 to +85°C	MP7529AJP	±1	±1	±5
PLCC	−40 to +85°C	MP7529AKP	±1/2	±1	±3

PIN CONFIGURATIONS   *See Packaging Section for Package Dimensions*
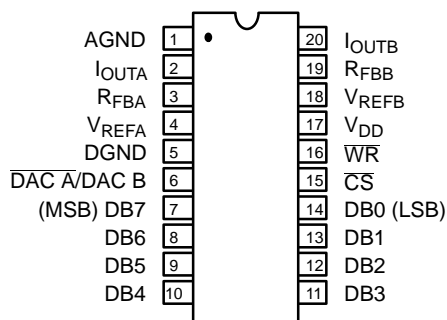
20 Pin PDIP (0.300")
N20
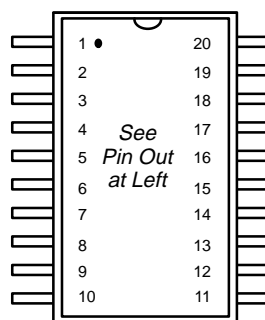
20 Pin SOIC (Jedec, 0.300")
S20
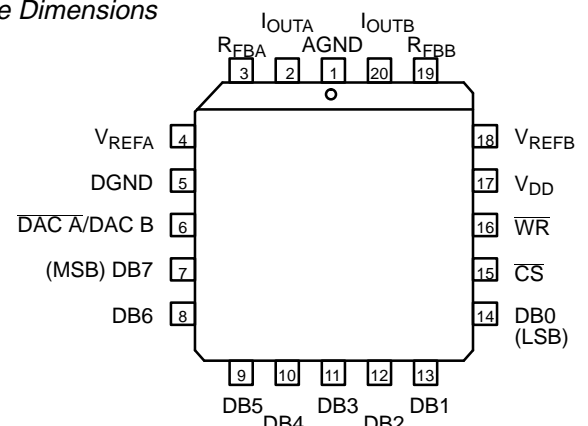
20 Pin PLCC
P20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	AGND	Analog Ground
2	I_{OUTA}	Current Output of DAC A
3	R_{FBA}	Internal Feedback Resistor of DAC A
4	V_{REFA}	Reference Input Voltage of DAC A
5	DGND	Digital Ground
6	$\overline{DAC\ A}/$ DAC B	DAC selection control
7	DB7	Data Input Input Bit 7 (MSB)
8	DB6	Data Input Bit 6
9	DB5	Data Input Bit 5
10	DB4	Data Input Bit 4

PIN NO.	NAME	DESCRIPTION
11	DB3	Data Input Bit 3
12	DB2	Data Input Bit 2
13	DB1	Data Input Bit 1
14	DB0	Data Input Bit 0 (LSB)
15	$\overline{CS}$	Chip Select (Active Low)
16	$\overline{WR}$	Write Enable (Active Low)
17	V_{DD}	Power Supply
18	V_{REFB}	Reference Input Voltage of DAC B
19	R_{FBB}	Internal Feedback Resistor of DAC B
20	I_{OUTB}	Current Output of DAC B

TXM

ELECTRICAL CHARACTERISTICS
(V_{DD} = +10.8 V to +15.75, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	8			8		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity Spec.
J				±1		±1		
K				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
J				±1		±1		
K				±1		±1		
Gain Error	GE						LSB	Using Internal R_{FB}
J				±4		±5		
K				±2		±3		
Gain Temperature Coefficient[2]	TC_{GE}		±15			±35	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±100		±200	ppm/%	$|\Delta Gain/\Delta V_{DD}|$, ΔV_{DD} = ± 5% V_{DD} = 10.8 V, ±5%, & 15.75 V ±5%
Output Leakage Current	I_{LKG}			±50		±200	nA	
DYNAMIC PERFORMANCE[2]								
Harmonic Distortion	THD		−95				dB	V_{IN} = 6V_{RMS} @ 1 kHz
Digital Crosstalk	Q		30				nVs	
AC Feedthrough	F_T						dB	
V_{REFA} to I_{OUTA}	F_{TA}		−70			−65	dB	
V_{REFB} to I_{OUTB}	F_{TB}		−70			−65	dB	
Channel-to-Channel Isolation	CCI						dB	
V_{REFA} to I_{OUTB}	C_{CIBA}		−77				dB	
V_{REFB} to I_{OUTA}	C_{CIAB}		−77				dB	
Glitch Energy	Egl		10				nVs	All zeros to all ones Input Change To 1/2 LSB, R_L=100Ω, C_{EXT}=13pF
Current Settling Time	t_S		200			250	ns	From 50% of digital input to 90% of final analog output current R_L=100Ω, C_{EXT}=13pF
Propagation Delay	t_{PD}		100			150	ns	
REFERENCE INPUT[1]								
Input Resistance	R_{IN}	8		15	8	15	kΩ	
Input Resistance Matching				±1		±1	%	
DIGITAL INPUTS[3]								
Logical "1" Voltage	V_{IH}	3.0	2.4		3.0		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±10	μA	
Input Capacitance[2]								
Data	C_{IN}			10		10	pF	
Control	C_{IN}			15		15	pF	

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
ANALOG OUTPUTS[2]								
Output Capacitance								
	$C_{OUTA/B}$			120		120	pF	DAC inputs all 1's
	$C_{OUTA/B}$			50		50	pF	DAC inputs all 0's
POWER SUPPLY[1]								
Supply Current	I_{DD}			1		1	mA	All digital inputs = 0 V, or all = 5 V
				2		2	mA	All digital inputs = V_{IL}, or all = V_{IH}
TIMING SPECIFICATIONS[4]								
Chip Select to Write Set-Up Time	t_{CS}	60			80		ns	
Chip Select to Write Hold Time	t_{CH}	15			20		ns	
DAC Select to Write Set-Up Time	t_{AS}	60			80		ns	
DAC Select to Write Hold Time	t_{AH}	15			20		ns	
Data Valid to Write Set-Up Time	t_{DS}	60			80		ns	
Data Valid to Write Hold Time	t_{DH}	0			0		ns	
Write Pulse Width[5]	t_{WR}	60			80		ns	

NOTES:

[1] Full Scale Range (FSR) is 10V for unipolar mode.

[2] Guaranteed but not production tested.

[3] Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.

[4] See timing diagram *Figure 1.*

[5] t_{WR} = 40ns minimum if t_{DH} > 15ns (@T = 25°C).

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND . . . . GND –0.5 to +17 V

AGND to DGND . . . . ±1 V
(Functionality Guaranteed ±0.5 V)

Digital Input Voltage to GND . . . . GND –0.5 V to +7 V

I_{OUTA}, I_{OUTB} to GND . . . . GND –0.5 V to +7 V

V_{REFA}, V_{REFB} to GND . . . . ±25 V

V_{RFBA}, V_{RFBB} to GND . . . . ±25 V

Storage Temperature . . . . –65°C to +150°C

Lead Temperature (Soldering, 10 seconds) . . . . . . +300°C

Package Power Dissipation Rating to 75°C
    PDIP, SOIC, PLCC 900mW
   Derates above 75°C . . . . 12mW/°C

NOTES:

[1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

[2] Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

[3] GND refers to AGND and DGND.

DIGITAL INTERFACE

The digital inputs are designed to be both TTL and 5 V CMOS compatible. All logic inputs are static protected MOS gates with typical input currents of less than 10nA.

The control input $\overline{\text{DAC A}}$/DAC B selects which DAC can accept data from the input port. Inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operating mode of the selected DAC (*Table 1.*). When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0-DB7 (Write mode). The selected DAC latch retains the data which was present on DB0-DB7 just prior to $\overline{\text{CS}}$ or $\overline{\text{WR}}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches (Hold mode).
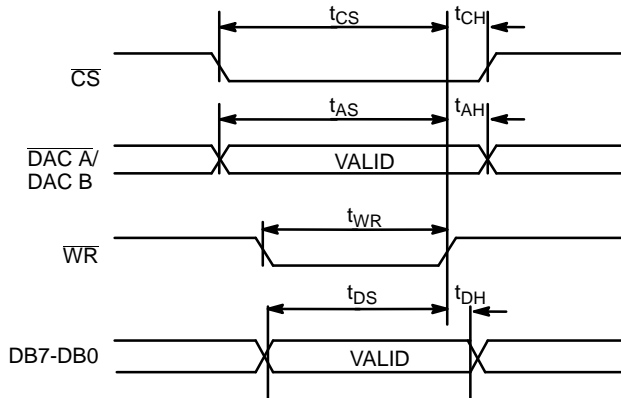
NOTE:
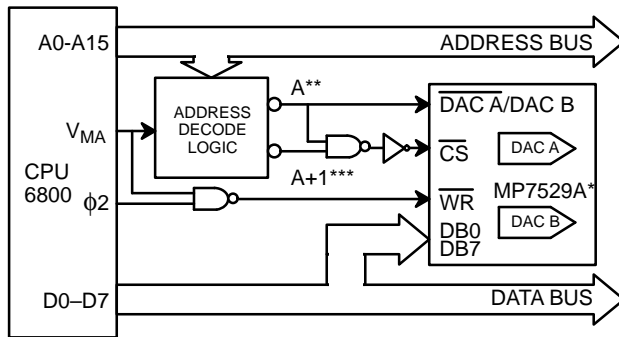1. Timing measured from $(V_{IH} + V_{IL})/2$

Figure 1. Write Cycle Timing Diagram

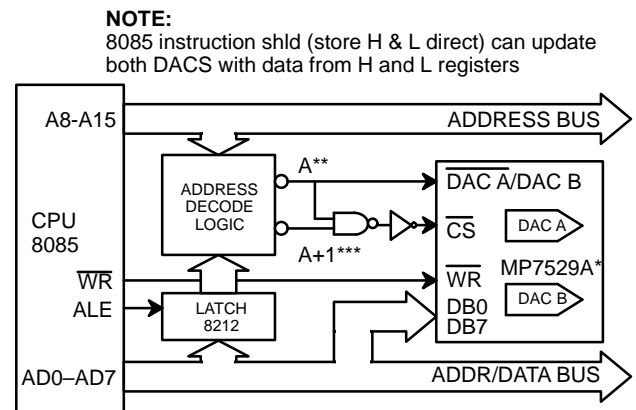| $\overline{\text{DAC A}}$/ DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State   H = High State   X = Don't Care

Table 1. DACs Mode Selection

MICROPROCESSOR INTERFACE

*Analog circuitry has been omitted for clarity
**A = Decoded 7529A DAC A Address
***A+1 = Decoded 7529A DAC B Address

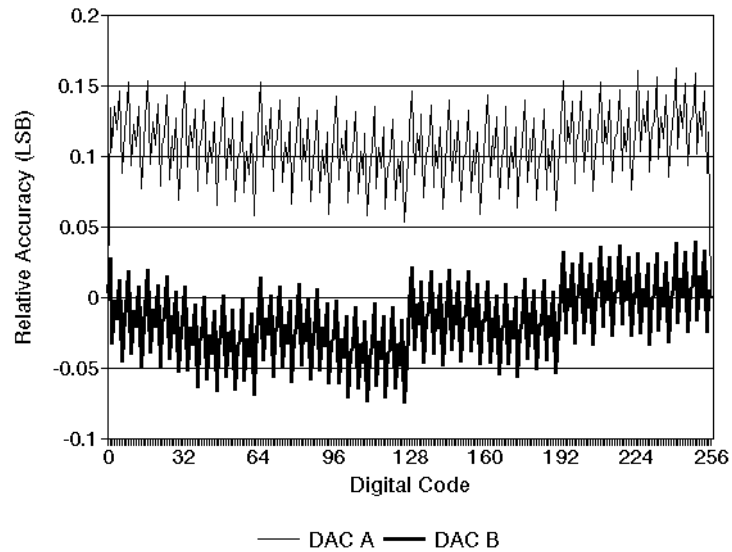**Figure 2. MP7529A Dual DAC to 6800 CPU Interface**

NOTE:
8085 instruction shld (store H & L direct) can update both DACS with data from H and L registers

*Analog circuitry has been omitted for clarity
**A = Decoded 7529A DAC A Address
***A+1 = Decoded 7529A DAC B Address

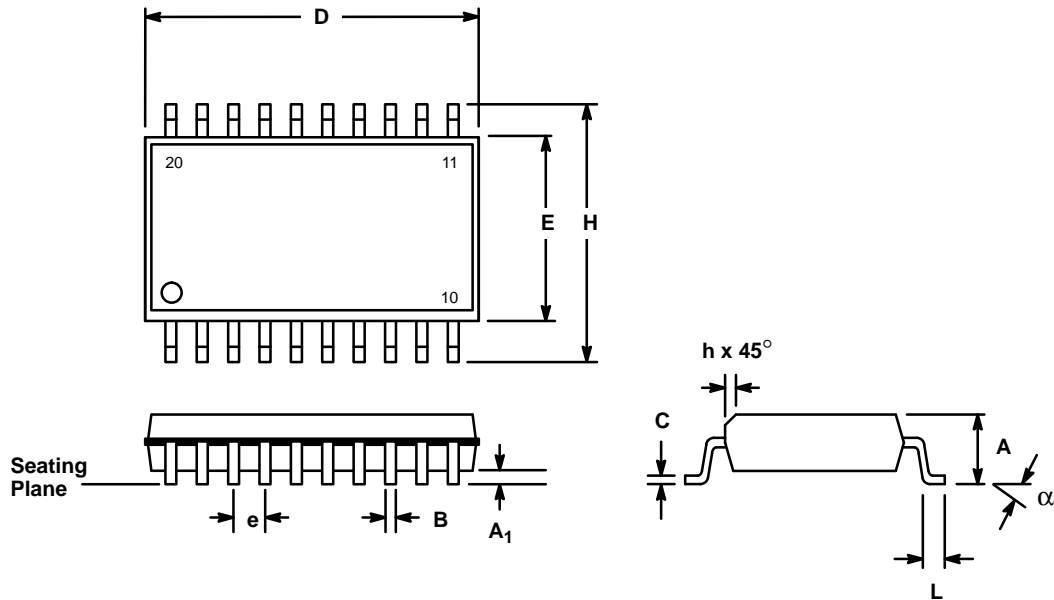**Figure 3. MP7529A Dual DAC to 8085 CPU Interface**

Graph 1. Relative Accuracy vs. Digital Code

APPLICATION NOTES
*Refer to Section 8 for Applications Information*

20 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S20

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.642
A_1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.500	0.510	12.70	12.95
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

20 LEAD PLASTIC LEADED CHIP CARRIER
(PLCC)
P20
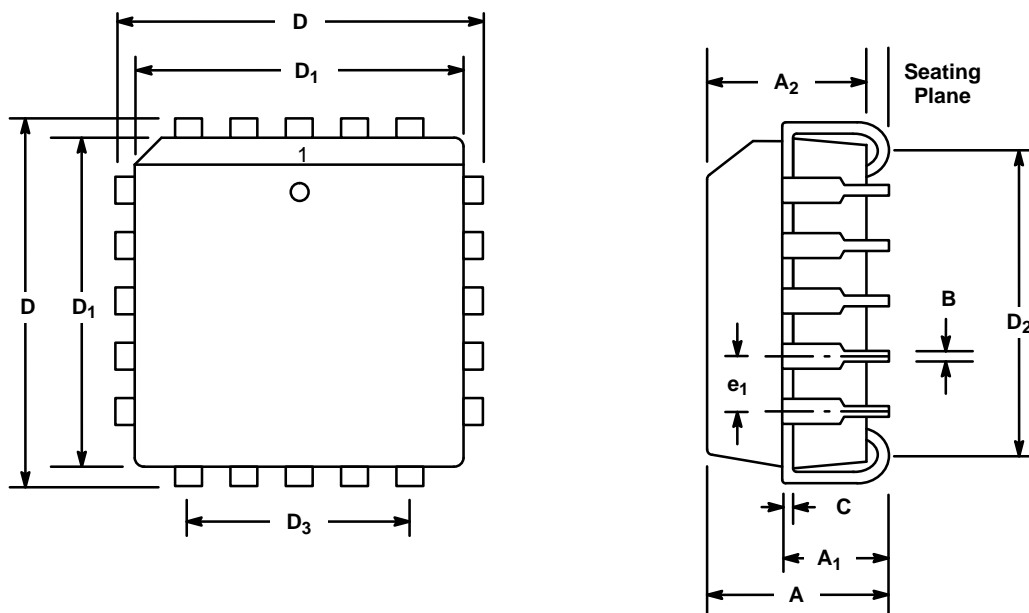
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A_1	0.100	0.110	2.54	2.79
A_2	0.148	0.156	3.76	3.96
B	0.013	0.021	0.330	0.533
C	0.008	0.012	0.203	0.305
D	0.385	0.395	9.78	10.03
D_1 (1)	0.350	0.354	8.89	8.99
D_2	0.290	0.330	7.37	8.38
D_3	0.200 Ref		5.08 Ref.	
e_1	0.050 BSC		1.27 BSC	

Note: (1) Dimension D_1 does not include mold protrusion.
Allowed mold protrusion is 0.254 mm/0.010 in.

**20 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N20**
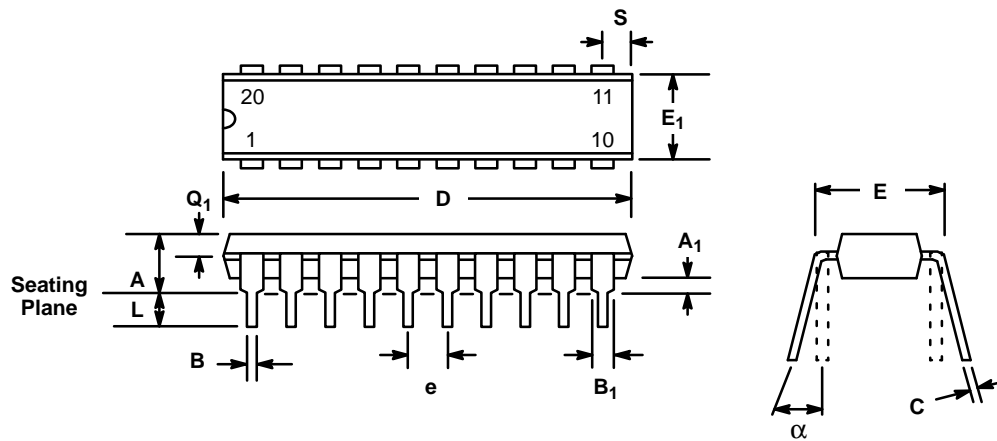
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.945	1.060	24.0	26.92
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.080	1.02	2.03

Note: (1) The minimum limit for dimensions B1 may be 0.023"
(0.58 mm) for all four corner leads only.

Notes

Notes

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