MP1230/31/32

Microprocessor Compatible
Double-Buffered 12-Bit
Digital-to-Analog Converter

FEATURES

- **Lower Data Bus Feedthrough @ $\overline{CS}$ = 1**
- **Stable, More Accurate Segmented DAC Approach**
- **Ultra Stable**
  - **0.2 ppm/°C Linearity Tempco**
  - **2 ppm/°C Max. Gain Error Tempco**
- **Low Sensitivity to Amplifier V_{OS}**
- **C_{OUT1} = 80 pF at Full Scale, Gives Fastest Settling Times and Larger, Stable Bandwidth**
- **Lower Glitch Energy**
- **Four Quadrant Multiplication**
- **Low Feedthrough Error**
- **Low Power Consumption**
- **TTL/5 V CMOS Compatible**
- **Latch-Up Free**
- **Use MP1230A/1231A/1232A for New Designs**

GENERAL DESCRIPTION

The MP1230/31/32 are 12-bit Digital-to-Analog Converters with 8/4 bit latched inputs for direct interface to the 8-bit data bus. All data loading and data transfer operations are identical to the WRITE cycle of a static RAM.

The MP1230 series uses a unique circuit which significantly reduces transients in the supplies during DATA bus transitions at $\overline{CS}$= 1.

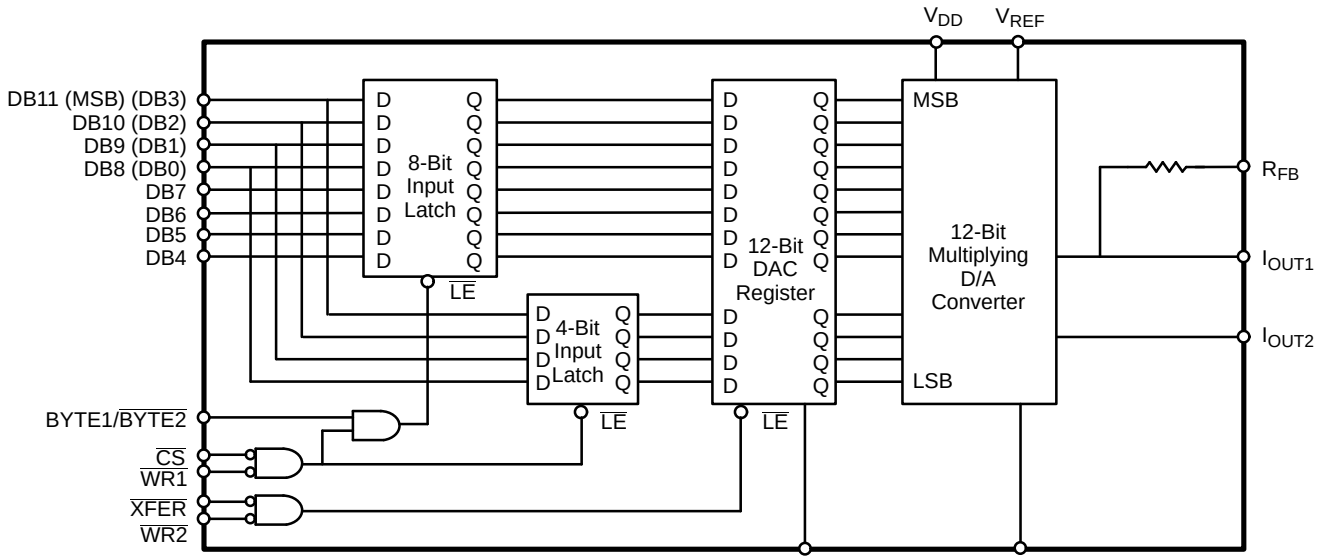
The MP1230 series is manufactured using advanced thin film resistors on a double metal CMOS process. The MP1230 series incorporates a unique decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. 12-bit linearity is achieved with minimal trimming. Outstanding features include:

– Stability: Both integral and differential linearity are rated at 0.2 ppm/°C typical, and monotonicity is guaranteed over the entire temperature range including the industrial and military ranges. Scale factor is a low 2 ppm/°C maximum.

– Low Output Capacitance: Due to smaller MOSFET switch geometries allowed by decoding, the output capacitance at I_{OUT1} is a low 80pF / 40pF and 25pF / 65 pF at I_{OUT2} for the conditions of full scale/zero . This is over twice less than the National DAC1230 Series. Lower capacitance allows the MP1230 series to achieve faster CMOS DAC settling times; less than 1 µsec for a 10 V step to 0.01% when utilizing a high speed output amplifier. Larger output amplifier bandwidths are available for a given amplifier loop gain because a smaller feedback “zero” compensating capacitor is required to offset the smaller I_{OUT} capacitance.

– Low Sensitivity to Output Amplifier Offset: 4 quadrant multiplying CMOS DACs provide an output current into the virtual ground of an op amp. The additional linearity error incurred by amplifier offset is reduced by a factor of 2 in the MP1208/1230 series over conventional R-2R DACs, to 330µV per millivolt of offset.

SIMPLIFIED BLOCK DIAGRAM



When $\overline{LE}$ = 1, Q outputs follow D inputs.

When $\overline{LE}$ = 0, Q outputs are latched.

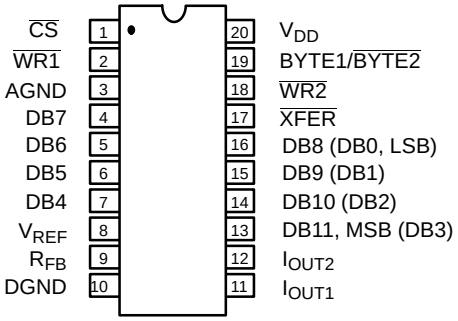
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP1231JN	±1	±1	±0.4
Plastic Dip	–40 to +85°C	MP1230KN	±1/2	±3/4	±0.4
Plastic Dip	–40 to +85°C	MP1232HN	±2	±2	±0.4
SOIC	–40 to +85°C	MP1231JS	±1	±1	±0.4
Ceramic Dip	–40 to +85°C	MP1231AD	±1	±1	±0.4
Ceramic Dip	–40 to +85°C	MP1230BD	±1/2	±3/4	±0.4
Ceramic Dip	–40 to +85°C	MP1232ZD	±2	±2	±0.4
Ceramic Dip	–55 to +125°C	MP1231SD*	±1	±1	±0.4

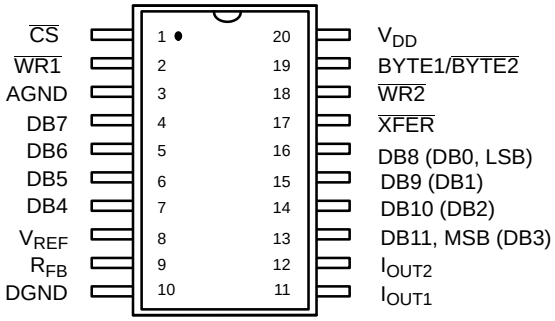
*Contact factory for non-compliant military processing

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



20 Pin CDIP, PDIP (0.300")
D20, N20



20 Pin SOIC (Jedec, 0.300")
S20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	$\overline{CS}$	Chip Select (Active Low)
2	$\overline{WR1}$	Write 1 (Active Low)
3	AGND	Analog Ground
4	DB7	Data Input Bit 7
5	DB6	Data Input Bit 6
6	DB5	Data Input Bit 5
7	DB4	Data Input Bit 4
8	V_{REF}	Reference Input Voltage
9	R_{FB}	Internal Feedback Resistor
10	DGND	Digital Ground
11	I_{OUT1}	Current Output 1
12	I_{OUT2}	Current Output 2
13	DB11 (DB3)	Data Input Bit 9 (MSB)
14	DB10 (DB2)	Current Output 10
15	DB9 (DB1)	Data Input Bit 9
16	DB8 (DB0)	Data Input Bit 8 (LSB)
17	$\overline{XFER}$	Transfer Control Signal (Active Low)
18	$\overline{WR2}$	Write 2 (Active Low)
19	BYTE1/ $\overline{BYTE2}$	Byte Sequence Control
20	V_{DD}	Positive Power Supply

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	12			12			Bits
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
MP1230				±1/2		±1/2		
MP1231				±1		±1		
MP1232				±2		±2		
Differential Non-Linearity	DNL						LSB	
MP1230				±3/4		±3/4		
MP1231				±1		±1		
MP1232				±2		±2		
Gain Error	GE		±0.1	±0.4		±0.4	% FSR	Using Internal R_{FB}
Gain Temperature Coefficient[2]	TC_{GE}		1			±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR		5	±20		±20	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{OUT}		1	±10		±200	nA	
DYNAMIC PERFORMANCE[2]								R_L=100Ω, C_L=13pF
Current Settling Time	t_S		1.0				µs	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT1}	F_T		1.0				mV p-p	V_{REF}=100kHz, 20Vp-p, sinewave
REFERENCE INPUT								
Input Resistance	R_{IN}	5	10	20	5	20	kΩ	
DIGITAL INPUTS[3]								
Logical “1” Voltage	V_{IH}	3.0	2.4		3.0		V	
Logical “0” Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}		0.1	±1		±1	µA	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}		80	100			pF	DAC Inputs all 1’s
	C_{OUT1}		40	60			pF	DAC Inputs all 0’s
	C_{OUT2}		65	85			pF	DAC Inputs all 1’s
	C_{OUT2}		25	45			pF	DAC Inputs all 0’s
POWER SUPPLY								
Functional Voltage Range[5]	V_{DD}	4.5	15	16			V	
Supply Current	I_{DD}		1.2	2		2	mA	All digital inputs = 0 V or all = 5 V

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
SWITCHING CHARACTERISTICS[2, 4]								
$\overline{WR}$, $\overline{XFER}$ Pulse Width	t_{WR}	100	50				ns	
Data Set-Up Time	t_{DS}	100	50				ns	
Data Hold Time	t_{DH}	90	70				ns	
$\overline{CS}$ Set-Up Time	t_{CS}	200	100				ns	
$\overline{CS}$ Hold Time	t_{CH}	10	0				ns	

NOTES:

1 Full Scale Range (FSR) is 10V.
2 Guaranteed but not production tested
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See switching waveforms
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +17 V
Digital Input Voltage to GND .... GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V
AGND to DGND ..... ±1 V
(Functionality Guaranteed ±0.5 V)

Storage Temperature ..... –65°C to +150°C

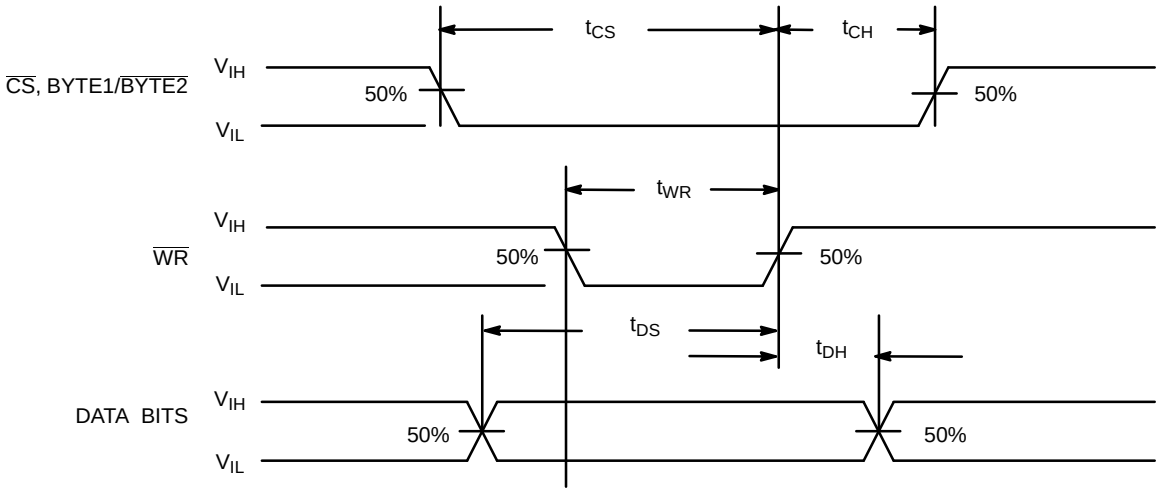
Lead Temperature (Soldering, 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC 900mW
Derates above 75°C ..... 12mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3 GND refers to AGND and DGND.

SWITCHING WAVEFORMS



DEFINITION OF CONTROL SIGNALS:

$\overline{CS}$: Chip Select.(Active low)
It will enable $\overline{WR1}$.

$\overline{WR1}$: Write 1 (Active low)
The $\overline{WR1}$ is used to load the digital data bits (DB) into the input latch.

BYTE1/$\overline{BYTE2}$: Byte sequence control.
The BYTE1/$\overline{BYTE2}$ control pin is used to select both MSB and LSB input latches.

$\overline{WR2}$: Write 2 (Active low)
It will enable $\overline{XFER}$.

$\overline{XFER}$: Transfer control signal (Active low)
This signal in combination with $\overline{WR2}$ causes the 16-bit data which is available in the input latches to transfer to the DAC register

DB0 to DB11: Digital Inputs.
DB0 is the least significant digital input (LSB) and DB11 is the most significant digital input (MSB).

I_{OUT1}: DAC Current Output 1 Bus.
I_{OUT1} is a maximum for a digital code of all 1's in the DAC register, and is zero for all 0's in the DAC register.

I_{OUT2}: DAC Current Output 2 Bus.
I_{OUT2} is a complement of I_{OUT1}.

R_{FB}: Feedback Resistor.
This internal feedback resistor should always be used (not an external resistor) since it matches the resistors in the DAC and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input.
This input connects an external precision voltage source to the internal DAC. The V_{REF} can be selected over the range of +25V to –25V or the analog signal for a 4-quadrant multiplying mode application.

V_{DD}: Power Supply Voltage.
This is the power supply pin for the part. The V_{DD} can be from +5 V DC to +15 V DC, however optimum voltage is +12 to +15 V DC.

AGND: Analog Ground
Back gate of the DAC N-channel current steering switches.

DGND: Digital Ground

APPLICATION NOTES

Refer to Section 8 for Applications Information

The MP1230 series allows direct interface to microprocessor system buses without the need for additional interface circuitry. They provide 8 data input lines in parallel for optimum interface to a 16-bit data bus, but can be mapped onto an 8-bit bus by tying lines DB0 through DB3 to lines DB8 through DB11, respectively.

All digital inputs maintain TTL compatibility over the entire range of V_{DD}. The internal latches are level-triggered, and therefore can be hardwired for transparent operation. The MP1208 series can be wired for a single layer of buffering by tying the 12-bit DAC register transparent (ground $\overline{XFER}$ and $\overline{WR2}$) or by tying the 8-bit and 4-bit latch transparent (ground $\overline{CS}$, $\overline{WR1}$, BYTE1/$\overline{BYTE2}$ = V_{DD}). In non-microprocessor applications, the MP1230 series can be wired for flow-through operation. The analog output will continuously reflect the state of the digital inputs by tying the 8-bit latch, 4-bit latch, and 12-bit DAC register transparent.

Double-buffering provides the user with the capability of refreshing simultaneously all 12 data bits to the DAC from an 8-bit data bus. Double-buffering also allows a single DAC or several DACs to be updated from the same data bus at the same time. This will be done asynchronously by an external monitoring device (such as a voltage comparator) or by a system interrupt. In this example, tie $\overline{WR2}$ low and use the $\overline{XFER}$ to update the 12-bit register.

For a two byte load, tie BYTE1/$\overline{BYTE2}$ and $\overline{XFER}$ together and $\overline{WR1}$ and $\overline{WR2}$ together. The first write will update the 8-bit input latch (the 4-bit latch is also changed). The second write will overwrite the 4-bit latch and transfer all 12 bits to the 12-bit DAC register, updating the DAC. (*See Typical Application*.)

Use the high order address lines for the device select ($\overline{CS}$). Normally the low order address lines (A0, A1) will be decoded for BYTE1/$\overline{BYTE2}$ and $\overline{XFER}$. The $\overline{XFER}$ input can be decoded independently (3 write loads) when independent control is desired.

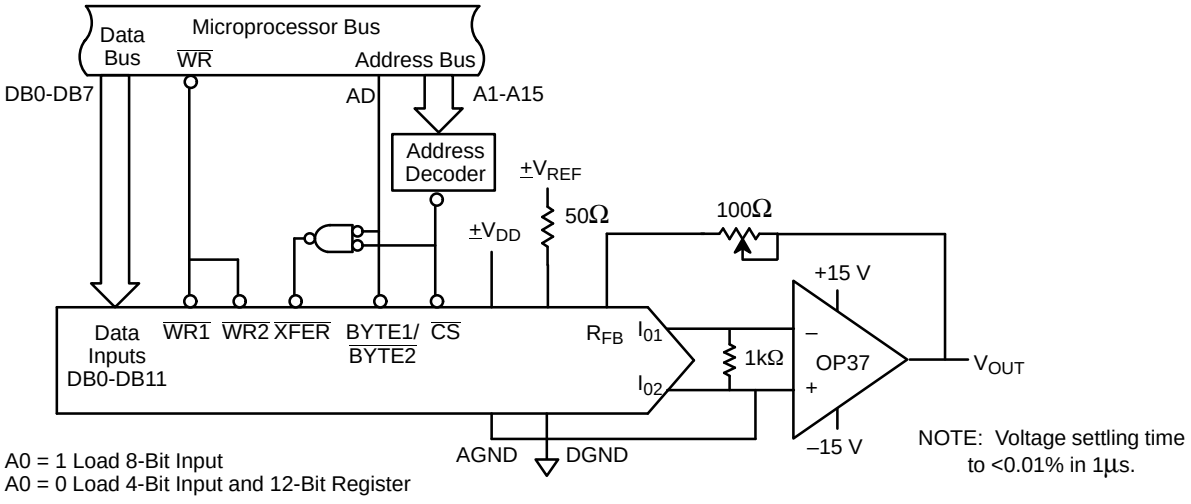
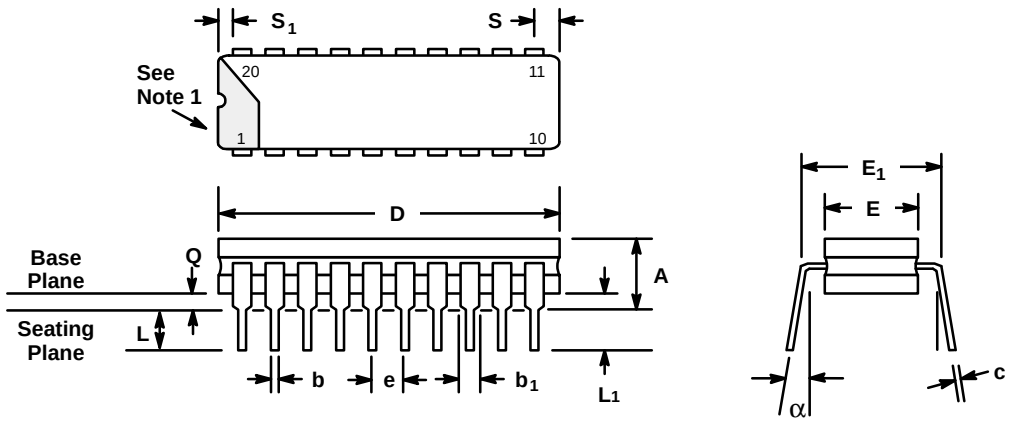


Figure 1. Two Write Load / Unipolar Configuration

20 LEAD CERAMIC DUAL-IN-LINE
(300 MIL CDIP)
D20

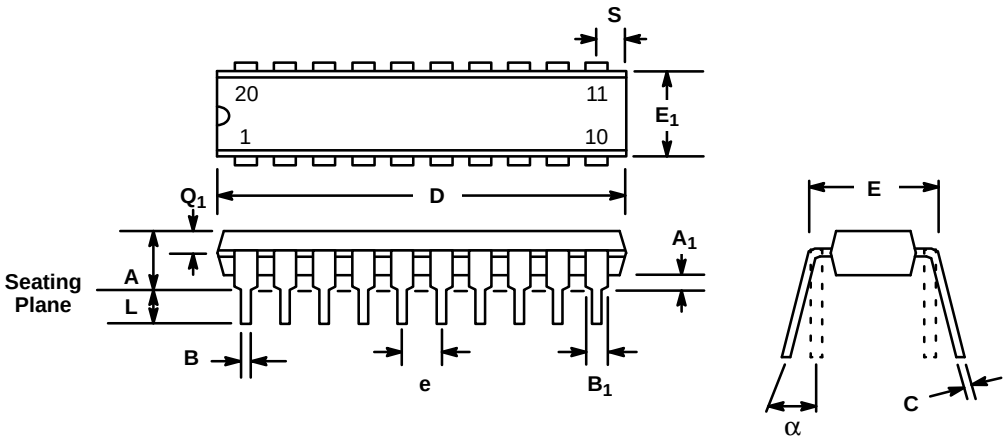


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	1.060	—	26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.070	0.381	1.78	3
S	—	0.080	—	2.03	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

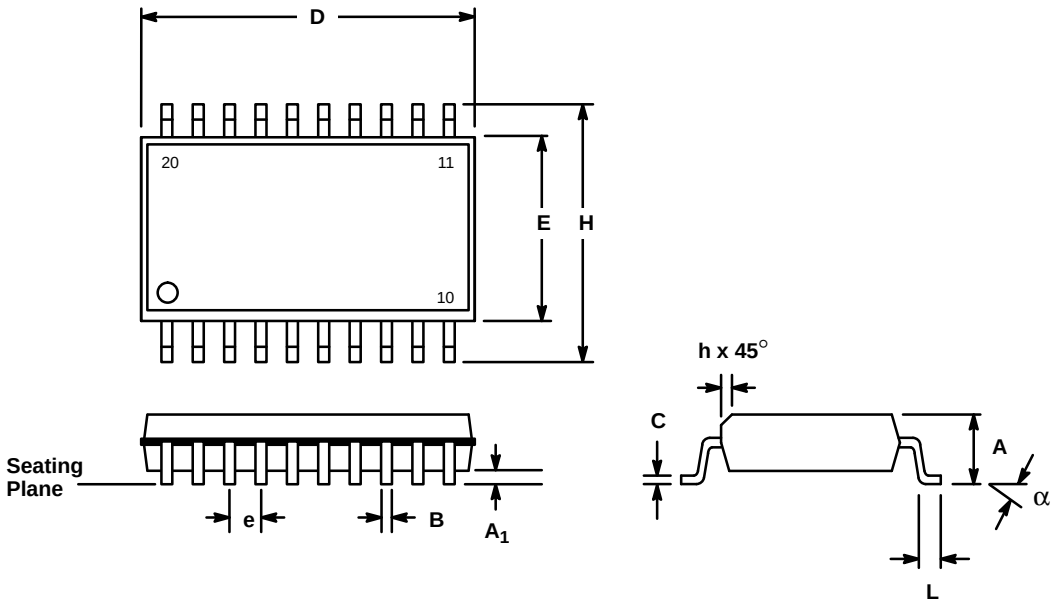
20 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.945	1.060	24.0	26.92
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.080	1.02	2.03

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

20 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.642
A_1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.500	0.510	12.70	12.95
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

Notes

NOTICE

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