MP1208/9/10

Microprocessor Compatible
Double-Buffered, 12-Bit
Digital-to-Analog Converter

FEATURES

- **Lower Data Bus Feedthrough @ $\overline{CS}$ = 1**
- **Stable, More Accurate Segmented DAC Approach**
- **Ultra Stable**
  - **0.2 ppm/°C Linearity Tempco**
  - **2 ppm/°C Max Gain Error Tempco**
- **Low Sensitivity to Amplifier V_{OS}**
- **Low Output Capacitance**
- **C_{OUT1} = 80 pF at Full Scale, Gives Fastest Settling Times, and Larger Stable Bandwidth capability**
- **Lower Glitch Energy**
- **Four Quadrant Multiplication**
- **All Parts guaranteed 12-Bit Monotonic**
- **Low Feedthrough Error**
- **Low Power Consumption**
- **TTL/5 V CMOS Compatible**
- **Latch-Up Free**
- **–55°C to +125°C Operation**
- **8-Bit Bus Version: MP1230A/1231A/1232A**

GENERAL DESCRIPTION

The MP1208/09/10 series are 12-bit Digital-to-Analog Converters with an 8/4 bit latched input interface that provide maximum flexibility in interfacing to µP data bus. All data loading and data transfer operations are identical to the WRITE cycle of a static RAM.

The MP1208 series use a unique circuit which significantly reduces transients in the supplies during DATA bus transitions at $\overline{CS}$ = 1.

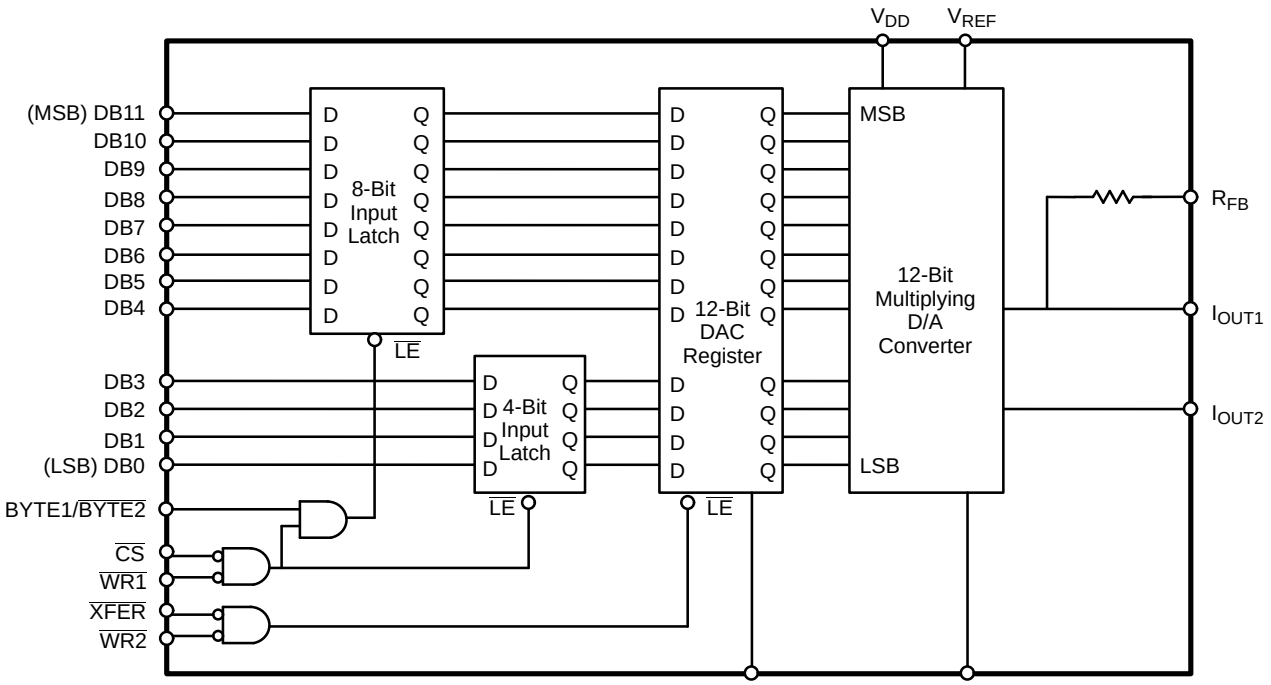
The MP1208 series are manufactured using advanced thin film resistors on a double metal CMOS process. The MP1208 series incorporates a unique bit decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. 12-bit linearity is achieved with minimal trimming. Outstanding features include:

– Stability: Both integral and differential linearity are rated at 0.2 ppm/°C typical, and monotonicity is guaranteed over the entire temperature range including the industrial (–40 to +85°C) and military ranges. Scale factor is a low 2 ppm/°C maximum.

– Low Output Capacitance: Due to smaller MOSFET switch geometries allowed by decoding, the output capacitance at I_{OUT1} and I_{OUT2} are a low 80pF / 40pF and 25pF / 65 pF for the conditions of full/zero scale. This is over two times less than the National DAC 1208 Series. Lower capacitance allows the MP1208 series to achieve faster CMOS DAC settling times; less than 1 µsec for a 10 V step to 0.01% when utilizing a high speed output amplifier. Larger output amplifier bandwidths are available, for a given amplifier loop gain, because a smaller feedback “zero” compensating capacitor is required to offset the smaller I_{OUT} capacitance.

– Low Sensitivity to Output Amplifier Offset: 4 quadrant multiplying CMOS DACs provide an output current into the virtual ground of an op amp. The additional linearity error incurred by amplifier offset is reduced by a factor of 2 in the MP1208 series over conventional R-2R DACs, to 330µV per millivolt of offset.

SIMPLIFIED BLOCK DIAGRAM



When $\overline{LE}$ = 1, Q outputs follow D inputs.

When $\overline{LE}$ = 0, Q outputs are latched.

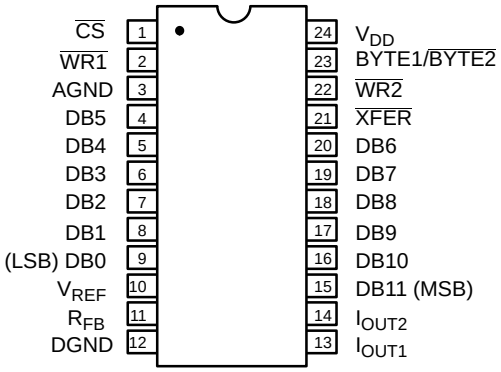
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP1210HN	±2	±2	±0.4
Plastic Dip	–40 to +85°C	MP1209JN	±1	±1	±0.4
Plastic Dip	–40 to +85°C	MP1208KN	±1/2	±3/4	±0.4
Ceramic Dip	–40 to +85°C	MP1208BD	±1/2	±3/4	±0.4
Ceramic Dip	–55 to +125°C	MP1208TD*	±1/2	±3/4	±0.4
Ceramic Dip	–40 to +85°C	MP1209AD	±1	±1	±0.4
Ceramic Dip	–55 to +125°C	MP1209SD*	±1	±1	±0.4
Ceramic Dip	–55 to +125°C	MP1210RD*	±2	±2	±0.4

*Contact factory for non-compliant military processing

PIN CONFIGURATION

See Packaging Section for Package Dimensions



24 Pin CDIP, PDIP (0.600")
D24, N24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	$\overline{CS}$	Chip Select (Active Low)
2	$\overline{WR1}$	Write1 (Active Low)
3	AGND	Analog Ground
4	DB5	Data Input Bit 5
5	DB4	Data Input Bit 4
6	DB3	Data Input Bit 3
7	DB2	Data Input Bit 2
8	DB1	Data Input Bit 1
9	DB0	Data Input Bit 0 (LSB)
10	V_{REF}	Reference Input Voltage
11	R_{FB}	Internal Feedback Resistor
12	DGND	Digital Ground
13	I_{OUT1}	Current Output 1
14	I_{OUT2}	Current Output 2
15	DB11	Data Input Bit 11 (MSB)
16	DB10	Data Input Bit 10
17	DB9	Data Input Bit 9
18	DB8	Data Input Bit 8
19	DB7	Data Input Bit 7
20	DB6	Data Input Bit 6
21	$\overline{XFER}$	Transfer Control Signal (Active Low)
22	$\overline{WR2}$	Write 2 (Active Low)
23	BYTE1/ $\overline{BYTE2}$	Byte Sequence Control
24	V_{DD}	Positive Power Supply

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
MP1208				±1/2		±1/2		
MP1209				±1		±1		
MP1210				±2		±2		
Differential Non-Linearity	DNL						LSB	
MP1208				±3/4		±3/4		
MP1209				±1		±1		
MP1210				±2		±2		
Gain Error	GE		±0.1	±0.4		±0.4	% FSR	Using Internal R_{FB}
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR			±50		±50	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ±5%
Output Leakage Current	I_{OUT}	–10	1	10		±200	nA	
DYNAMIC PERFORMANCE[2]								RL=100Ω, CL=13pF
Current Settling Time	t_S		1				µs	Full Scale Change to 1/2 LSB R_L = 100Ω
AC Feedthrough at I_{OUT1}	FT		1				mV p-p	V_{REF}=100kHz, 20 Vp-p, sinewave
REFERENCE INPUT								
Input Resistance	R_{IN}	5	10	20	5	20	kΩ	
V_{IN}[2]			±10	±25			V	
DIGITAL INPUTS								
Logical “1” Voltage	V_{IH}	3.0	2.4		3.0		V	
Logical “0” Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}	–1	0.1	1		±1	µA	V_{IN} = 0 or V_{DD}
ANALOG OUTPUTS								
Output Capacitance[2]								
	C_{OUT1}		80	100			pF	DAC Inputs all 1’s
	C_{OUT1}		40	60			pF	DAC Inputs all 0’s
	C_{OUT2}		65	85			pF	DAC Inputs all 0’s
	C_{OUT2}		25	45			pF	DAC Inputs all 1’s
POWER SUPPLY								
Functional Voltage Range[5]	V_{DD}	4.5	15	16	4.5	16	V	
Supply Current	I_{DD}		1.2	2.0		2.0	mA	All digital inputs = 0 V or all = 5 V

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
SWITCHING CHARACTERISTICS[2, 4]								
Write and $\overline{XFER}$ Pulse Width	t_{WR}	100	50				ns	
Data Set-Up Time	t_{DS}	100	50				ns	
Data Hold Time	t_{DH}	90	70				ns	
Control Set-Up Time	t_{CS}	200	100				ns	
Control Hold Time	t_{CH}	10	0				ns	

NOTES:

1 Full Scale Range (FSR) is 10V.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... 0 to +17 V
Digital Input Voltage to GND .... GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V
AGND to DGND ..... ±1 V
(Functionality Guaranteed ±0.5 V)

Storage Temperature ..... –65°C to +150°C

Lead Temperature (Soldering, 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C
CDIP, PDIP 1150mW
Derates above 75°C ..... 15mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3 GND refers to AGND and DGND.

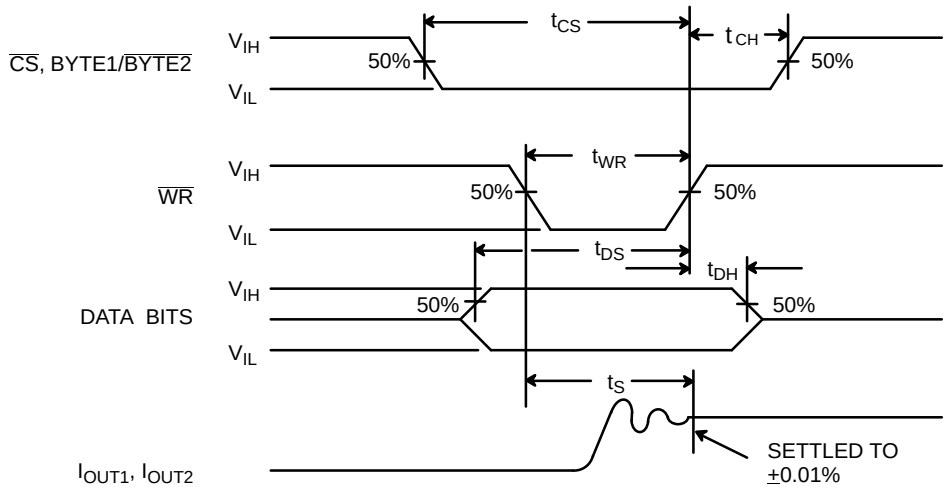


Figure 1. Timing Diagram

APPLICATION NOTES
Refer to Section 8 for Applications Information

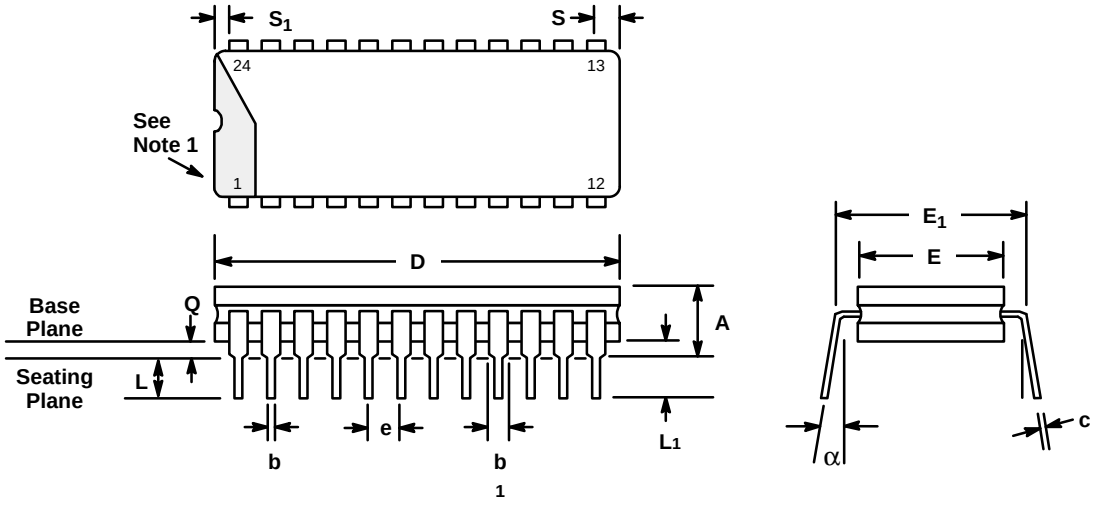
The MP1208 series allows direct interface to microprocessor system buses without the need for additional interface circuitry. They also provide all 12 data input lines in parallel for optimum interface to a 16-bit data bus, but can be mapped onto an 8-bit bus by tying lines DB0 through DB3 to lines DB8 through DB11, respectively.

All digital inputs maintain TTL compatibility over the entire range of V_{DD}. The internal latches are lever-triggered, and therefore can be hardwired for transparent operation. The MP1208 series can be wired for a single layer of buffering by tying the 12 bit DAC register transparent (ground $\overline{XFER}$ and $\overline{WR2}$) or by tying the 8-bit and 4-bit latch transparent (ground $\overline{CS}$, $\overline{WR1}$, BYTE1/$\overline{BYTE2}$ = V_{DD}). In non-microprocessor applications, the MP1208 series can be wired for flow-through operation. The analog output will continuously reflect the state of the digital inputs by tying the 8-bit latch, 4-bit latch, and 12-bit DAC register transparent.

Double-buffering provides the user with the capability of refreshing simultaneously all 12 data bits to the DAC from an 8-bit data bus. Double-buffering also allows a single DAC or several DACs to be updated from the same data bus at the same time. This will be done asynchronously by an external monitoring device (such as a voltage comparator) or by a system interrupt. In this example, tie $\overline{WR2}$ low and use the $\overline{XFER}$ to update the 12-bit register.

For a two byte load, tie BYTE1/$\overline{BYTE2}$ and $\overline{XFER}$ together and $\overline{WR1}$ and $\overline{WR2}$ together. The first write will update the 8-bit input latch (the 4-bit latch is also changed). The second write will overwrite the 4-bit latch and transfer all 12 bits to the 12-bit DAC register, updating the D/A converter. (See *Typical Application*.)

24 LEAD CERAMIC DUAL-IN-LINE
(600 MIL CDIP)
D24

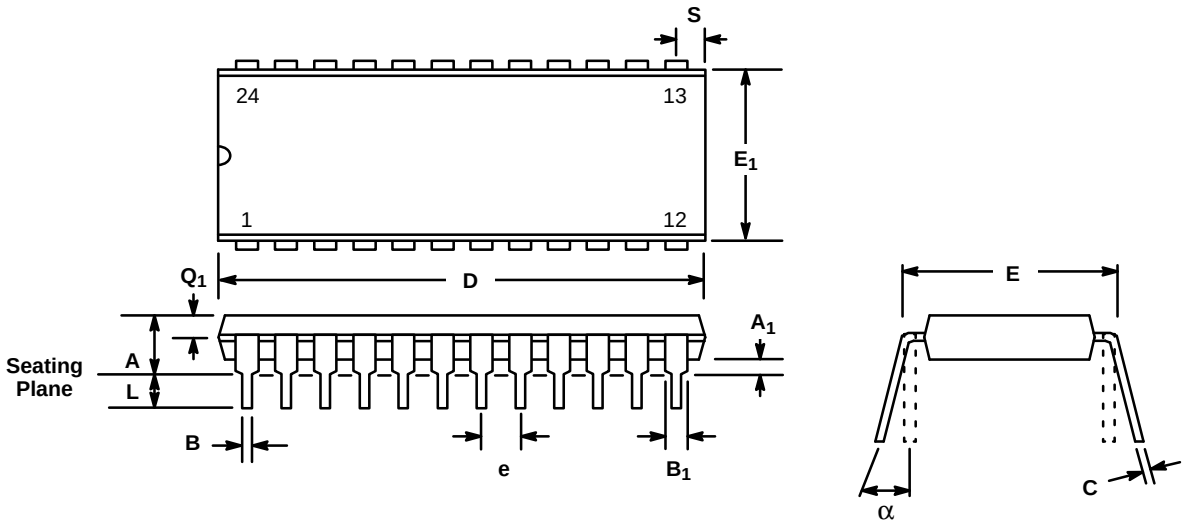


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	—	0.225	—	5.72	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	1.290	—	32.77	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.120	0.200	3.05	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.075	0.381	1.91	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

24 LEAD PLASTIC DUAL-IN-LINE
(600 MIL PDIP)
N24



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.225	—	5.72
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.160	1.290	29.46	32.77
E	0.585	0.625	14.86	15.88
E_1	0.500	0.610	12.70	15.49
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.098	1.02	2.49

Note: (1) The minimum limit for dimensions B1 may be 0.023” (0.58 mm) for all four corner leads only.

Notes

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