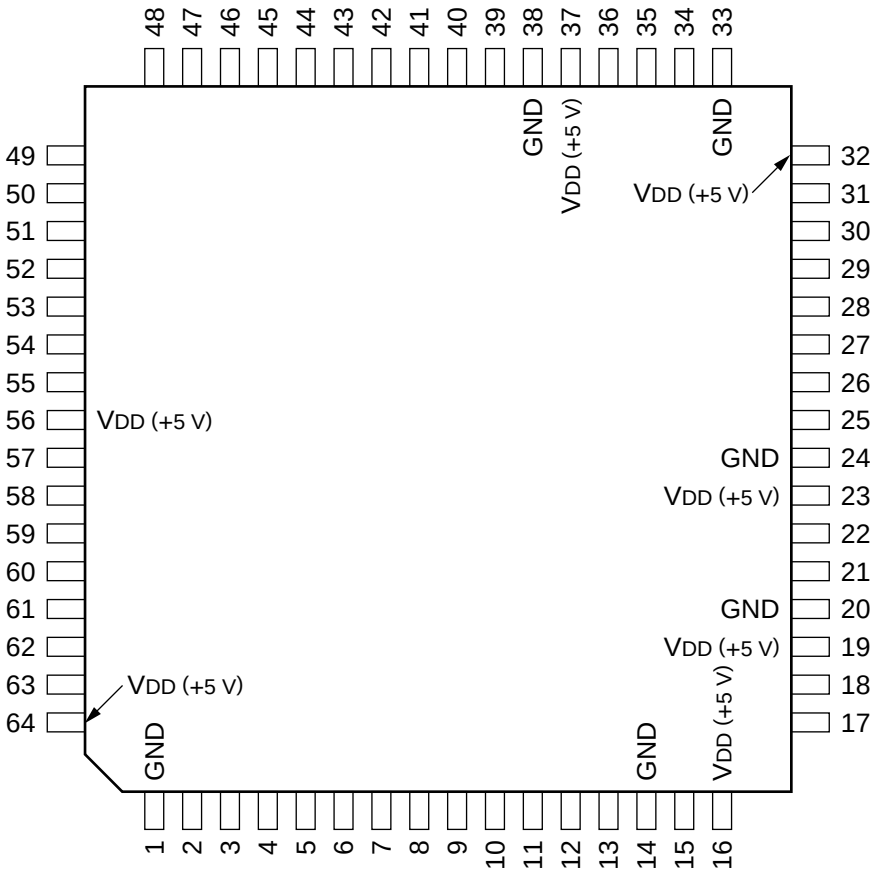
C-MOS TIMING GENERATOR FOR CCD

—TOP VIEW—



(VDD = +5 V)

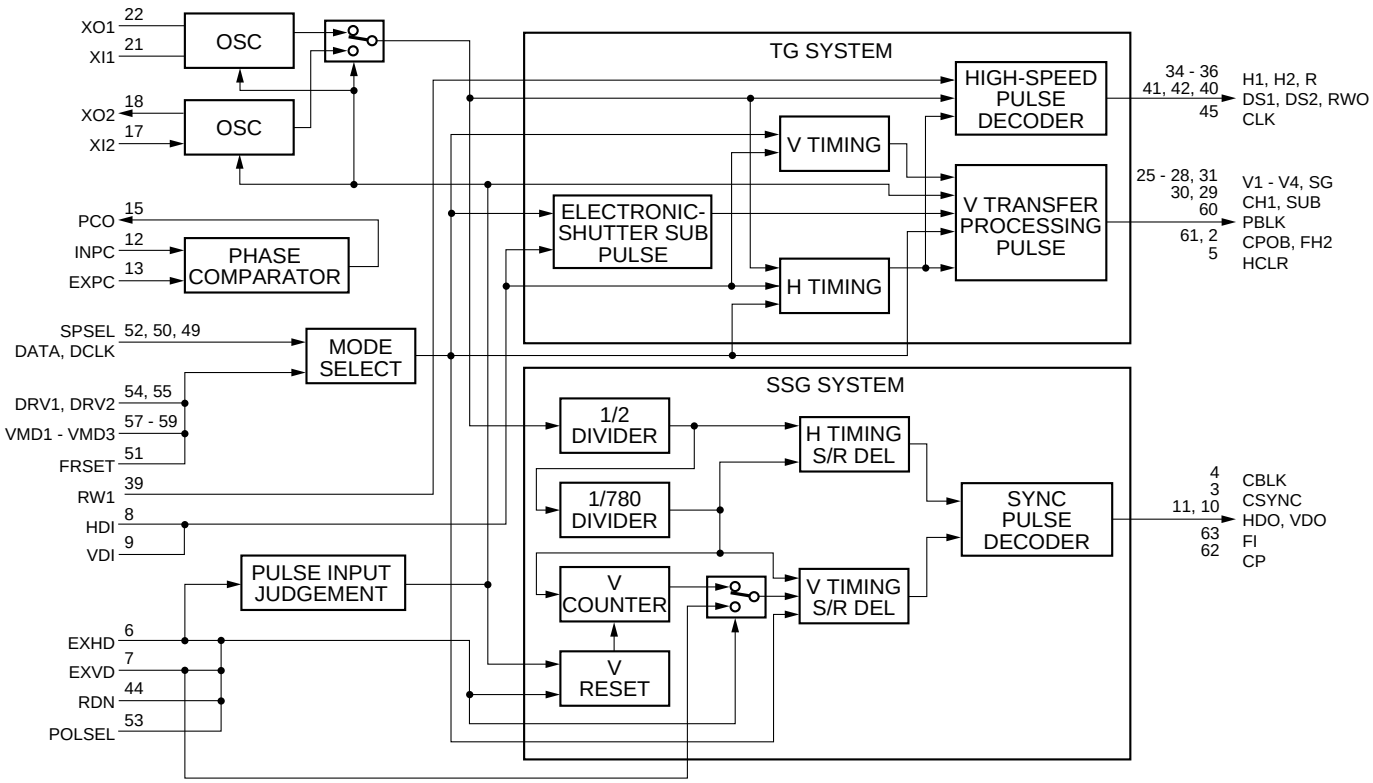
PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	GND	17	I	XI2	33	—	GND	49	I	DCLK
2	O	FH2	18	O	XO2	34	O	H1	50	I	DATA
3	O	CSYNC	19	—	VDD	35	O	H2	51	I	FRSET
4	O	CBLK	20	—	GND	36	O	R	52	I	SPSEL
5	O	HCLR	21	I	XI1	37	—	VDD	53	I	POLSEL
6	I	EXHD	22	O	XO1	38	—	GND	54	I	DRV1
7	I	EXVD	23	—	VDD	39	I	RWI	55	I	DRV2
8	I	HDI	24	—	GND	40	O	RWO	56	—	VDD
9	I	VDI	25	O	V1	41	O	DS1	57	I	VMD1
10	O	VDO	26	O	V2	42	O	DS2	58	I	VMD2
11	O	HDO	27	O	V3	43	I	TEST	59	I	VMD3
12	I	INPC	28	O	V4	44	I	RDN	60	O	PBLK
13	I	EXPC	29	O	SUB	45	O	CLK	61	O	CPOB
14	—	GND	30	O	CH1	46	I	CLR	62	O	CP
15	O	PCO	31	O	SG	47	I	TEST1	63	O	FI
16	—	VDD	32	—	VDD	48	I	TEST2	64	—	VDD

INPUT

CLR	:	ALL CLEAR
DATA	:	SERIAL ELECTRONIC SHUTTER DATA
DCLK	:	SERIAL ELECTRONIC SHUTTER CLOCK
DRV1, DRV2	:	ØV DRIVE MODE SELECT
EXHD	:	EXTERNAL HD PULSE
EXPC	:	PHASE COMPARATOR 2
EXVD	:	EXTERNAL VD PULSE
FRSET	:	TG SYSTEM FRAME RESET MODE
HDI	:	HD PULSE
INPC	:	PHASE COMPARATOR 1
POLSEL	:	POLARITY SELECT
RDN	:	SSG RESET
RWI	:	ØR TRANSFER PULSE WIDTH ADJUSTMENT
SPSEL	:	SERIAL/PARALLEL SELECT
TEST	:	TEST
TEST 1, TEST 2	:	TEST
VDI	:	VD PULSE
VMD1 - VMD3	:	PARALLEL ELECTRONIC SHUTTER MODE SELECT
XI1	:	2FCK (24.5 MHz) EXTERNAL CRYSTAL
XI2	:	2FCK (24.5 MHz) EXTERNAL CRYSTAL

OUTPUT

CBLK	:	COMPOSITE BLANKING PULSE
CH1	:	ØV1 READ PULSE
CLK	:	FCK CLOCK
CP	:	CLAMP PULSE
CPOB	:	OB CLAMP PULSE
CSYNC	:	COMPOSITE SYNC
DS1, DS2	:	CDS PULSE
FH2	:	FH2 PULSE
FI	:	FIELD INDEX
H1, H2	:	ØH TRANSFER PULSE
HCLR	:	ØH CLEAR PULSE
HDO	:	HD PULSE
PBLK	:	PRE-BLANKING
PCO	:	PHASE COMPARATOR
R	:	ØR TRANSFER PULSE
RWO	:	ØR TRANSFER PULSE WIDTH ADJUSTMENT
SG	:	ØSG PULSE
SUB	:	SUBSTRATE PULSE
V1 - V4	:	ØV TRANSFER PULSE
VDO	:	VD PULSE
XO1	:	2FCK (24.5 MHz) EXTERNAL CRYSTAL
XO2	:	2FCK (24.5 MHz) EXTERNAL CRYSTAL


XO1
22
XI1
21
OSC
XO2
18
XI2
17
OSC
PCO
15
INPC
12
EXPC
13
PHASE COMPARATOR
SPSEL
DATA, DCLK
52, 50, 49
MODE SELECT
DRV1, DRV2
54, 55
VMD1 - VMD3
57 - 59
FRSET
51
RW1
39
HDI
8
VDI
9
PULSE INPUT JUDGEMENT
EXHD
6
EXVD
7
RDN
44
POLSEL
53
TG SYSTEM
HIGH-SPEED PULSE DECODER
V TIMING
ELECTRONIC-SHUTTER SUB PULSE
V TRANSFER PROCESSING PULSE
H TIMING
34 - 36
41, 42, 40
45
H1, H2, R
DS1, DS2, RWO
CLK
25 - 28, 31
30, 29
60
61, 2
5
V1 - V4, SG
CH1, SUB
PBLK
CPOB, FH2
HCLR
SSG SYSTEM
1/2 DIVIDER
1/780 DIVIDER
V COUNTER
V RESET
H TIMING S/R DEL
V TIMING S/R DEL
SYNC PULSE DECODER
4
3
11, 10
63
62
CBLK
CSYNC
HDO, VDO
FI
CP