5.5Mbit AS Memory

P/N: MN47V07AF

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■ Description

The MN47V07AF is a 5.5Mbit CMOS Dynamic RAM with 8bit serial shift registers which can perform serial input and output as 50ns Min. clock rate.

Large scale memory and low power dissipation are realized by using 1 transistor type dynamic memory cell, and CMOS circuits for peripheral circuits.

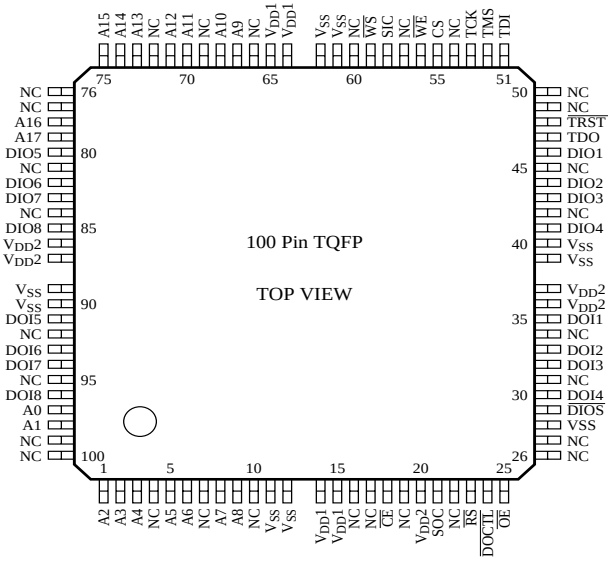
This memory has shift-in and shift-out registers for serial / parallel data conversion, and can execute high speed data transfer, read, and write operation.

This memory can provide many features to construct frame memory systems.

■ Features

- 8 bit serial / parallel converter incorporated
- Data Output/Input are possible to be switched
- Random Access by 8 Byte serial unit
- Boundary Scan Test function incorporated
- Power Supply voltage : V_{DD1}=2.7V~3.3V
  V_{DD2}=2.0V~V_{DD1}V

■ Pin Assignment



■ Pin Names

Symbol	Pin names	Symbol	Pin names
A0~A17	Address Inputs	$\overline{DIOS}$	Data Input/Output Select
$\overline{CE}$	Chip Enable	$\overline{DOCTL}$	Data Output Control
$\overline{OE}$	Output Enable	TCK	Boundary Scan Test Clock
$\overline{WE}$	Write Enable	TMS	Boundary Scan Test Mode Select
$\overline{WS}$	Write Strobe	$\overline{TRST}$	Boundary Scan Test Reset
$\overline{RS}$	Read Strobe	TDI	Boundary Scan Test Data Input
CS	Chip Select	TDO	Boundary Scan Test Data Output
SIC	Shift-in Clock	V_{DD1}	Internal Power Supply (2.7V~3.3V)
SOC	Shift-out Clock	V_{DD2}	I/F Power Supply (2.0V~V_{DD1}V)
DIO1~8	Data Input/Output	V_{SS}	Power Supply (GND)
DOI1~8	Data Output/Input	NC	No Connection

■ Pin Descriptions

● Chip Enable Input Pin [$\overline{CE}$]

The MN47V07AF fetches addresses (row address and column address together) at the falling edge $\overline{CE}$, and after selecting the concerned word line and activating the sense amplifier, selects the corresponding 8-word(64bits) of memory cell when CS level is “H”.

● Chip Select Input Pin [CS]

This is an input pin for chip selection. To the chip intended for Read/Write, the level must be put into “H”. CS is fetched together with the address at the falling edge of $\overline{CE}$.

■ Pin Descriptions

● Read Strobe Input Pin [$\overline{RS}$]

When $\overline{CE}$ clock and $\overline{RS}$ are inactivated by the read strobe input, the selected 8-word (64 bits) of memory data is transferred to the I/O controller and latched, and thereafter transferred to the shift-out register.

● Write Enable Input Pin [$\overline{WE}$]

The write enable input inactivates $\overline{CE}$ clock and $\overline{WE}$ to write the data of the I/O controller into the selected 8-word (64 bit) of memory cell.

● Write Strobe Input Pin [$\overline{WS}$]

When $\overline{WS}$ is activated by the write strobe input, the data of the shift-in register is transferred to the I/O controller and latched.

● Output Enable Input Pin [$\overline{OE}$]

The output enable input is a clock to control the output impedance. When the output enable signal is input, $\overline{OE}$ level becomes "H", and after the interval of t_{OEZ}, the DIO1~DIO8 (DOI1~DOI8) output become Hi-Z. When $\overline{OE}$ level becomes "L", and after the interval of t_{OEA}, the DIO1~DIO8 (DOI1~DOI8) output is enabled. $\overline{OE}$ exerts no influence on SOC clock shift-out register control.

● Shift-in Clock Input Pin [SIC]

This is an input pin of the shift-in clock. At the rising of this clock, data is sequentially fetched into the shift-in register.

● Shift-out Clock Input Pin [SOC]

This is an input pin of the shift-out clock. At the rising of this clock, 1 word (8 bits) of the serial data is sequentially output. This output data is held until next rising of the shift-out clock.

● Address Input Pin [A0~A17]

The MN47V07AF requires 18bit address inputs to select one address from among the 90,720 addresses. The row address and the column address are simultaneously fetched at the falling edge of $\overline{CE}$.

● Data Input/Output Pin [DIO1~DIO8]

These are serial data input/output pins. When $\overline{DIOS}$ is "H", these work as data input pins. When $\overline{DIOS}$ is "L", these work as data output pins.

● Data Output/Input Pin [DOI1~DOI8]

These are serial data output/input pins. When $\overline{DIOS}$ is "H", these work as data output pins. When $\overline{DIOS}$ is "L", these work as data input pins.

● Data Input/Output Select Pin [$\overline{DIOS}$]

This is a data input/output select pin for serial data input/output selection.

● Data Output Contorol Pin [$\overline{DOCTL}$]

This is a data output control pin. After $\overline{DOCTL}$ is "H" in the interval of t_{DOL}, the output data of DOI1 ~DOI8 (DIO1~DIO8) is "L". After $\overline{DOCTL}$ is "L" in the interval of t_{DOA}, the output data of DOI1~DOI8 (DIO1~DIO8) is enable.

■ Pin Descriptions

● Boundary Scan Test Clock Pin [TCK]

This is a clock pin for boundary scan testing. This clock signal is independent from circuit area expect for boundary scan test ciucuits.

● Boundary Scan Test Mode Select Pin [TMS]

This is a mode select pin for boundary scan testing. At the rising edge of TCK clock, this is fetched and defines TAP controller movement.

● Boundary Scan Test Reset Pin [$\overline{\text{TRST}}$]

This is a reset pin for boundary scan testing. When $\overline{\text{TRST}}$ is “L”, it initializes TAP controller asynchronously.

● Boundary Scan Test Data Input Pin [TDI]

This is a scan data input pin for boundary scan testing. At the rising edge of TCK clock, this is fetched.

● Boundary Scan Test Data Output Pin [TDO]

This is a scan data output pin for boundary scan testing. At the falling edge of TCK clock, this is changed. This is a 3 states output pin and controlled by boundary scan test controller.

● Internal Power Supply Pin [V_{DD1}]

This is an internal power supply pin. (2.7V~3.3V)

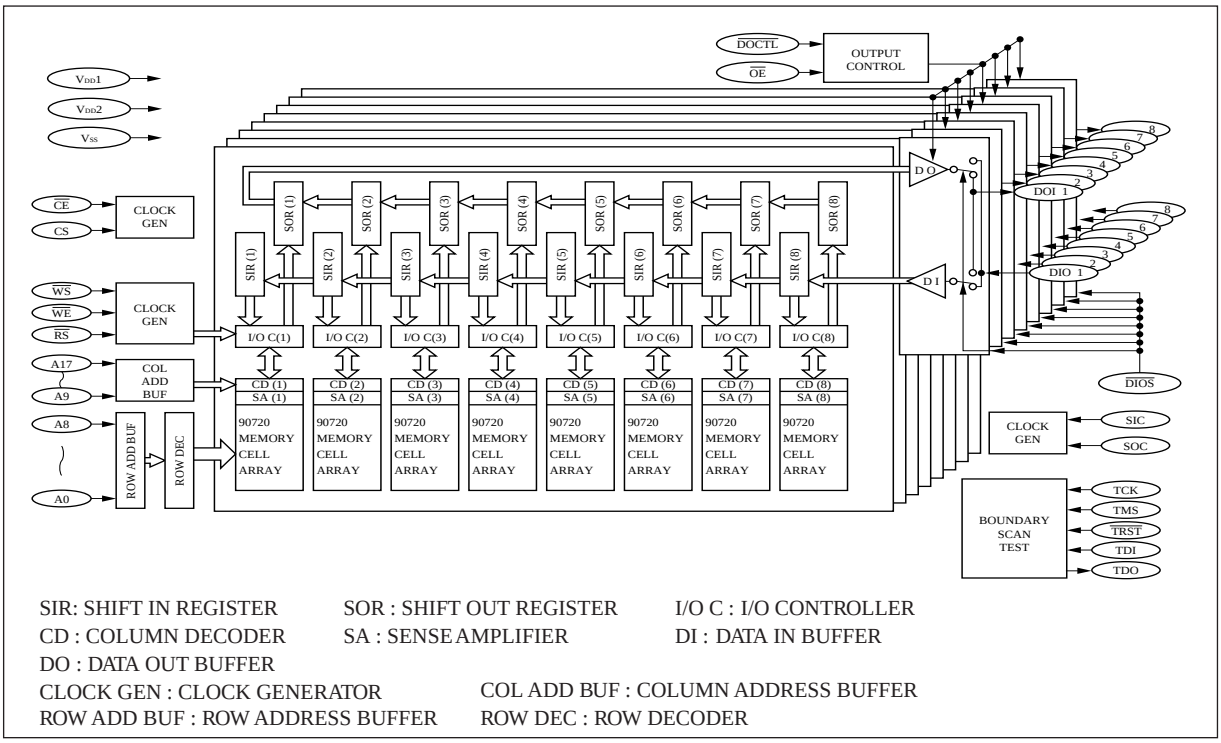
● I/F Power Supply Pin [V_{DD2}]

This is an I/F power supply pin. (2.0V~V_{DD1}V)

● Power Supply Pin [V_{SS}]

This is a power supply pin. (GND)

■ Block Diagram



SIR: SHIFT IN REGISTER SOR : SHIFT OUT REGISTER I/O C : I/O CONTROLLER
CD : COLUMN DECODER SA : SENSE AMPLIFIER DI : DATA IN BUFFER
DO : DATA OUT BUFFER
CLOCK GEN : CLOCK GENERATOR COL ADD BUF : COLUMN ADDRESS BUFFER
ROW ADD BUF : ROW ADDRESS BUFFER ROW DEC : ROW DECODER

■ Explanation of Operation

● Data operation

The eight data inputs and outputs (DIO1~DIO8, DOI1~DOI8) of the MN47V07AF are dealt with 8-byte serial form respectively.

The input data is fetched in by the rising edge of SIC, and transferred to the internal 8-bit shift-in register in turn. The 8-bit data in the shift-in register is transferred to the I/O controller simultaneously at the falling edge of $\overline{WS}$.

The input data latched in the I/O controller is written into the memory cell by the memory write cycle. Therefore, the data written into the memory cell corresponds to the input data for SIC 8 cycles before falling of $\overline{WS}$.

The 8-bit data read from the memory block by the memory read cycle is latched in the I/O controller at the falling edge of $\overline{RS}$, and the read data is transferred to the shift-out register simultaneously. The data transferred to the shift-out register is output in turn synchronized with SOC from SOC rising immediately after the $\overline{RS}$ falling. When the 8-bytes data is output in turn synchronized with SOC from the SOC rising immediately after the $\overline{RS}$ falling, the 9th-byte or later data are indefinite.

● Memory read/write cycle

When CS is in the "H" level(chip selection), and $\overline{CE}$ falls down, the memory read cycle or the memory write cycle starts. The read operation or the write operation is selected by $\overline{WE}$.
When $\overline{WE}$ is in the "H" level, the read cycle is selected,and when $\overline{WE}$ is in the "L" level, the write cycle is selected.

The address of memory cell to be selected is fetched at the falling edge of $\overline{CE}$. For read cycle,when $\overline{RS}$ falls after the time of t_{CRD} from the falling edge of $\overline{CE}$, the data read from memory cell is transferred to the shift-out register. The read data transferred to the shift-out register is output in turn by the rising of SOC clock when $\overline{OE}$ is in the "L" level and $\overline{DOCTL}$ is in the "L" level.

The write cycle is started by falling $\overline{WE}$ within the time of t_{WCS} from the falling edge of $\overline{CE}$. In this case, the timing to be completed the data transfer to the I/O controller by $\overline{WS}$ is specified by t_{WSS}.

● $\overline{CE}$ only refresh cycle

The MN47V07AF supports $\overline{CE}$ only refresh mode. The refresh period is 1,080 cycle/4ms. The refresh address of the MN47V07AF consists of row addresses from 0 to 269 (A0 to A8) and column address from 0 to 3(A9 to A10).

$\overline{CE}$ only refresh cycle is used to refresh the data of 5,376 bits per one address using the sense amplifier to rewrite in each memory cell by selecting one address from 1,080 addresses specified by the 11 lower bits (A0 to A10) of the address. A system, which has access to all above-stated 1,080 addresses within 4ms, may not require another refresh cycle newly.

When $\overline{CE}$ only refresh performs, CS must be set in the "H" level.

Explanation of the Address Space

The address space of the MN47V07AF is 90,720 addresses space consisted of 270 row addresses and 336 column addresses.

The address input is taken by the 9 bits respectively of row addresses (A0 to A8) and column addresses (A9 to A17). Therefore, it is possible to be taken Max 512 address both row and column, but the address space of this memory consists of row addresses from 0 to 269 and column addresses from 0 to 335. So there are not memory area except the addresses above.

The addresses space (A0 to A17) which are present in the memory and the address space which are not present in the memory is shown in figure below.

When the address which is not present in the memory is input, the memory access is not performed.

			A0	A1	A2	A3	A4	A5	A6	A7	A8
	○	×	0	0	0	0	0 ≀ 1	0	0	0	0
			1	0	1	1	0	0	0	0	1
	×	×	0	1	1	1	0 ≀ 1	0	0	0	1
			1	1	1	1	1	1	1	1	1
A9	0	1	0	1							
A10	0	1	0	1							
A11	0	1	0	1							
A12	0	1	0	1							
A13	0 ~ 0		1 ~ 1								
A14	0	0	0	1							
A15	0	1	1	1							
A16	0	0	0	1							
A17	0	1	1	1							

○: The address which are present in the memory
×: The address which are not present in the memory

Relation Between Input and Output Data

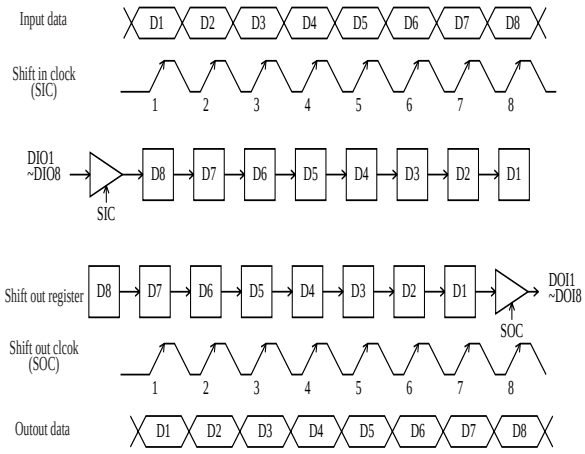
This input data are fetched from D1 of the input pins of DIO1~DIO8 or DOI1~DOI8 by the shift-in clock (SIC) in turn, and the data are lined up in the shift-in register as shown in the figure below after eight clocks have been input. These data are written in parallel of eight bits by the memory write cycle.

The output data is read by the memory read cycle, and transferred to the shift-out register in parallel of eight bits by $\overline{RS}$.

The data in this time lined up as shown in the figure below, and are output in turn from D1 to the each pin of DOI1 to DOI8 or DIO1 to DIO8 in the input sequence by the shift-out clock(SOC).

● Conception chart

($\overline{DIOS}$="H" , $\overline{DOCTL}$="L")



Explanation of Output Pin Control

There are two data, output control pins of the MN47V07AF the $\overline{OE}$ pin and $\overline{DOCTL}$ pin. Each level combination of these pins determines the states of output pins as shown in the table.

		$\overline{DOCTL}$	
		"H"	"L"
$\overline{OE}$	"H"	Hi-Z	Hi-Z
	"L"	Fix "L"	Output enable

■ Absolute Maximum Ratings (V_{SS}=0V)

Parameter	Symbol	Rating	Unit	Notes
Internal Power Supply Voltage	V_{DD1}	–0.5 ~ +4.2	V	
I/F Power Supply Voltage	V_{DD2}	–0.5 ~ +V_{DD1}	V	
Input Voltage	V_{IN}	–0.5 ~ +V_{DD2}	V	
Output Voltage	V_{OUT}	–0.5 ~ +V_{DD2}	V	
Short Circuit Output Current	I_{OS}	20	mA	
Power Dissipation	P_D	1.0	W	1)
Operating Temperature	Ta	–20 ~ +75	˚C	
Storage Temperature	Tstg	–55 ~ +125	˚C	

Stress greater than those listed under “Absolute Maximum Ratings” (ex. excess voltage input or reverse insertion) may affect reliability of the device and cause unusual heat, deterioration of characteristics or breakdown of the device.
1) Ta=25˚C

■ Operating Conditions (V_{SS}=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Internal Power Supply Voltage	V_{DD1}	2.7		3.3	V
I/F Power Supply Voltage	V_{DD2}	2.0		V_{DD1}	V
Input High Voltage	V_{IH}	0.7V_{DD2}		V_{DD2}	V
Input Low Voltage	V_{IL}	0		0.3V_{DD2}	V
Operating Temperature	Ta	–20	25	75	˚C

■ Pin Capacitance (V_{DD2}=2.0V~V_{DD1}V , f=1MHz, Ta=25˚C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance	C_I			7	pF
Input and Output Capacitance	C_O			10	pF

■ DC Characteristics (V_{DD1}=2.7V ~ 3.3V, V_{DD2}=2.0V ~ V_{DD1}V, Ta=–20 ~ +75°C, V_{SS}=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Output High Voltage (I_{OH}= –100µA)	V_{OH}	V_{DD2}×0.8		V_{DD2}	V	
Output Low Voltage (I_{OL}= 400µA)	V_{OL}			0.4	V	
Input Current (V_{IN}=V_{DD2})	I_{I1}	5		50	µA	2)
Input Current (V_{IN}= 0V)	I_{I2}	–5		–50	µA	3)
Operating Current (Average Current) (Min.memory cycle, $\overline{OE}$="H")	I_{DD1}			58	mA	
Standby Current (SIC=SOC="L", $\overline{CE}$=$\overline{OE}$="H")	I_{DD2}			1.5	mA	4)

2) Pulled-down pins : A0~A17, DIO1~DIO8, DOI1~DOI8, $\overline{DOCTL}$, $\overline{DIOS}$, CS, SIC, SOC, TCK
3) Pulled-up pins : $\overline{CE}$, $\overline{RS}$, $\overline{OE}$, $\overline{WE}$, $\overline{WS}$, $\overline{TRST}$, TDI, TMS
4) Input voltage of pulled-down pins fix V_{SS} level. Input voltage of pulled-up pins fix V_{DD2} level.

■ AC Characteristics (V_{DD1}=2.7V ~ 3.3V, V_{DD2}=2.0V ~V_{DD1} V, Ta=–20 ~ +75°C, V_{SS}=0V)

Parameter	Symbol	MN47V07AF		Unit	Notes
		Min.	Max.		
Refresh Cycle Time	t_{REF}		4	ms	
$\overline{OE}$ Access Time	t_{OEA}		45	ns	7)
SOC Access Time	t_{SOA}		45	ns	7)
Output Disable Time	t_{OEZ}		40	ns	7)
Read/Write Cycle Time $\overline{CE}$ Only Refresh Cycle Time	t_C	215		ns	
$\overline{CE}$ Precharge Time	t_P	100		ns	
$\overline{CE}$ Pulse Width	t_{CE}	80	1000	ns	
Address and CS Setup Time	t_{ASC}	0		ns	8)
Address and CS Hold Time	t_{AHC}	30		ns	8)
$\overline{CE}$ • $\overline{RS}$ Delay Time	t_{CRD}	140		ns	9)
$\overline{RS}$ Pulse Width	t_{RS}	30	1000	ns	
$\overline{RS}$ Precharge Time	t_{RSP}	30		ns	
$\overline{WE}$ Setup Time	t_{WCS}		30	ns	
$\overline{WS}$ Setup Time	t_{WSS}		20	ns	
$\overline{WE}$ Read Cycle Setup Time	t_{RCS}	0		ns	
$\overline{WE}$ Read Cycle Hold Time	t_{RCH}	75		ns	
$\overline{CE}$ to $\overline{WE}$ Hold Time	t_{WHC}	125		ns	
$\overline{WS}$ Precharge Time	t_{WSP}	30		ns	
$\overline{WS}$ Pulse Width	t_{WS}	30	1000	ns	
$\overline{WS}$ Prohibition Time	t_{WIH}	85		ns	
SOC Setup Time	t_{SOS}	3		ns	
SOC Effective Time	t_{SOV}	20		ns	
SOC Precharge Time	t_{SOP}	15		ns	
SOC Pulse Width	t_{SO}	15		ns	
Serial Out Cycle Time	t_{SOC}	50	200	ns	
Output Data Hold Time	t_{SOH}	8		ns	
SIC Effective Time	t_{SIV}	3		ns	
SIC Hold Time	t_{SIH}	20		ns	
SIC Precharge Time	t_{SIP}	15		ns	
SIC Pulse Width	t_{SI}	15		ns	

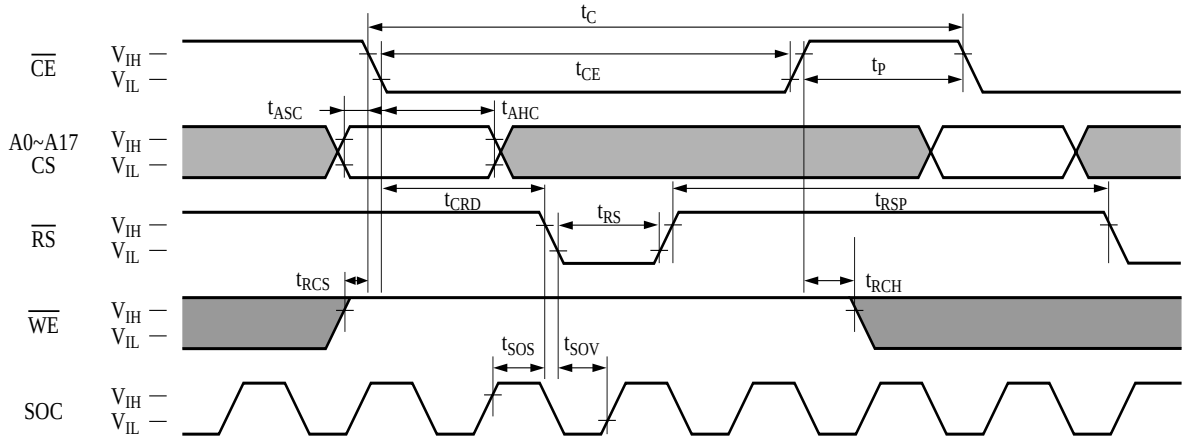
■ AC Characteristics (V_{DD1}=2.7V ~ 3.3V, V_{DD2}=2.0V ~V_{DD1} V, Ta=–20 ~ +75°C, V_{SS}=0V)

Parameter	Symbol	MN47V07AF		Unit	Notes
		Min.	Max.		
Serial in Cycle	t_{SIC}	50	200	ns	
Data Input Setup Time	t_{DS}	13		ns	
Data Input Hold Time	t_{DH}	2		ns	
$\overline{DOCTL}$ "L" Access Time	t_{DOL}		45	ns	
$\overline{DOCTL}$ Access Time	t_{DOA}		45	ns	
Data Input and Output Change Time	t_{IOC}		100	ns	
Transition Time (Rise and Fall)	t_T	3	30	ns	10)

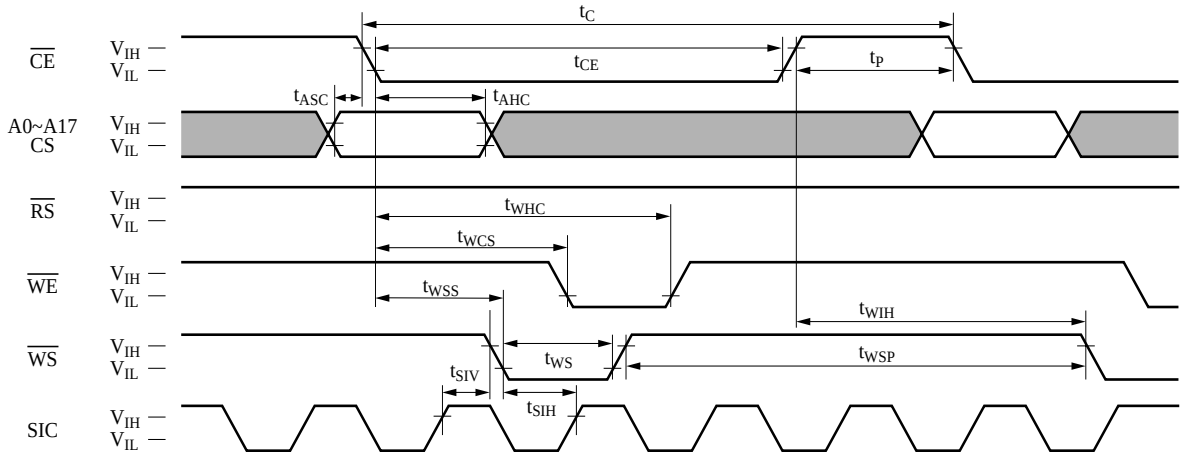
5) After the power supply has been turned on, the input pins set at low level for the waiting time of 200ms before memory operation. After that, input the dummy cycles of more than eight times by $\overline{CE}$, SIC and SOC, then CS is in the "H" level. The dummy cycle is necessary even after $\overline{CE}$ have been continued in the "H" level for more than 4ms.
6) Standard level for AC measurement is V_{IH}=0.7V_{DD2}V, V_{IL}=0.3V_{DD2}V, V_{OH}=0.7V_{DD2}V, V_{OL}=0.3V_{DD2}V.
7) The output pin load is measured with 10pF.
8) CS is taken in the same timing as the address input.
9) The data read the memory read cycle started from $\overline{CE}$ falling immediately before the $\overline{RS}$ falling is transferred to the shift-out register.
10) The measurement is performed assuming that t_T=5.0ns.

■ Timing Chart

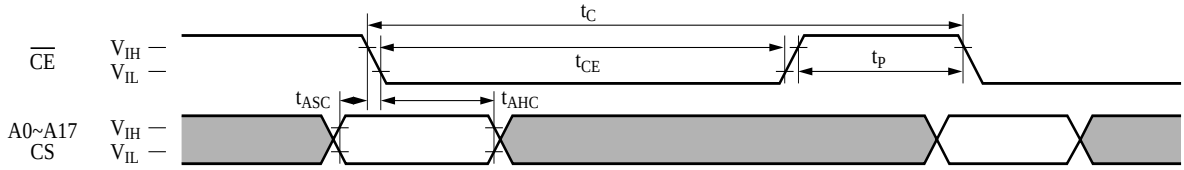
● MEMORY READ CYCLE



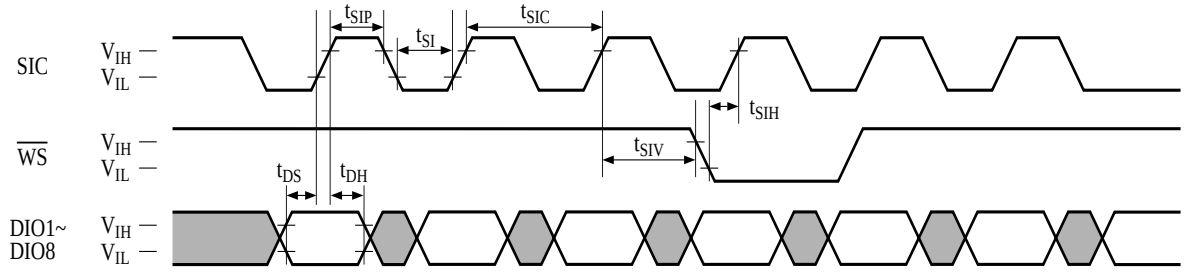
● MEMORY WRITE CYCLE



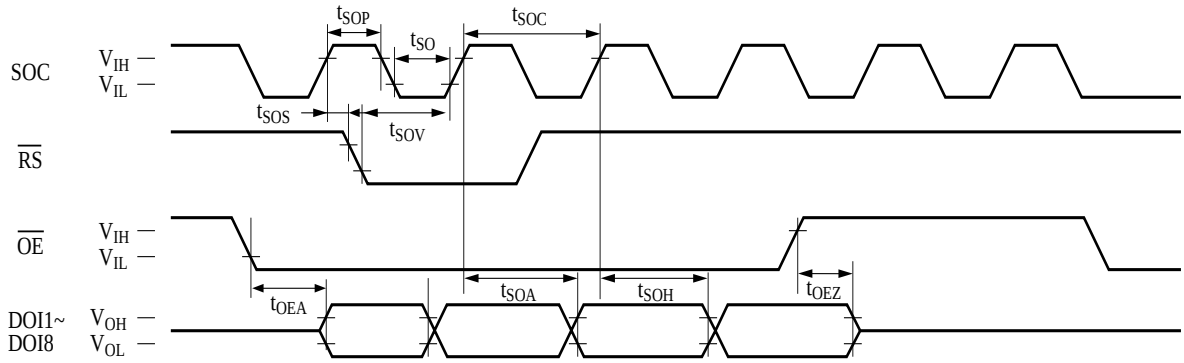
● $\overline{CE}$ ONLY REFRESH CYCLE



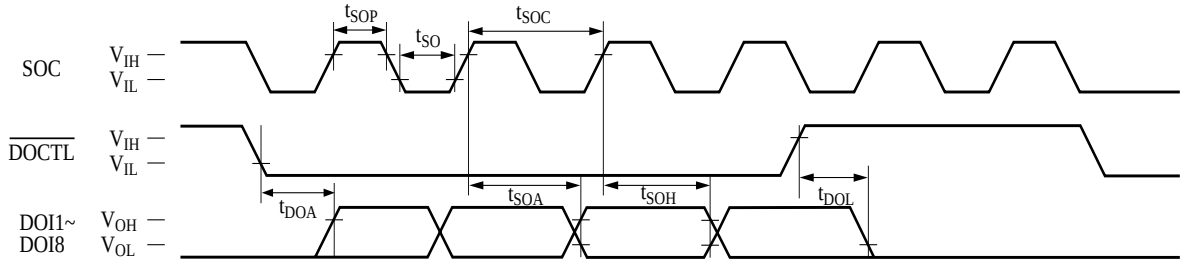
● SHIFT IN CYCLE ($\overline{DIOS}$="H")



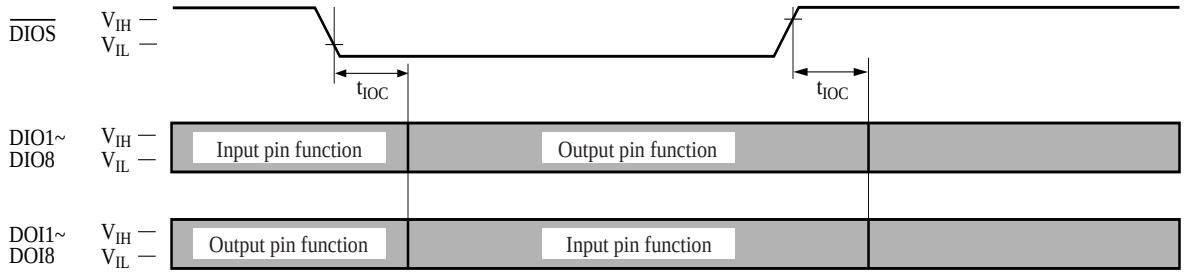
● SHIFT OUT CYCLE ($\overline{DIOS}$="H", $\overline{DOCTL}$="L")



● SHIFT OUT CYCLE ($\overline{DIOS}$="H", $\overline{OE}$="L")



● INPUT and OUTPUT CHANGE TIMING



■ Boundary Scan

1.Features

(1)IEEE1149.1 JATG Boundary Scan Stadard

(2)Boundary scan exclusive pin (5pins)

TCK (Test Clock)

TMS (Test Mode Select)

TDI (Test Data Input)

TDO (Test Data Output)

$\overline{\text{TRST}}$ (Test Reset)

(3)Boundary scan exclusive register

IR:Instruction Register

BR:Bypass Register

BSR:Boundary Scan Register

IDR:IDcode Register

(4)Command

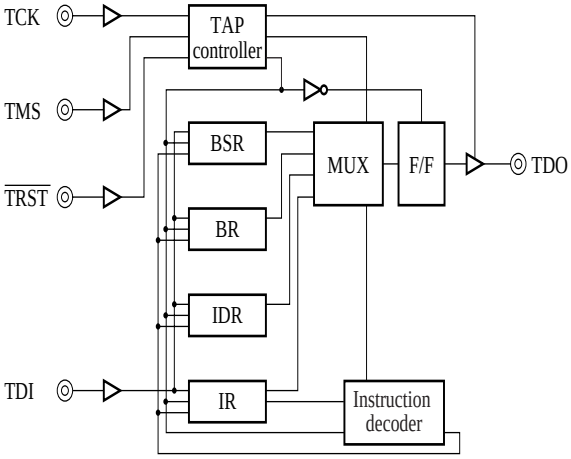
EXTEST command

IDCODE command

SAMPLE command

BYPASS command

2.Block diagram of boundary scan circuit



(1)TAP controller

TAP controller changes its state of operating, by latching the input data of TMS at the rising edge of TCK.

(2)Instruction register

Instruction register consists of 3-bit shift register. Input data of TDI is latched-in at the rising edge of TCK clock. And the data is output to TDO pin on the falling edge of TCK clock. The command data determines which register/command be selected.

(3)Bypass register

Bypass register consists of 1-bit shift register that connects between TDI pin and TDO pin. When TAP controller is in the Shift-DR stat and the bypass register is selected, this register latches input data of TDI pin at the rising edge of TCK clock. And the data is output to TDO pin at the falling edge of TCK clock.

(4)Boundary scan register

There are boundary scan registers between outside pins and logic circuit. When this register is selected, data is latched to or loaded from this register by the command of TAP controller. When the TAP controller is in the Shift-DR state and this register is selected, the data is output to TDO pin at the falling edge of TCK clock.

(5)IDCODE register

After the TAP controller changed to the Capture-DR state, IDCODE register loads 32-bit identification code at the rising edge of TCK clock. When the TAP controller is in the Shift-DR state and the register is selected, the data is output sequentially to TDO pin from LSB at the falling edge of TCK clock.

3.Pin descriptions

(1)TCK pin

TCK pin is used to supply the clock to boundary scan circuit.This clock is separated not to supply for a system circuit. And this pin is pulled-down internally to V_{SS} through a 50kΩ ~ 200kΩ resister.

(2)TMS pin

Input data of TMS pin is latched at the rising edge of TCK clock, and it defines TAP controller operation. And this pin is pulled-up internally to V_{DD2} through a 50kΩ ~ 200kΩ resister.

(3)TDI pin

TDI pin is an input pin to be input the data from the register of boundary scan circuit to serial register. And this pin is pulled-up internally to V_{DD2} through a 50kΩ ~ 200kΩ resister.

(4)TDO pin

TDO pin is an output pin to be output the data from the register of boundary scan circuit to serial register. Output data changes at the falling edge of TCK clock. This output pin is tri-state, and it is controlled by TAP controller.

(5)$\overline{\text{TRST}}$ pin

When $\overline{\text{TRST}}$ pin is in "L" level, TAP controller is reset asynchronously. In this case, the device becomes a normal operation mode and the boundary scan circuit becomes the standby state (IDCODE command). And this pin is pulled-up internally to V_{DD2} through a 50kΩ ~ 200kΩ resister.

4.Explanation of operation

(1)TAP controller

TAP controller is a circuit constituted of 16 states to be changed when input data of TMS is latched at the rising of TCK clock. This operation is regulated in the IEEE standard 1149.1.

(2)TAP controller state

TAP controller states are shown in the figure 2. The change of all states of TAP controller are determined by the TMS state at the falling edge of TCK clock. Operation of instruction register, boundary scan register, bypass register, and IDCODE register are changed on the rising/falling edge of TCK clock.

Note)"H" level and "L" level to adjoin the arrows in the figure shows the state of TMS pin at the rising edge of TCK clock.

5.Operation of TAP controller

(1)Operation of TAP controller

TAP controller changes its state by any (1),(2),(3).

(1) At the rising edge of TCK clock

(2) During "L" level of $\overline{\text{TRST}}$ pin

(3) Power on

TAP controller generates a signal to control the operation of test data register (bypass register, boundary scan register, IDCODE register) and instruction register.(Fig4. Fig5.)The circuit, that selects the enable signal of TDO pin and the register to be output, is controlled as table 1.TDO pin changes its state at the falling edge of TCK clock after it is changed to the state described in table 1.

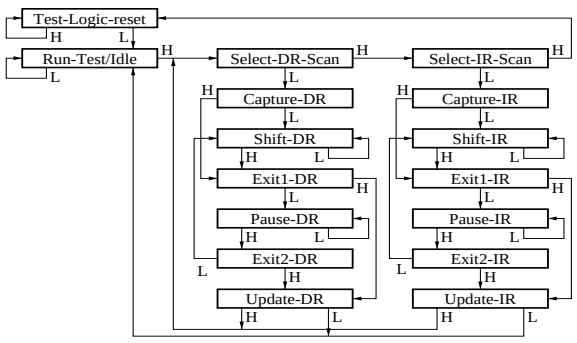


Fig 2. TAP controller state

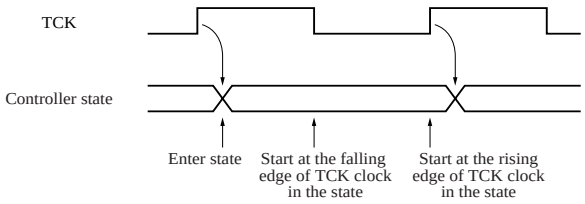


Fig 3. Operation timing of controller state

Table 1. Controller operation

Control state	Register to drive TDO pin	The state of TDO pin
Test-Logic-Reset	Not defined	Inactive (Hi-impedance)
Run-Test/Idle		
Slect-DR-Scan		
Slect-IR-Scan		
Capture-DR		
Shift-IR	Instruction register	Active
Exit1-IR	Not defined	Inactive (Hi-impedance)
Pause-IR		
Exit2-IR		
Update-IR		
Capture-IR		
Shift-DR	Test data register	Active
Exit1-DR	Not defined	Inactive (Hi-impedance)
Pause-DR		
Exit2-DR		
Update-DR		

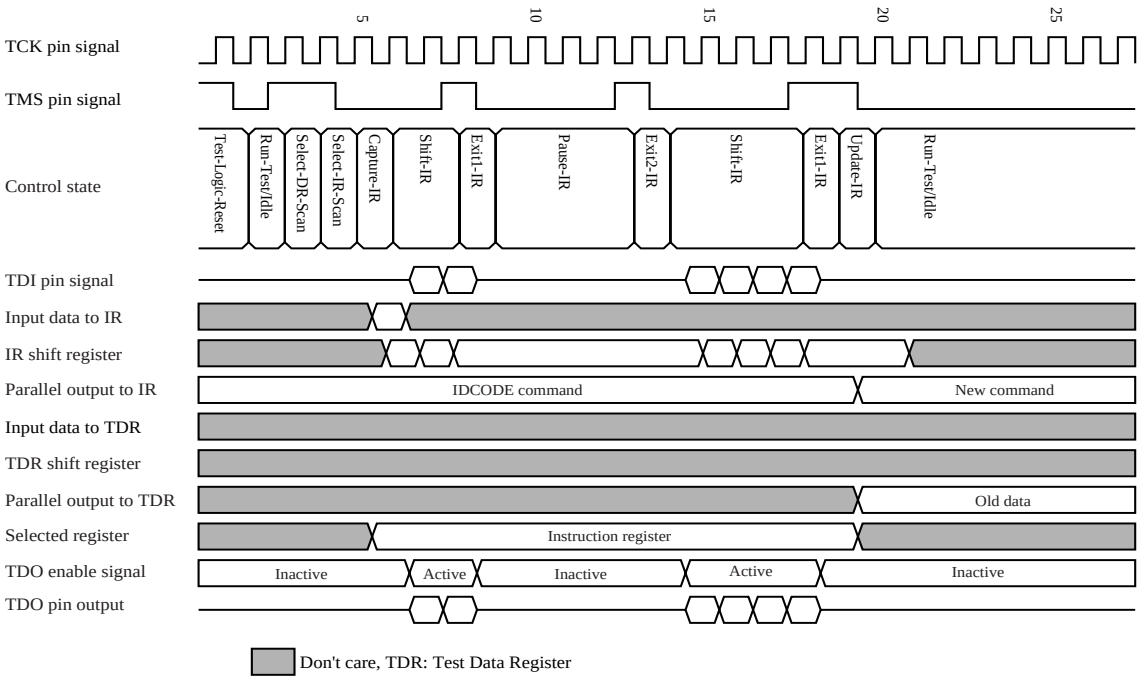


Fig 4 Operation of test logic (Instruction scan)

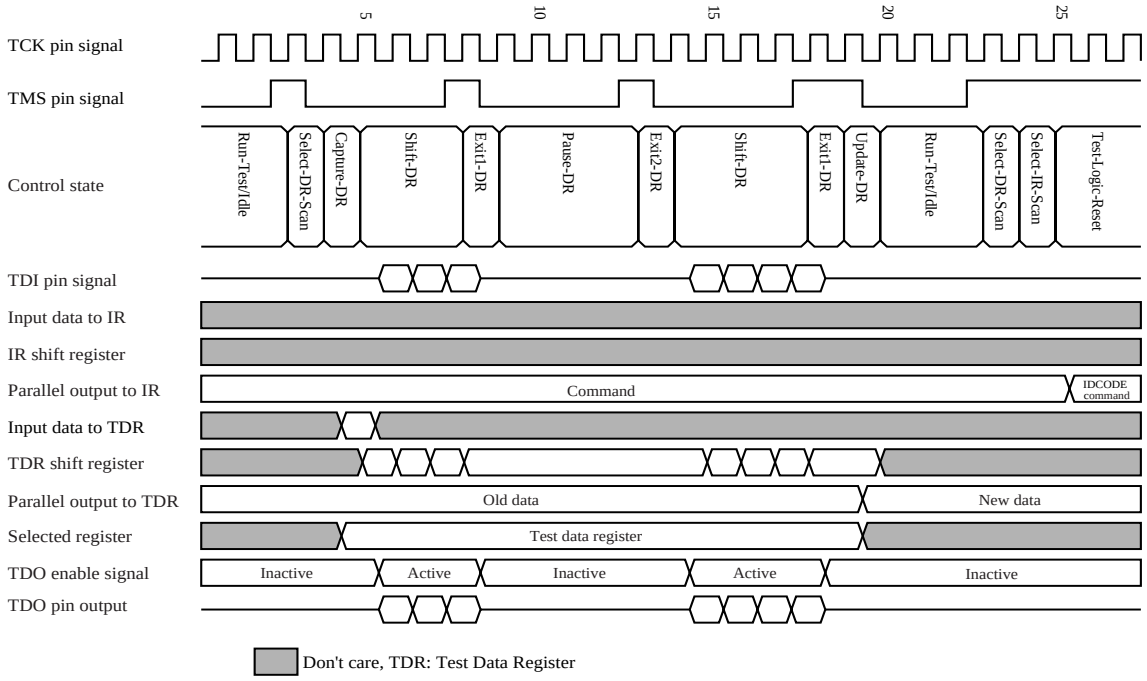


Fig 5 Operation of test logic (Data scan)

6.Reset of TAP controller

(1)Reset of TAP controller

1)TAP controller turns its state to Test-Logic-Reset by force of a power-on reset circuit during power on.

2)TAP controller cannot be reset by a system input signal such as system reset.

3)When TMS pin data keeps "H" level for five times continuously at the rising edge of TCK clock, TAP controller changes its state to Test-Logic-Reset.

4)TAP controller turns its state to Test-Logic-Reset by force when $\overline{\text{TRST}}$ pin is in the "L" level.

7.Instruction register

(1)Instruction register

1)Command to be shift-input to the instruction register is changed only in the Update-IR or Test-Logic-Reset state.

2)The data of serial input to and serial output from the instruction register are the same.

3)In the state of Capture-IR, the shift register part of this register is loaded fixed logic value "001". (Binary LSB is "1".)

4)For the state of Test-Logic-Reset, the parallel register part of this register is set fixed logic value "001". (Binary LSB is "1".)

5)When this register is read, the data is output from MSB to LSB in TDO pin at the falling edge of TCK clock.

This boundary scan circuit can support the following four commands by the data specified by the instruction register.

1.EXTEST command
2.IDCODE command
3.SAMPLE command
4.BYPASS command

Instruction register			Command
D2	D1	D0	
0	0	0	EXTEST command
0	0	1	IDCODE command (The state after reset)
0	1	0	SAMPLE command
0	1	1	Not used (CLAMP-IO command)
1	0	0	Not used (INTEST command)
1	0	1	Not used (BYPASS command)
1	1	0	Not used (BYPASS command)
1	1	1	BYPASS command

1.EXTEST command (Table 2)

The open/short test of the input pin and output pin of this device is available.
When this command is selected, the state of all signals to be driven from output pin of the system are defined completely by the data to be kept in parallel register part of boundary scan register. And all signal to be input from input pin of system is loaded into the shift register of boundary scan register.
Boundary scan register is connected between TDI pin and TDO pin in this operation.

2.IDCODE command (Table 3)

It is possible to confirm identification of this device and mount position.
When this command is selected, as input pin and output pin are connected with system circuit directly, operation of boundary scan circuit does not influence the operation of system circuit.
IDCODE register is connected between TDI pin and TDO pin in this operation.
IDCODE is output from TDO pin.
For the state of Test-Logic-Reset this command is selected.

3.SAMPLE command (Table 4)

In system operation of this device, data sampling and its evaluation are available.
When this command is selected, as input pin and output pin are connected with system circuit directly, operation of boundary scan circuit does not influence operation of system circuit.
Boundary scan register is connected between TDI pin and TDO pin in this operation.
Sampling data is output from TDO pin.

4.BYPASS command (Table 5)

Data transfer to next device is available without influence on this device.
When this command is selected, as input pin and output pin are connected with system circuit directly, operation of boundary scan circuit does not influence the operation of system circuit.
BYPASS register is connected between TDI pin and TDO pin in this operation.

Table 2. EXTEST control

Control state	IR	BR	BSR	IDR	TDI pin	TDO pin	Input pin	Output pin	System circuit	Notes
Run-Test/Idle	000	Keep	Keep	Keep	Connecting with serial input of BSR	Connecting with serial input of BSR	Connecting with parallel input of BSR	Connecting with parallel input of BSR	Not defined	
Select-DR-Scan										
Capture-DR			Load from input pin in parallel							
Shift-DR			Shift to TDO pin through BSR from TDI pin							
Exit1-DR			Keep							
Pause-DR										
Exit2-DR										
Update-DR			Change the state of output pin							

Table 3. IDCODE control

Control state	IR	BR	BSR	IDR	TDI pin	TDO pin	Input pin	Output pin	System circuit	Notes
Run-Test/Idle	001	Keep	Keep	Keep	Connecting with serial input of IDR	Connecting with serial input of IDR	Connecting with system circuit	Connecting with system circuit	System operation	
Select-DR-Scan										
Capture-DR				Load identification of this device in parallel						
Shift-DR				Shift to TDO pin through IDR from TDI pin						
Exit1-DR				Keep						
Pause-DR										
Exit2-DR										
Update-DR										

Table 4. SAMPLE control

Control state	IR	BR	BSR	IDR	TDI pin	TDO pin	Input pin	Output pin	System circuit	Notes
Run-Test/Idle	010	Keep	Keep	Keep	Connecting with serial input of BSR	Connecting with serial input of BSR	Connecting with system circuit	Connecting with system circuit	System operation	
Select-DR-Scan										
Capture-DR			Load from input and output part of system circuit							
Shift-DR			Shift to TDO pin through BSR from TDI pin							
Exit1-DR			Keep							
Pause-DR										
Exit2-DR										
Update-DR										

Table 5. BYPASS control

Control state	IR	BR	BSR	IDR	TDI pin	TDO pin	Input pin	Output pin	System circuit	Notes
Run-Test/Idle	111	Keep	Keep	Keep	Connecting with input of BS	Connecting with serial input of BR	Connecting with system circuit	Connecting with system circuit	System operation	
Select-DR-Scan										
Capture-DR		Load the data "0"			Not set-up					
Shift-DR		Shift to TDO pin through BSR from TDI pin			Connecting with input of BS					
Exit1-DR		Keep								
Pause-DR										
Exit2-DR										
Update-DR										

8.Bypass register

(1)The input data to bypass register is latched to change only the state of Shift-DR.
(2)The data of input and output of bypass register does not change.
(3)In the state of Capture-DR, this register is loaded fixed logic value "0". (Binary)
(4)When this register is read, the data is output from TDO pin on the falling edge of TCK clock.

9.Boundary scan register

1)The data of parallel register in boundary scan registers are latched to change only the state of Update-DR.
2)The data of input and output of boundary scan register does not change.
3)In the state of Capture-DR, the shift register part of this register is loaded from system input pin.
4)The data of the serial register part in the boundary scan register is shifted only in the state of Shift-DR.
5)When this register is read, the data is output from LSB to MSB through TDO pin at the falling edge of TCK clock.
6)Boundary scan register consists of 2 types systems.

● I type (All input pin)

Boundary scan register of this type consists of the circuit as shown in fig 6. Input pin is directly connected with system circuit. When input level is between V_{IH} min and V_{IL} max, input buffer is required of protecting against over-current.

● I/O type

Boundary scan register of this type consists of the circuit as shown in fig 7.In this type, this register is for output data from the pin to system circuit, signal enabled output of the pin and input data from the pin into system circuit. I/O type is applied for DIO1~DIO8 and DOI1~DOI8.

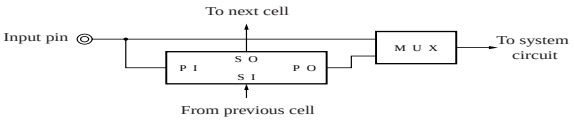


Fig6. I type cell

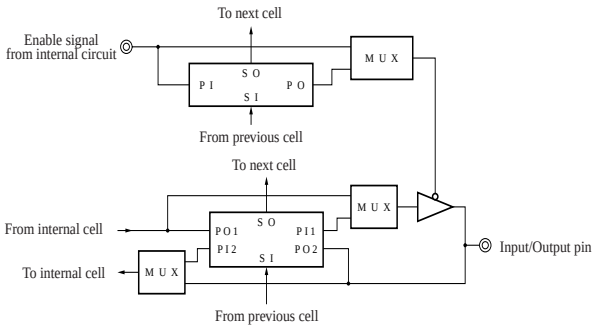


Fig7. I/O type cell

■ Connecting Table of Boundary Scan Register

BSR no.	Terminal no.	Symbol	BSR symbol	Terminal attribute	ID code	Previous BSR symbol
—	51	TDI	—	I	—	—
—	52	TMS	—	I	—	—
—	53	TCK	—	I	—	—
1	55	CS	CS	I	0	(TDI)
2	56	$\overline{WE}$	WE	I	0	CS
3	58	SIC	SIC	I	0	WE
4	59	$\overline{WS}$	WS	I	1	SIC
5	60	NC	OP1	I	0	WS
6	67	A9	A9	I	1	OP1
7	68	A10	A10	I	0	A9
8	70	A11	A11	I	0	A10
9	71	A12	A12	I	0	A11
10	73	A13	A13	I	0	A12
11	74	A14	A14	I	0	A13
12	75	A15	A15	I	0	A14
13	78	A16	A16	I	0	A15
14	79	A17	A17	I	0	A16
15	80	DIO5	DIO5	I/O	0	A17
16	82	DIO6	DIO6	I/O	0	DIO5
17	83	DIO7	DIO7	I/O	1	DIO6
18	85	DIO8	DIO8	I/O	0	DIO7
19	91	DOI5	DOI5	I/O	0	DIO8
20	93	DOI6	DOI6	I/O	1	DOI5
21	94	DOI7	DOI7	I/O	0	DOI6
22	96	DOI8	DOI8	I/O	0	DOI7
23	97	A0	A0	I	0	DOI8
24	98	A1	A1	I	0	A0
25	1	A2	A2	I	0	A1
26	2	A3	A3	I	1	A2
27	3	A4	A4	I	1	A3
28	5	A5	A5	I	0	A4
29	6	A6	A6	I	0	A5
30	8	A7	A7	I	1	A6
31	9	A8	A8	I	0	A7
32	17	NC	OP2	I	1	A8
33	18	$\overline{CE}$	CE	I	—	OP2

■ Connecting Table of Boundary Scan Register (cont.)

BSR no.	Terminal no.	Symbol	BSR symbol	Terminal attribute	ID code	Previous BSR symbol
34	20	V_{DD2}	OP3	I	—	CE
35	21	SOC	SOC	I	—	OP3
36	23	$\overline{RS}$	RS	I	—	SOC
37	24	$\overline{DOCTL}$	DOCTL	I	—	RS
38	25	$\overline{OE}$	OE	I	—	DOCTL
39	—	—	(DIC)	—	—	OE
40	—	—	(DOC)	—	—	(DIC)
41	29	$\overline{DIOS}$	DIOS	I	—	(DOC)
42	30	DOI4	DOI4	I/O	—	DIOS
43	32	DOI3	DOI3	I/O	—	DOI4
44	33	DOI2	DOI2	I/O	—	DOI3
45	35	DOI1	DOI1	I/O	—	DOI2
46	41	DIO4	DIO4	I/O	—	DOI1
47	43	DIO3	DIO3	I/O	—	DIO4
48	44	DIO2	DIO2	I/O	—	DIO3
49	46	DIO1	DIO1	I/O	—	DIO2
—	47	TDO	—	O	—	DIO1
—	48	$\overline{TRST}$	—	I	—	—

● Connecting sequence of boundary scan register

TDI pin → CS pin → WE pin → SIC pin • • •
• • • → DIO2 pin → DIO1 pin → TDO pin

Notes) BSR : Boundary scan register
<TDI> : Input signal of test data
I : Input pin (Used BSR of input)
I/O : Input and output pin (Used BSR of input and output)
O : Output pin
(DIC) : BSR of output control signal for DIOn
(DOC) : BSR of output control signal for DOIn

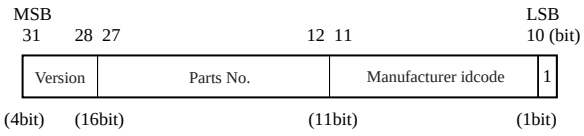


Fig 8 IDCODE register

10.IDCODE register

1)The input data to IDCODE register is latched to change only the state of Shift-DR.
2)The data of input and output of IDCODE register does not change.
3)In the state of Capture-DR, this register is loaded fixed logic value of 32-bit. (Binary)
4)When this register is read, the data is output from TDO pin at the falling edge of TCK clock.
5)IDCODE register consists as shown in figure 8.

- Version information is shown by 4-bit unit. Version No. is incremented from "0001" by every version up.
- Information of parts No. is specified by 16-bit binary code. Parts No. is shown of the "0100000000001001".
- Information of manufacturer idcode is specified by 11-bit binary code. This code is shown of JEDEC code. ("00000110010")

11.Specification of boundary scan circuit

(1)Specification of boundary scan circuit

Parameter	Symbol	MN47V07AF		Unit	Notes
		Min.	Max.		
TCK Setup Time from $\overline{\text{TRST}}$	t_{TRS}	10		ns	
TCK Hold Time from $\overline{\text{TRST}}$	t_{TRH}	10		ns	
$\overline{\text{TRST}}$ Pulse Width	t_{TRP}	20		ns	
TCK Pulse Width	t_{TCP}	80		ns	
TCK Cycle Time	t_{TCS}	200		ns	
TMS Setup Time	t_{TMS}	10		ns	
TMS Hold Time	t_{TMH}	30		ns	
TDI Setup Time	t_{TDS}	10		ns	
TDI Hold Time	t_{TDH}	30		ns	
TDO Hold Time	t_{TOH}	10		ns	
TDO Low Impeadance Time	t_{TLZ}		100	ns	
TDO High Impeadance Time	t_{THZ}		100	ns	
TCK Access Time	t_{TOA}		100	ns	

● BOUNDARE SCAN CYCLE