3Mbit 3Ports FIFO MEMORY

P/N: MN4795F

The technical information described herein provides the typical characteristics and the application circuit of a respective product, not intended to guarantee or permit a license for the industrial property rights.

When the mounting this device rotated 90˚ or 270˚ on the board is executed, short between V_{DD} and V_{SS} is occurred, and break down of this device and this system may be occurred. So that, please take care of mounting this device.

■ Request for your special attention and precautions in using the technical information and semiconductors described in this book.

(1) An export permit needs to be obtained from the competent authorities of the Japanese Government if any of the products or technologies described in this book and controlled under the "Foreign Exchange and Foreign Trade Control Law" is to be exported or taken out of Japan.

(2) The Technical -information described in this book is limited to showing representative characteristics and applied circuit examples of the products. It does not constitute the warranting of industrial property, the granting of relative rights, or the granting of any license.

(3) The products described in this book are intended to be used for standard applications or general electronic equipment (such as office equipment, communication equipment, measuring instruments and household appliances). Consult one of our sales offices in advance for the following applications:

- Special applications (such as airplanes, aerospace, traffic control equipment, combustion equipment, life support systems and safety devices) in which special quality and reliability are required, and the failure or malfunction of the products may directly jeopardize life or harm the human body.
- Any applications other than the standard applications intended.

(4) When designing your equipment, comply with the guaranteed values, in particular those of maximum rating, the range of operating power supply voltage and heat radiation characteristics. Otherwise, we will not be liable for any defect which may arise later in your equipment.

Even when the products are used within the guaranteed values, redundant design is recommended, so that such equipment may not violate relevant laws or regulations because of the function of our products.

(5) When vacuum packing is required for the products, make sure of the details of the warranty. Observe the conditions (including shelf life and after-unpacking standby time) in their use.

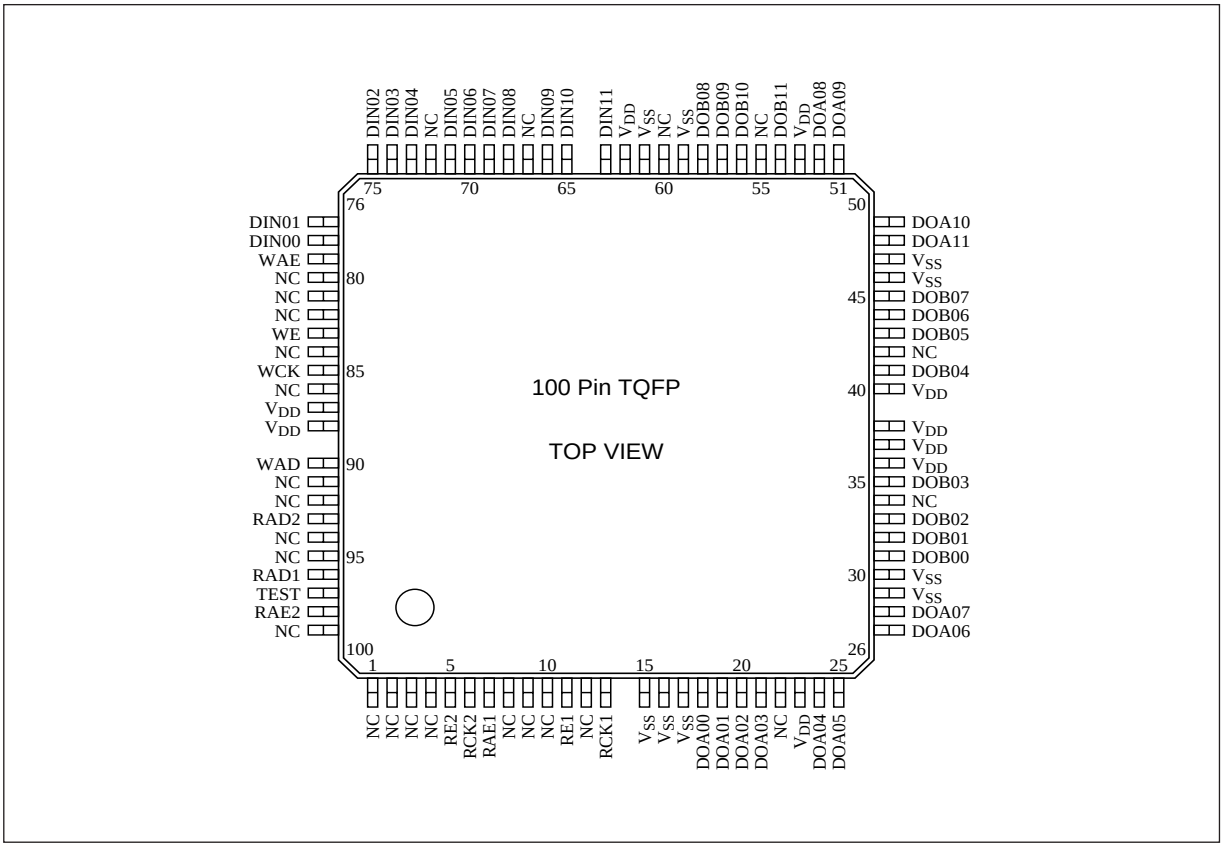
■ Description

The MN4795F is a 3Mbit 3Ports FIFO (First In First Out) memory which has one serial WRITE port and two serial READ ports. Manufactured with MEC's advanced CMOS processing technology and circuit configuration, a high speed, low a power dissipation and a wide operating range have been realized.

■ Features

- Organization ; 768dot × 313line × 12bit × 1 (serial write port)
  768dot × 313line × 12bit × 2 (serial read port)
- High Speed FIFO operation ; Serial access time : 60ns (max.)
  Serial cycle time : 70ns (min.)
- Each WRITE/READ operation is possible asynchronously and synchronously
- Random Line Access
- Self refresh function incorporated
- Power Supply voltage ; 3.0±0.3V
- Operating Current ; Max.40mA
- Package ; 100pin TQFP

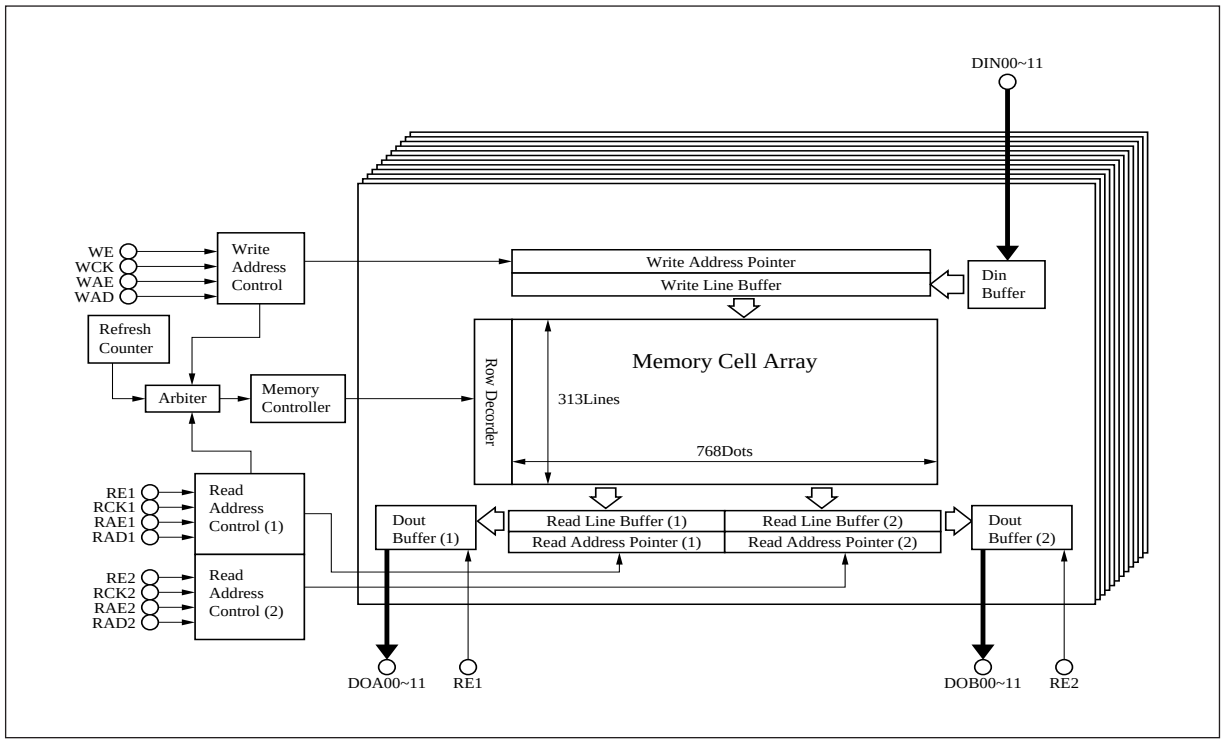
■ Pin Assignment



■ Pin Names

Symbol	Pin name	Symbol	Pin name
WCK	Write Clock Input	RE2	R2port Read Enable Input
WE	Write Enable Input	RAD2	R2port Read Address Input
WAD	Write Address Input	RAE2	R2port Read Address Enable Input
WAE	Write Address Enable Input	DOB00~11	R2port Data Output
DIN00~11	Data Input	V_{DD}	Power Supply (3.3V)
RCK1	R1port Read Clock Input	V_{SS}	Power Supply (0.0V)
RE1	R1port Read Enable Input	TEST	Testing Pin
RAD1	R1port Read Address Input	NC	No Connection
RAE1	R1port Read Address Enable Input		
DOA00~11	R1port Data Output		
RCK2	R2port Read Clock Input		

■ Block Diagram



■ PIN Description

● Write Clock Input Pin [WCK]

This is a serial write clock input pin. When WE is “H”, write action is worked synchronously with WCK and internal write address pointer increases at the same time.

● Write Enable Pin [WE]

This is an input pin for controlling write action and write address pointer. When WE is “H”, write address pointer becomes enable and internal write address pointer increases synchronously with WCK. When WE is “L”, this becomes disable and the pointer stops at that time. Write reset action is worked by rising “H”level of WE that is fetched by rising edge of WCK. When write reset action is worked, write address pointer is reset and moved to the head of line.

● Write Address Pin [WAD]

This is a line address input pin for the write port. The line is expressed 9bits and is necessary to be input serially from A8 to A0. In 0~511 lines expressed 9bits, 0~312 lines are able to be used as line address and 313~511 lines are prohibited to be input. If 313~511 lines are input addresses, access to memory is not worked. Address is fetched by the rising edge of WCK when WAE is “H” level.

● Write Address Enable Input Pin [WAE]

This is an input pin for controlling line address of the write port. When WAE is “H”, line address becomes enable and the write line address is fetched from WAD.

● Data Input Pin [DIN00~11]

This is a 12 bit serial data input pin. The data is fetched by the rising edge of WCK when WE is “H” level.

■ PIN Description

● R1port Read Clock Input Pin [RCK1]

This is a R1port read clock input pin. When RE1 is “H” level, R1port read action is worked synchronously with RCK1 and the internal read address pointer increases at the same time.

● R1port Read Enable Input Pin [RE1]

This is an input pin for controlling R1port read and read address pointer. When RE1 is “H”, this becomes enable and internal read address pointer increases synchronously with RCK1. When RE1 is “L” level, this becomes disable and pointer stops at that time. R1port read reset action is worked by rising “H”level of RE1 that is fetched by rising edge of RCK1. When R1port read reset action is worked, R1port read address pointer is reset and moved to the head of line. If address is not input before reset action, the address increases with one line. If address is input, the read address is moved to the specified line address.

● R1port Read Address Input Pin [RAD1]

This is a R1port read address input pin. The line address expressed 9bits and is necessary to be input serially from A8 to A0. In 0~511 lines expressed 9bits, 0~312 lines are able to be used as line address and 313~511 lines are prohibited to be input. If 313~511 lines are input address, access to memory is not worked. Address is fetched by the rising edge of RCK1 during RAE1 is “H” level.

● R1port Read Address Enable Input Pin [RAE1]

This is an input pin for controlling line address input of R1 port. When RAE1 is “H”, this becomes enable and the read line address is fetched from RAD1.

● R1port Data Output Pin [DOA00~11]

These are R1 port serial data output pins. R1port data output is worked by the rising edge of RCK1 when RE1 is “H” level. When RE1 is “L” level, R1 port data output pin becomes Hi-Z.

● R2port Read Clock Input Pin [RCK2]

This is a R2 port read clock input pin.When RE2 is “H” level, R2 port read action is worked synchronously with RCK2 and internal read address pointer increases at the same time.

● R2port Read Enable Input Pin [RE2]

This is an input pin for controlling R2 port read and read address pointer. When RE2 is “H”, this becomes enable and internal read address pointer increases synchronously with RCK2. When RE2 is “L” level, this becomes disable and pointer stops at that time. R2port read reset action is worked by rising “H”level of RE2 that is fetched by rising edge of RCK2. When R2port read reset action is worked, R2port read address pointer is reset and moved to the head of line. If address is not input before reset action, the address increases with one line. If address is input, the read address is moved to the specified line address.

● R2port Read Address Input Pin [RAD2]

This is a R2port read address input pin. The line address expressed 9bits and is necessary to be input serially from A8 to A0. In 0~511 lines expressed 9bits, 0~312 lines are able to be used as line address and 313~511 lines are prohibited to be input. If 313~511 lines are input address, access to memory is not worked. Address is fetched by the rising edge of RCK2 during RAE2 is “H” level.

■ PIN Description

● R2port Read Address Enable Input Pin [RAE2]

This is an input pin for controlling line address input of R2 port. When RAE2 is “H”, this becomes enable and the read line address is fetched from RAD2.

● R2port Data Output Pin [DOB00~11]

These are R2 port serial data output pins. R2port data output is worked by the rising edge of RCK2 when RE2 is “H” level. When RE2 is “L” level, R2 port data output pin becomes Hi-Z.

● Testing Pin [TEST]

This is a testing pin for special use. In normal operation, this pin should be fixed to “H” level.

■ Memory Operation

● WRITE

• Write Operation

When WE input is in "H" level, 12bit data of DIN00~11 is input for one line unit with synchronizing with WCK. Input data is taken in to the location that the address pointer expresses at the rising edge of next WCK cycle after WCK cycle that WE input rises in "H" level.

• Write Line Increment Operation

When Write Reset operation is executed without the address input, the line address of next write operation is increased. When Write Reset operation is executed in the last line (Line 312th),WAD and WAE inputs are required for the address data input of "Line 0th" so that the address returns to the head line (Line 0th). Reset operation is executed by turning WE to "H" level at the rising edge of WCK. The data input of the new line is begun from the next WCK cycle succeeding to the WCK cycle when WE input goes "H" level.

Interval of Write Reset operations is required for more than 3.5 µs.

Write Reset operation should be executed after the 47th data is written.

• Write Line Random Access Operation

Write Line Random Access operation is executed by rising WAE to "H" level and by the serial address data input of WAD synchronously with the rising edge of WCK. Line address data, expressed 9bits of A8~A0, is taken in serially from A8 to A0 at the rising edge of WCK during WAE holds "H" level.(See Fig.5)

WAE input is required to be kept "H" level during taking A8 data to A0 data, and be fallen to "L" level at the next WCK after taking A0 data.

After Write Reset operation is executed succeeding to the address data input, write operation to the specified line address starts from the next WCK cycle after WE goes "H" level.

Address data input can be executed only once during the reset operations. Address data input is required to be executed, between at moving to new line by reset operation and at rising WE to "H" level in the next reset operation.

Interval of Write Reset operations is required for more than 3.5 µs.

Write Reset operation is required to be executed after the 47th data is written.

• In the case that more than the 769 data are input.

Data input after the 767th is discarded until the next Reset operation is executed and the line address is renewed.

● READ

• Read Operation

When RE1 input is in "H" level, 12bit data output of DOA00~11 of the address pointed word is executed for 1 line unit synchronously with RCK1. Access time of the DOA00~11 output is regulated from the rising edge of RCK1.

When RE2 input is in "H" level, 12bit data output of DOB00~11 of the address pointed word is executed for 1 line unit synchronously with RCK2. Access time of the DOB00~11 output is regulated from the rising edge of RCK2.

• Read Line Increment Operation

When Read Reset operation is executed without the address input, the line address of read operation is increased to the next line address. When Read Reset operation is executed in the last line (Line 312th), RAD1, RAD2, RAE1, and RAE2 inputs are required for the address data input of "Line 0th" so that the address returns to the head line (Line 0th).

Reset operation of R1 port is executed by giving "H" level to RE1 at the rising edge of RCK1. Data output from DOA00~11 of new line is begun from RCK1 cycle after rising RE1 to "H" level.

Reset operation of R2 port is executed by giving "H" level to RE2 at the rising edge of RCK2. Data output from DOB00~11 of new line is begun from RCK2 cycle after rising RE2 to "H" level.

Interval of Read Reset operations is required for more than 3.5 µs.

Read Reset operation should be executed after the 47th data is read out.

• Read Line Random Access Operation

Read Line Random Access operation of R1 port is executed by rising RAE1 to "H" level and by inputting the serial address data to RAD1 synchronously with the rising edge of RCK1. Line address data is expressed 9bits of A8~A0, and is taken in serially from A8 to A0 at the rising edge of RCK1 during RAE1 is "H" level. (See Fig.6) RAE1 input is required to be kept "H" level during taking in A8 to A0 data, and be fallen to "L" level at the next RCK1 after taking to A0 data.

After Read Reset operation is executed succeeding to the address data input, read operation of R1 port from the specified line address starts from the next RCK cycle after RE1 goes "H" level.

Address data input can be executed only once between the Reset operations. Address data input is required to be executed after outputting the 96th data after moving to new line by Reset operation. More than 3.5 µs interval is required between the rising of RCK1 after falling RAE1 to "L" level the succeeding to address data input and the rising of the first RCK after rising RE1 to "H" level for Reset operation.

Read Line Random Access operation of R2 port is executed by rising RAE2 to "H" level and by inputting the serial address data to RAD2 synchronously with the rising edge of RCK2. Line address data is expressed 9bits of A8~A0, and is taken in serially from A8 to A0 at the rising edge of RCK2 during RAE2 is "H" level. (See Fig.6) RAE2 input is required to be kept "H" level during taking in A8 to A0 data, and be fallen to "L" level at the next RCK2 after taking to A0 data.

After Read Reset operation is executed succeeding to the address data input, read operation of R2 port from the specified line address starts from the next RCK cycle after RE2 goes "H" level.

Address data input can be executed only once during the Reset operations. Address data input is required to be executed after outputting the 96th data after moving to new line by Reset operation. More than 3.5µs interval is required between the rising of RCK2 after falling RAE2 to "L" level the succeeding to address data input and the rising of the first RCK after rising RE1 to "H" level for Reset operation.

• In the case that more than 769 data are outputted.

Data output of 767th data continues until the next Reset operation is executed and the line address is renewed.

• New Data Read Access

In order to execute New Data Read Access, that is, read the data just after written, write address pointer should be kept ahead more than 1line+96 address from read address pointer.

• Old Data Read Access

In order to execute Old Data Read Access, that is, read the previously written data other than newly written, write address pointer should be kept between 0 and 47 address ahead from read address pointer.

• Asynchronous Write And Read Operation

In order to execute Asynchronous Write And Read Operation, write address should be always kept ahead more than 1line+96 address from read address.

• Indefinite Operation

When the address difference between write and read pointer is more than 48 address and less than 1line+95 address, output data is indefinite to specify new or old, however, the newly written data is stored correctly.

• Power On

More than 200 µs pause time is required for normal operation of the device after the power supply is on and its voltage level settles down. Dummy cycles are required to be executed for moving 1line of write address and read address by Reset operation on each port, because read address pointer and write address pointer is indefinite at the power on. And when write line address data and read line address data is input into WAE, WAD, RAE1, RAE2, RAD2, normal operation of write and read data can be executed after the next RESET operation.

■ Absolute Maximum Ratings (V_{SS}=0V)

Parameter	Symbol	Rating	Unit	Notes
Power Supply Voltage	V_{DD}	–0.5 ~ +4.6	V	
Input Voltage	V_{IN}	–0.5 ~ +4.6	V	
Output Voltage	V_{OUT}	–0.5 ~ +4.6	V	
Short Circuit Output Current	I_{OS}	50	mA	
Power Dissipation	P_D	1.0	W	1)
Operating Temperature	T_{OPR}	0 ~ +70	˚C	
Storage Temperature	T_{STR}	–55 ~ +125	˚C	

Stress greater than those listed under "Absolute Maximum Ratings" (ex. excess voltage input or reverse insertion) may affect reliability of the device and cause unusual heat, deterioration of characteristics or breakdown of the device.

1) Ta=25˚C

■ DC Operating Conditions (V_{SS}=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	2.7	3.0	3.3	V
Input High Voltage	V_{IH}	V_{DD}–0.3	V_{DD}	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	–0.3		0.5	V
Operating Temperature	Ta	0	25	70	˚C

■ DC Characteristics (V_{DD}=3.0V ± 0.3V, Ta=0 ~ +70˚C, V_{SS}=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Output High Voltage (I_{OH}= –100µA)	V_{OH}	V_{DD}×0.8		V_{DD}	V	
Output Low Voltage (I_{OL}= 100µA)	V_{OL}			0.4	V	
Input Leakage Current (V_{IH}=0 ~ V_{DD})	I_{LI}	–10		10	µA	
Output Leakage Current (V_{OUT}=0 ~V_{DD} RE1 = RE2 = "L")	I_{LO}	–10		10	µA	
Operating Current (Min. cycle operation, Output Pin is open, Ave.)	I_{DD1}			40	mA	
Standby Current ($\overline{WE}$ = RE1 = RE2 = "L" after Write / Read Reset operation)	I_{DD2}			10	mA	

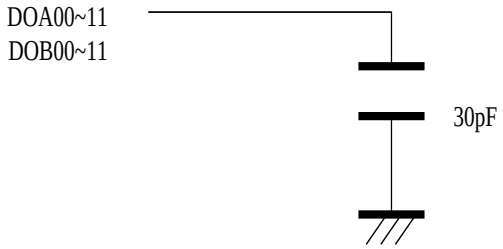
■ Capacitance (V_{DD}=3.0V ± 0.3V , f=1MHz , Ta=+25˚C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance	C_I			7	pF
Output Capacitance	C_O			10	pF

■AC Characteristics (V_{DD}=3.0V ± 0.3V, Ta=0 ~ +70˚C, V_{SS}=0V)

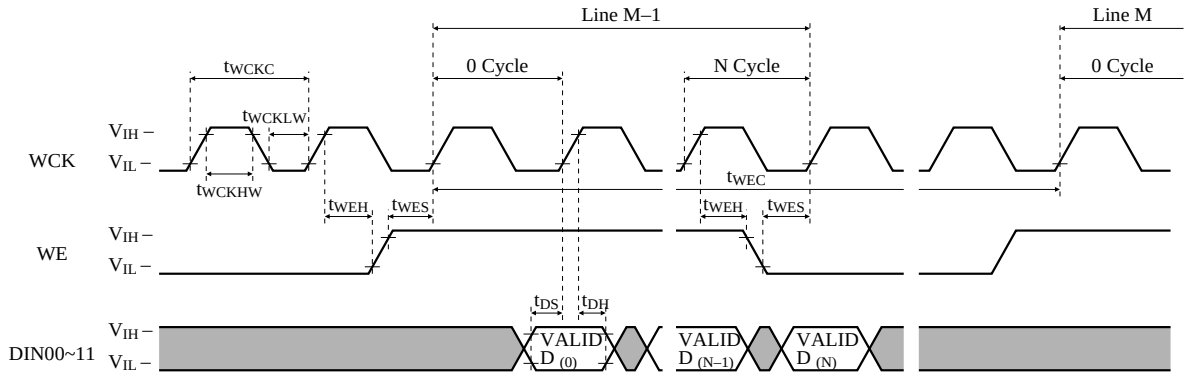
Parameter	Symbol	MN4795F		Unit	Notes
		Min.	Max.		
RCK1 Access Time	t_{AC1}		60	ns	
RCK2 Access Time	t_{AC2}		60	ns	
Output Hold Time from RCK1 Rise	t_{OH1}	10		ns	
Output Hold Time from RCK2 Rise	t_{OH2}	10		ns	
Output Disable Time of R1 Port	t_{OHZ1}		20	ns	
Output Disable Time of R2 Port	t_{OHZ2}		20	ns	
WCK Cycle Time	t_{WCKC}	70	150	ns	
WCK “H” Pulse Width	t_{WCKHW}	30		ns	
WCK “L” Pulse Width	t_{WCKLW}	30		ns	
RCK1 Cycle Time	t_{RCKC1}	70	150	ns	
RCK2 Cycle Time	t_{RCKC2}	70	150	ns	
RCK1 “H” Pulse Width	t_{RCKHW1}	30		ns	
RCK2 “H” Pulse Width	t_{RCKHW2}	30		ns	
RCK1 “L” Pulse Width	t_{RCKLW1}	30		ns	
RCK2 “L” Pulse Width	t_{RCKLW2}	30		ns	
Input Data Setup Time	t_{DS}	5		ns	
Input Data Hold Time	t_{DH}	15		ns	
$\overline{WE}$ Setup Time	t_{WES}	5		ns	
$\overline{WE}$ Hold Time	t_{WEH}	7		ns	
RE1 Setup Time	t_{RES1}	5		ns	
RE2 Setup Time	t_{RES2}	5		ns	
RE1 Hold Time	t_{REH1}	7		ns	
RE2 Hold Time	t_{REH2}	7		ns	
Write Address Setup Time	t_{WADS}	5		ns	
Write Address Hold Time	t_{WADH}	7		ns	
Read Address 1 Setup Time	t_{RADS1}	5		ns	
Read Address 2 Setup Time	t_{RADS2}	5		ns	
Read Address 1 Hold Time	t_{RADH1}	7		ns	
Read Address 2 Hold Time	t_{RADH2}	7		ns	
WAE Setup Time	t_{WAES}	5		ns	
WAE Hold Time	t_{WAEH}	7		ns	
RAE1 Setup Time	t_{RAES1}	5		ns	
RAE2 Setup Time	t_{RAES2}	5		ns	
RAE1 Hold Time	t_{RAEH1}	7		ns	
RAE2 Hold Time	t_{RAEH2}	7		ns	
Interval of Write Reset Operation	t_{WEC}	3.5		µs	
Interval of Read Reset 1 Operation	t_{REC1}	3.5		µs	
Interval of Read Reset 2 Operation	t_{REC2}	3.5		µs	
Transition Time (Rise and Fall)	t_T	5	30	ns	

2) Standard level of voltage for providing timings are V_{IH}=2.0V, V_{IL}=0.5V, V_{OH}=2.0V and V_{OL}=0.5V.
3) Input rise and fall times for AC measurement is 5ns.
4) Output loading condition

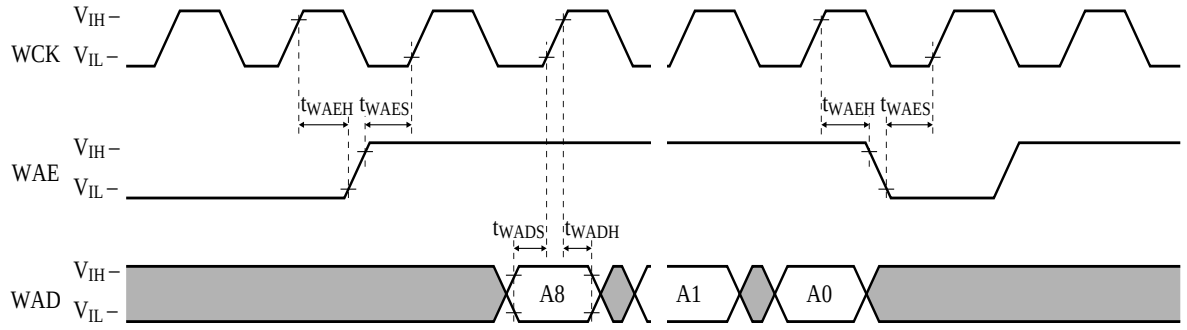


5) Usage not specified in this AC timing requirement may cause the destroy of the stored data.

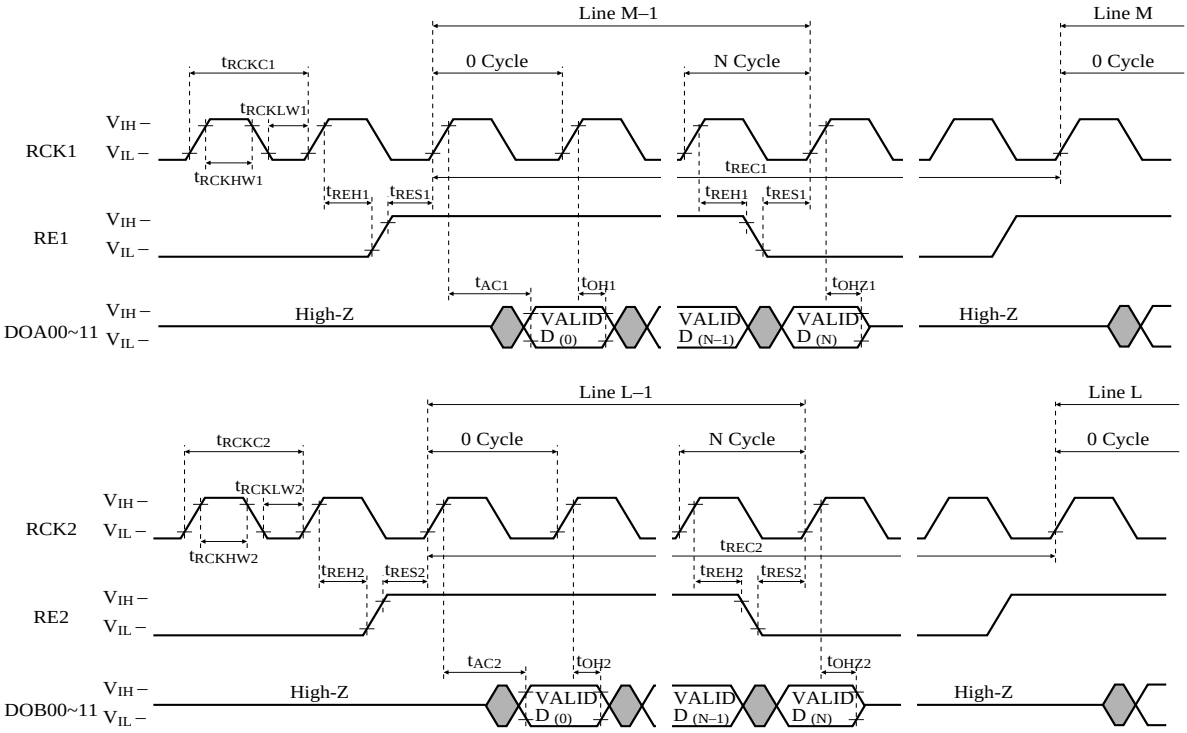
● WRITE PORT TIMING (WRITE RESET OPERATION, WRITE ENABLE)(N>47)



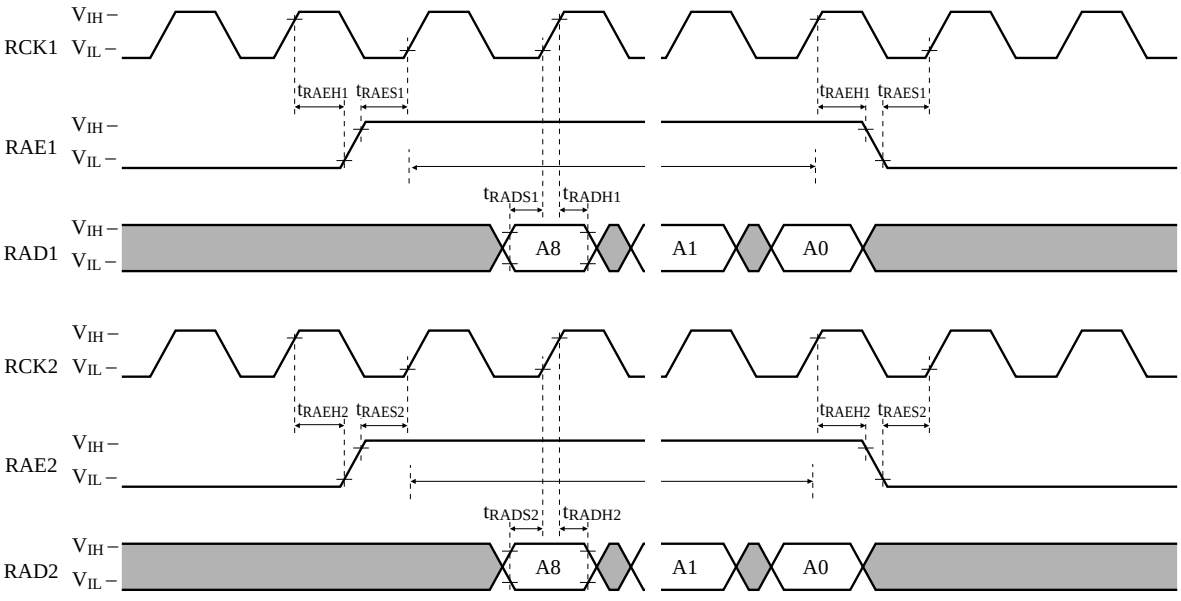
● WRITE PORT TIMING (WRITE ADDRESS ENABLE)



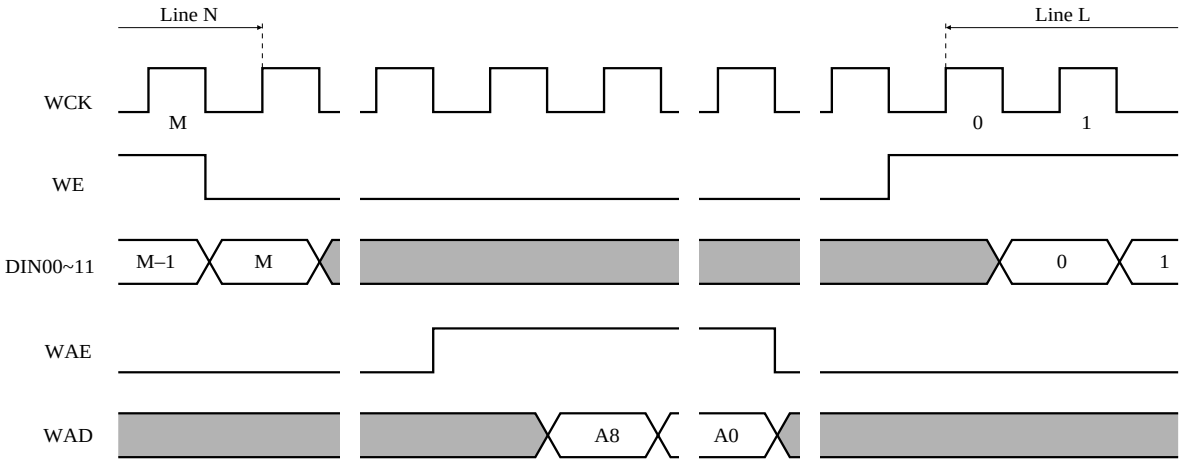
● READ PORT TIMING (READ RESET OPERATION, READ ENABLE)(N>47)



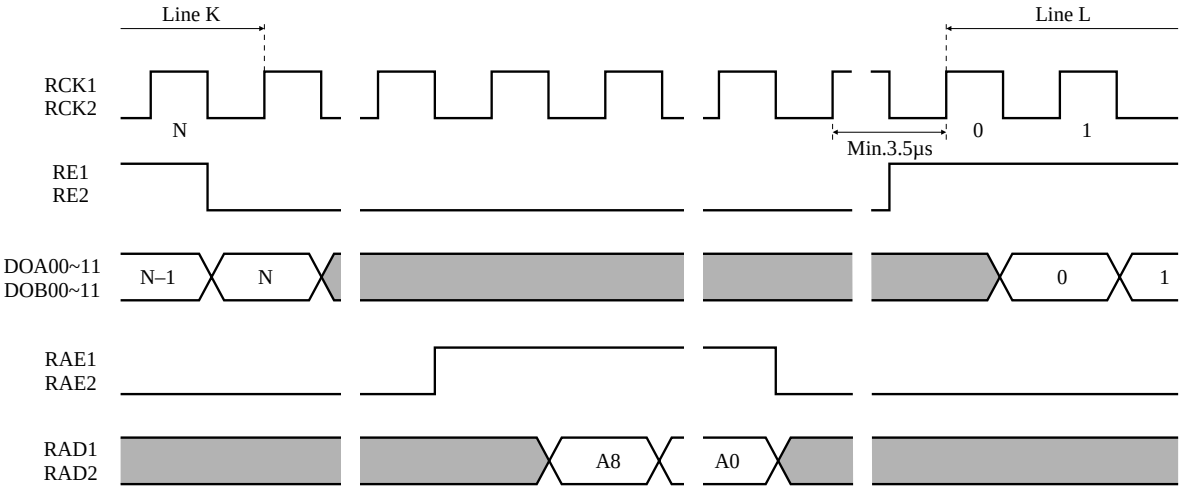
● READ PORT TIMING (READ ADDRESS ENABLE)



● WRITE LINE RANDOM ACCESS (M>47)



● READ LINE RANDOM ACCESS (N>96)



● NEW DATA READ ACCESS