

# MN3307

## 1024-Stage Ultra Low Voltage Operation BBD for Audio Signals

### ■ Overview

The MN3307 is a 1024-stage ultra low voltage operation BBD variable delay line in audio frequency range. The device operates on +3 V supply and provides a signal delay up to 51.2 ms and is suitable for use as reverberation effect of low voltage operation audio equipment such as portable stereo, radio cassette recorder and microphone.

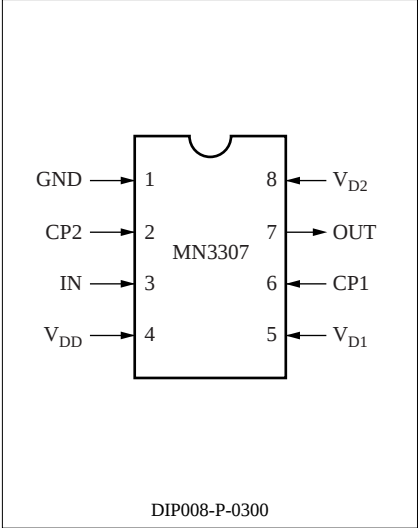
### ■ Features

- Variable signal delay of the audio signal : 1.024 to 51.2 ms
- Wide range of supply voltage : 1.8 to 5.0 V
- No insertion loss :  $L_i=0$  dB typ.
- Wide dynamic range :  $S/N=69$  dB typ.
- Low distortion :  $THD=0.6$  % typ. ( $V_i=0.22 V_{rms}$ )
- Clock frequency range : 10 to 200 kHz ( $1.8 V \leq V_{DD} < 4.0 V$ )  
10 to 500 kHz ( $4.0 V \leq V_{DD} \leq 5.0 V$ )
- N-channel 2-layer silicon gate process
- 8-Pin Dual-In-Line Plastic Package

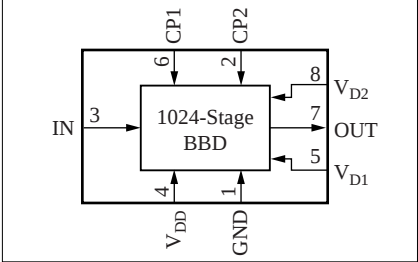
### ■ Applications

- Reverberation and echo effects of audio equipment such as radio cassette recorder, car radio, portable radio, portable stereo, echo microphone and Karaoke machine, etc.
- Sound effect of electronic musical instruments
- Variable or fixed delay of analog signals

### ■ Pin Assignment



### ■ Block Diagram



### ■ Pin Descriptions

| Pin No. | Symbol   | Pin Name           | Description                                                                                                                                                                          |
|---------|----------|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | GND      | Ground pin         | Connected to ground.                                                                                                                                                                 |
| 2       | CP2      | Clock input 2      | Basic clock pulse is applied to transfer electric charge of BBD.                                                                                                                     |
| 3       | IN       | Signal input pin   | Analog signal to be delayed is input. Most suitable DC bias should be applied to this pin.                                                                                           |
| 4       | $V_{DD}$ | $V_{DD}$ apply pin | Bias is applied to the gate of MOS transistor which is inserted in series with clock pulse input gate of the BBD transfer gate. Furthermore, voltage is supplied to step-up circuit. |
| 5       | $V_{D1}$ | $V_{D1}$ apply pin | The same phase clock pulse as CP1 is applied through capacitor.                                                                                                                      |
| 6       | CP1      | Clock input 1      | Clock pulse of inverted phase to CP2 is applied.                                                                                                                                     |
| 7       | OUT      | Output pin         | Composed signal of 1024th and 1025th stages is output.                                                                                                                               |
| 8       | $V_{D2}$ | $V_{D2}$ apply pin | The same phase clock pulse as CP2 is applied through capacitor.                                                                                                                      |

■ Absolute Maximum Ratings  $T_a=25^{\circ}\text{C}$

| Parameter                     | Symbol                                | Ratings       | Unit               |
|-------------------------------|---------------------------------------|---------------|--------------------|
| Pin voltage                   | $V_{DD}, V_{D1}, V_{D2}, V_{CP}, V_I$ | - 0.3 to +6.0 | V                  |
| Output voltage                | $V_O$                                 | - 0.3 to +6.0 | V                  |
| Operating ambient temperature | $T_{opr}$                             | -20 to +60    | $^{\circ}\text{C}$ |
| Storage temperature           | $T_{stg}$                             | -55 to +125   | $^{\circ}\text{C}$ |

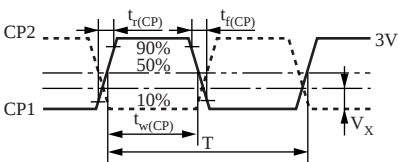
■ Operating Conditions  $T_a=25^{\circ}\text{C}$

| Parameter               | Symbol           | Conditions | min  | typ      | max                 | Unit |
|-------------------------|------------------|------------|------|----------|---------------------|------|
| Supply voltage          | $V_{DD}$         |            | +1.8 | +3.0     | +5.0                | V    |
| Clock voltage "H" level | $V_{CPH}$        |            |      | $V_{DD}$ |                     | V    |
| Clock voltage "L" level | $V_{CPL}$        |            |      | 0        |                     | V    |
| Clock input capacitance | $C_{CP}$         |            |      |          | 700                 | pF   |
| Clock frequency         | $f_{CP}$         |            | 10   |          | 200(500)*1          | kHz  |
| Clock pulse width       | $t_{w(CP)}^{*3}$ |            |      |          | 0.5T*2              |      |
| Clock rise time         | $t_{r(CP)}^{*3}$ |            |      |          | 500                 | ns   |
| Clock fall time         | $t_{f(CP)}^{*3}$ |            |      |          | 500                 | ns   |
| Clock cross point       | $V_X^{*3}$       |            | 0    |          | 0.3V <sub>CPH</sub> | V    |

Note) \*1 : ( ) :  $V_{DD}=4.0$  to  $5.0$  V

\*2 :  $T=1/f_{CP}$  (Clock period)

\*3 : Clock pulse waveforms

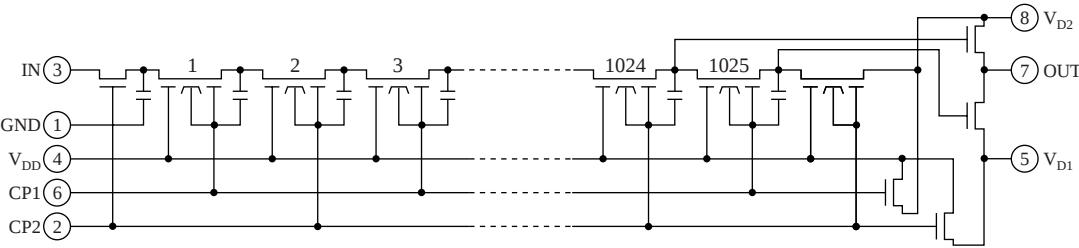


■ Electrical Characteristics  $V_{DD}=V_{CPH}=3\text{V}, V_{CPL}=0\text{V}, R_L=56\text{k}\Omega, \text{LPF} : f_C=20\text{kHz}, A_t=48\text{dB/oct.}, T_a=25^{\circ}\text{C}$

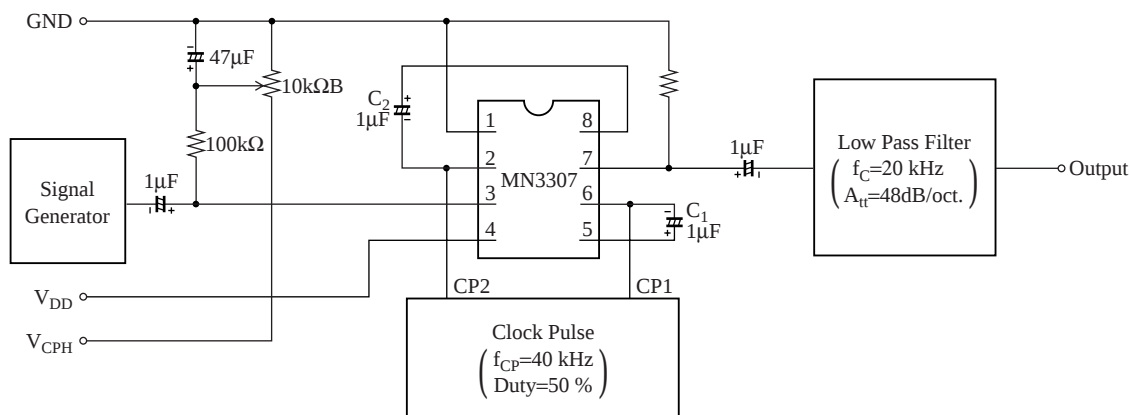
| Parameter                 | Symbol   | Conditions                                                                                  | min  | typ                        | max  | Unit              |
|---------------------------|----------|---------------------------------------------------------------------------------------------|------|----------------------------|------|-------------------|
| Supply current            | $I_{DD}$ | $f_{CP}=40$ kHz                                                                             |      | 0.05                       |      | mA                |
| Signal delay time 1       | $t_{D1}$ | $V_{DD}=1.8$ to $4.0$ V, $f_{CP}=10$ to $200$ kHz                                           |      | $\frac{N}{2 \cdot f_{CP}}$ |      | ms                |
| Signal delay time 2       | $t_{D2}$ | $V_{DD}=4.0$ to $5.0$ V, $f_{CP}=10$ to $500$ kHz                                           |      |                            |      |                   |
| Input signal frequency    | $f_i$    | $f_{CP}=40$ kHz, $V_i=0.22 V_{rms}$<br>Output attenuation $\leq 3$ dB (0 dB at $f_i=1$ kHz) | 11   |                            |      | kHz               |
| Input signal amplitude    | $v_i$    | $f_{CP}=40$ kHz, $f_i=1$ kHz, THD=2.5 %                                                     | 0.31 | 0.45                       |      | $V_{rms}$         |
| Insertion loss            | $L_i$    | $f_{CP}=40$ kHz, $f_i=1$ kHz, $V_i=0.22 V_{rms}$                                            | -4   | 0                          | 4    | dB                |
| Total harmonic distortion | THD      | $f_{CP}=40$ kHz, $f_i=1$ kHz, $V_i=0.22 V_{rms}$                                            |      | 0.6                        | 2.5  | %                 |
| Output noise voltage      | $V_{no}$ | $f_{CP}=100$ kHz, Weighted by "A" curve                                                     |      | 0.15                       | 0.25 | $\text{mV}_{rms}$ |
| Signal to noise ratio     | S/N      |                                                                                             |      | 69                         |      | dB                |

Note) \* :  $N=\text{BBD stages}$

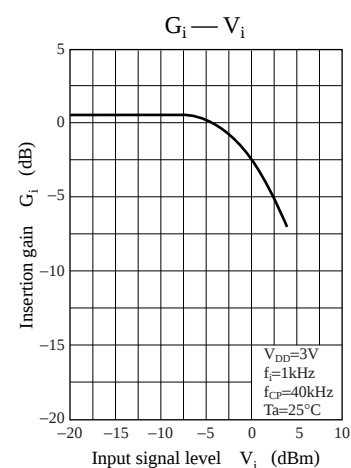
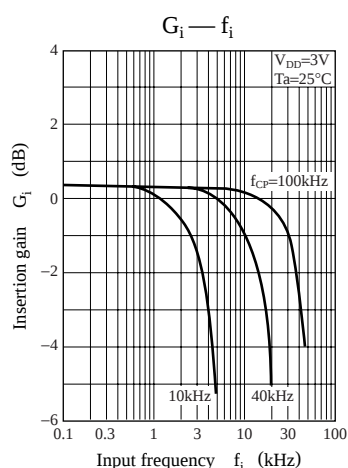
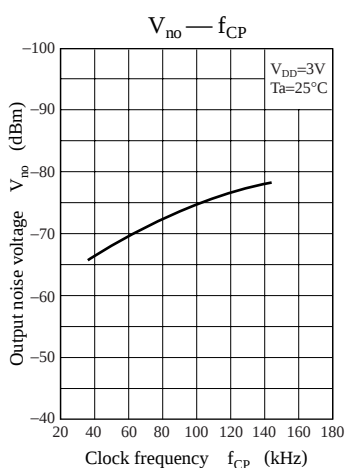
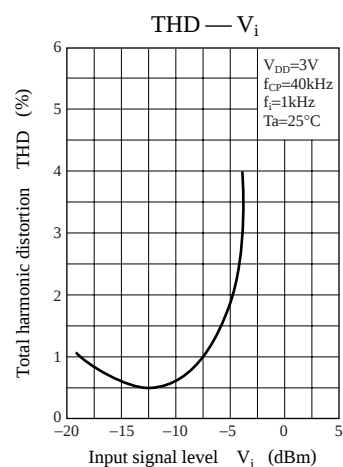
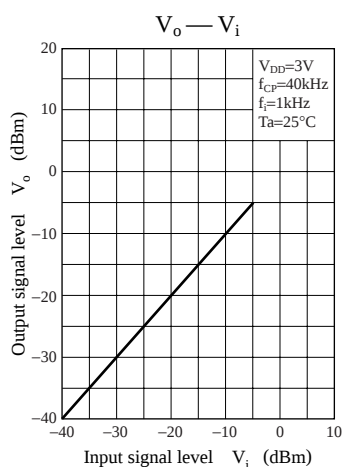
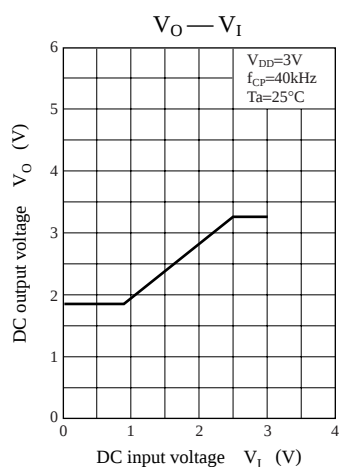
■ Circuit Diagram



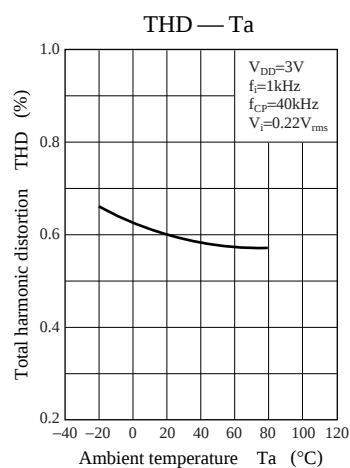
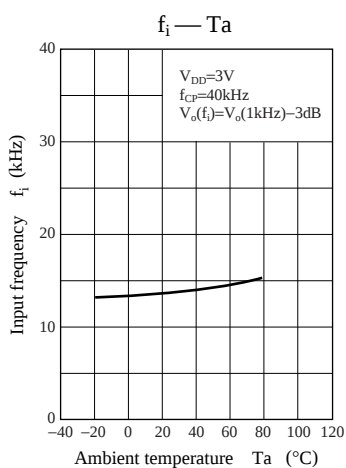
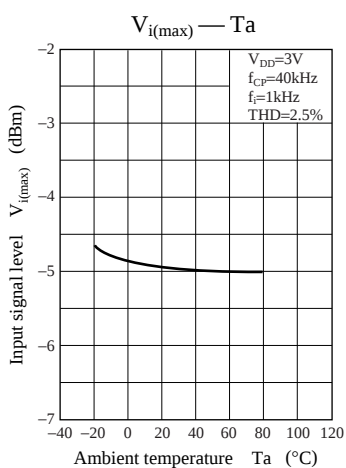
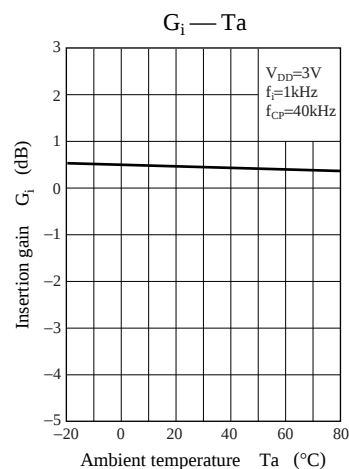
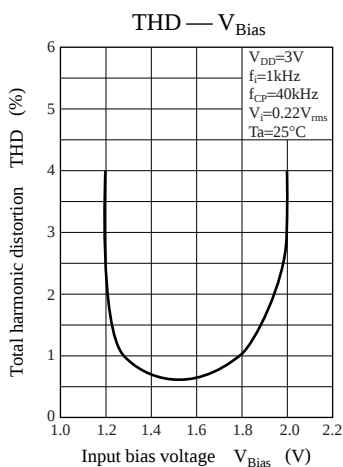
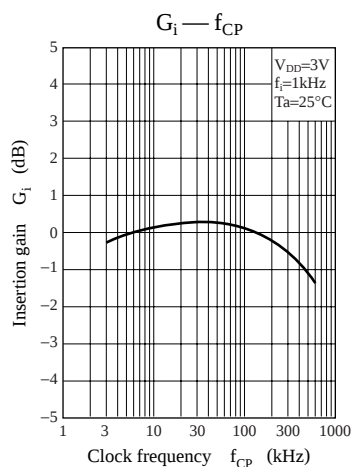
### Test Circuit



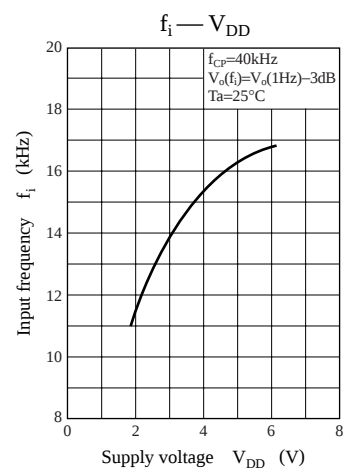
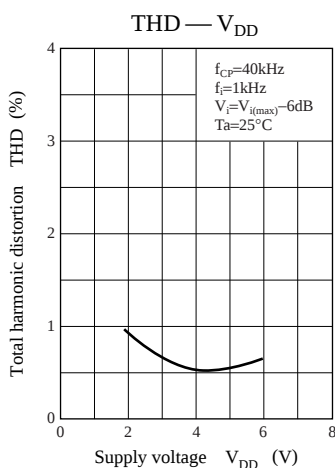
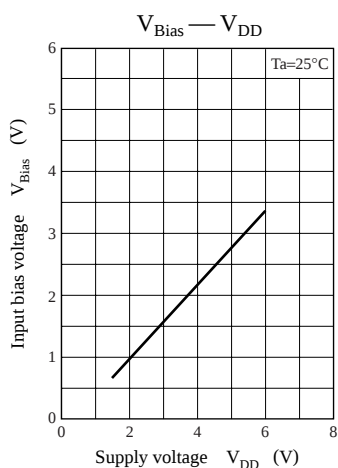
### Typical Characteristics



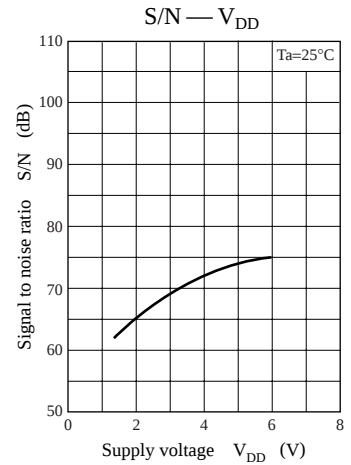
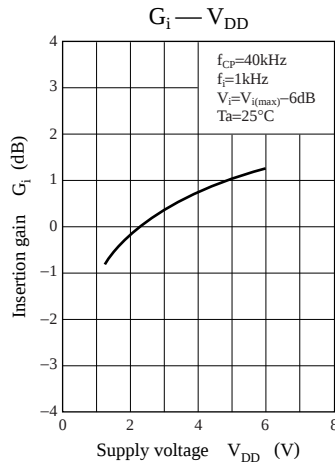
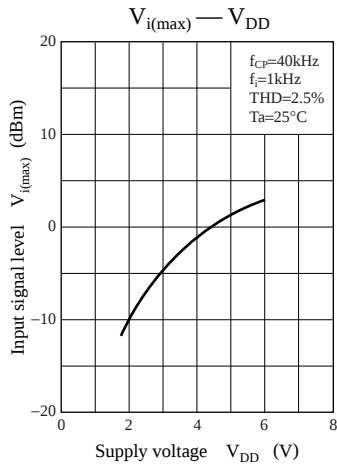
# Typical Characteristics (To be continued)



# Supply Voltage Characteristics



■ Supply Voltage Characteristics(To be continued)



■ Package Dimensions (Unit : mm)

- DIP008-P-0300

