MN3003

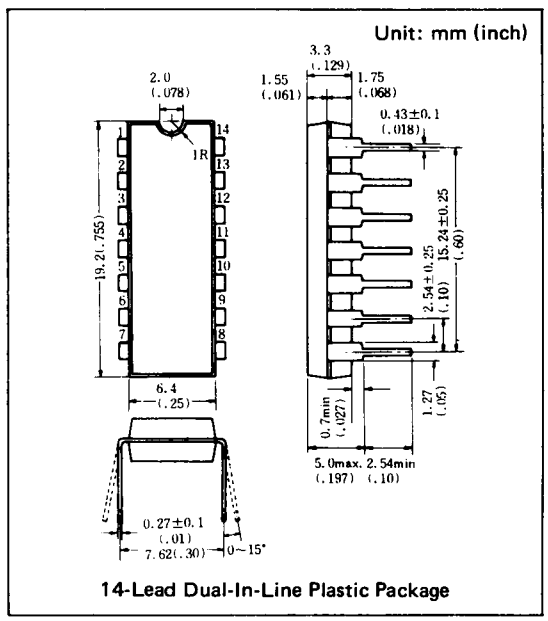
DUAL-64 STAGE BBD FOR LOW VOLTAGE OPERATION

■ General description

The MN3003 is a dual 64-stage BBD incorporating a clock generator on a single chip, which contains independent input, output and common clock terminals, as well as common power supply terminals. The MN3003 is operated by low power voltage of −9V.

The clock oscillation frequency is controlled by the external resistor and capacitor connected to CG_1, CG_2 and CG_3 terminals, and the MN3003 is suitably applied for short time delay since delay time of 0.16 ~ 3.2 ms can be obtained.

The MN3003 can be used as 128-stage in series connection and its output becomes twice as large in parallel connection, which offer space saving advantage.



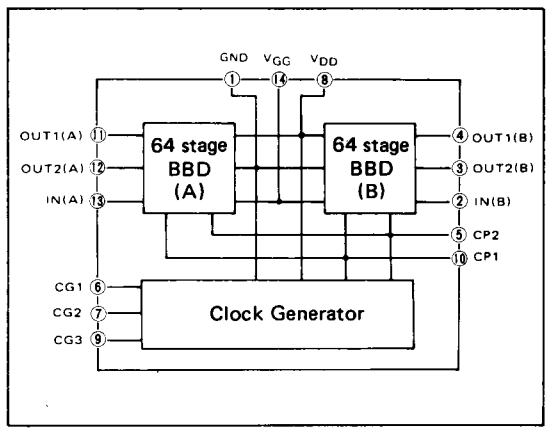
■ Features

- Variable delay line in audio frequency range: 0.16 ~ 3.2 ms.
- Built-in clock generator.
- P-channel silicon gate MOS.
- Wide frequency response: $f_i \simeq 0.3 \times f_{cp}$.
- Clock frequency range: 10 ~ 200KHz.
- Dynamic range: S/N ≃ 75dB typ.
- Low insertion loss: L_f = 3.5dB typ.
- Low noise: V_{no} = 0.14mVrms max.

■ Application

- Vibrato and chorus effects in electronic musical instruments.
- Reverberation effect of electronic musical instruments.
- Variable or fixed delay of analog signals.

■ Block Diagram



■ Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{GG}	−9, V_{DD} + 1	V
Signal Delay Time	t_D	0.16~6.4	ms
Total Harmonic Distortion	THD	0.5	%
Signal to Noise Ratio	S/N	68min.	dB

■ Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_I	−15～+0.3	V
Output Voltage	V_O	−15～+0.3	V
Operating Temperature	Topr	−20～+60	℃
Storage Temperature	Tstg	−55～+125	℃

■ Operating Conditions (Ta = 25°C)

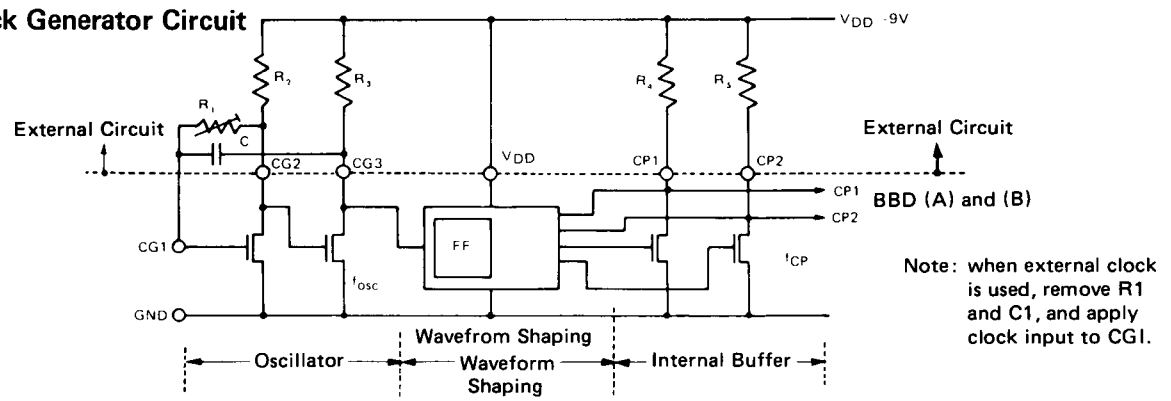
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}		−8.5	− 9	−9.5	V
Gate Supply Voltage	V_{GG}			$V_{DD}+1$		V
Clock Voltage "H" Level	V_{CPH}		0		−0.4	V
Clock Voltage "L" Level	V_{CPL}			V_{DD}		V
Clock Frequency	f_{CP}		10		200	kHz
Input DC Bias	V_{Bias}		−2.5		− 6	V

■ Electrical Characteristics (V_{DD} = −9V, V_{GG} = −8V, R_L = 100KΩ, R_2 = R_3 = 22KΩ, R_4 = R_5 = 2.2KΩ, C = 100pF, fcp = ½ f_{OSC} (adjustable by R_1), Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Signal Frequency	f_i	f_{CP} = 40kHz, V_i = 0.8Vrms 3dB down (0dB at f_i = 1kHz)	12			kHz
Input Signal Swing	V_i	f_{CP}=40kHz, f_i = 1 kHz, THD≦2.5%	0.8			Vrms
Insertion Loss	L_i	f_{CP}=40kHz, f_i = 1 kHz, V_i =0.8Vrms		3.5	7	dB
Total Harmonic Distortion	THD	f_{CP}=40kHz, f_i = 1 kHz, V_i =0.5Vrms		0.5	2.5	%
Noise Voltage	V_{no}	f_{CP}= 90kHz, Weighted by "A" curve			0.14	mVrms
Signal to Noise Ratio	S/N			75		dB

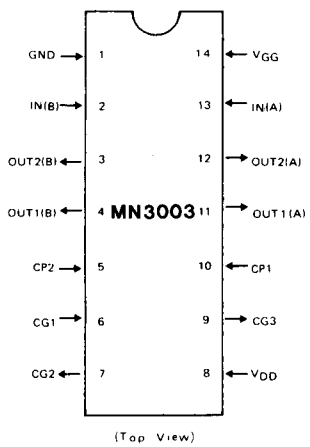
Note: Adjust input DC bias to the optimum value between −2.5 and −6 volts.

■ Clock Generator Circuit

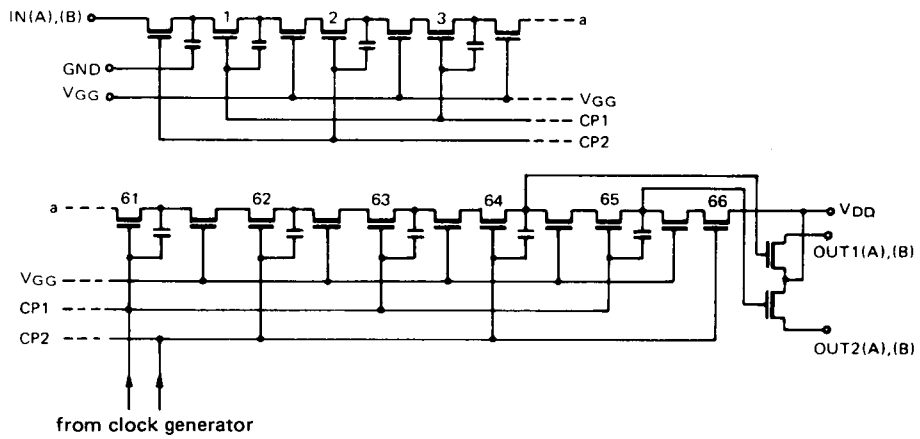


Note: when external clock is used, remove R1 and C1, and apply clock input to CGI.

■ Terminal Assignments

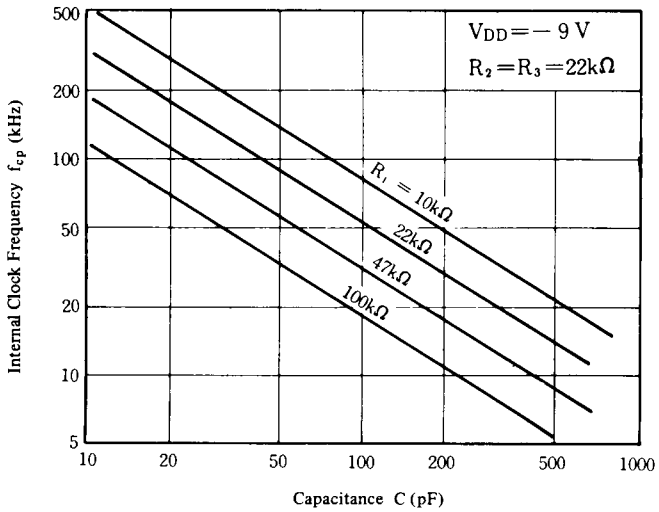


■ Circuit Diagram

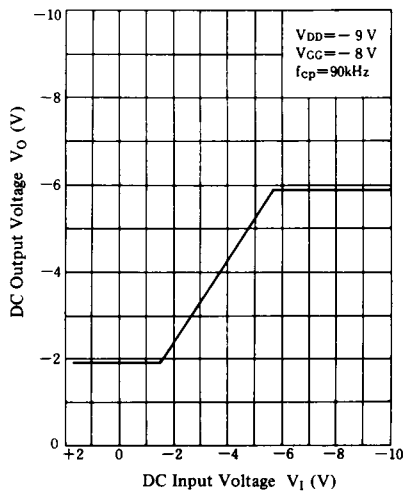


■ Typical Electrical Characteristic Curves

Clock Frequency Characteristics



VO—VI



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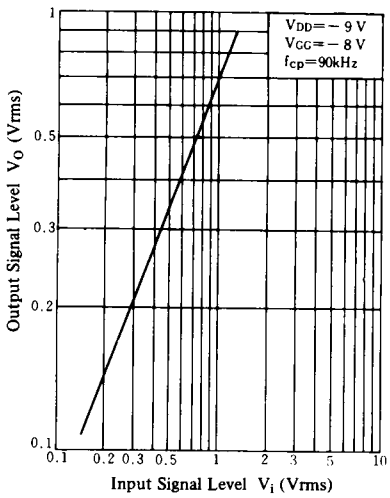
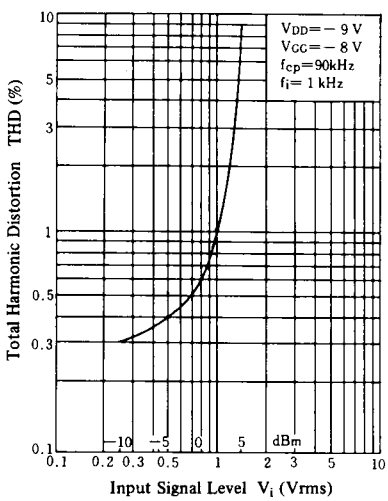
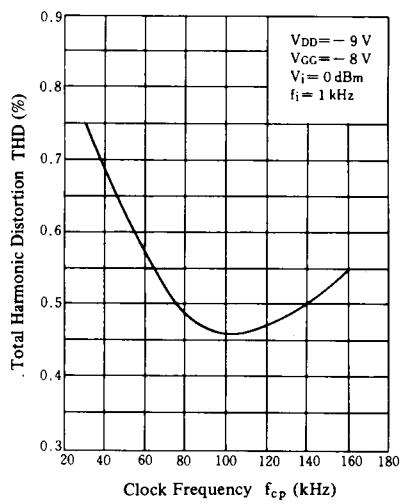


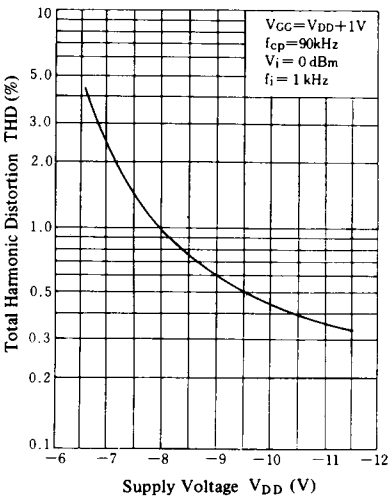
THD—Vi



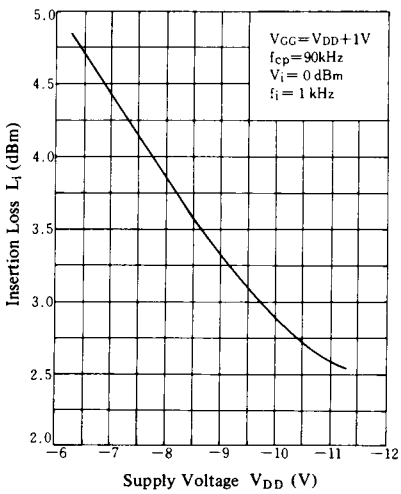
THD—fcp



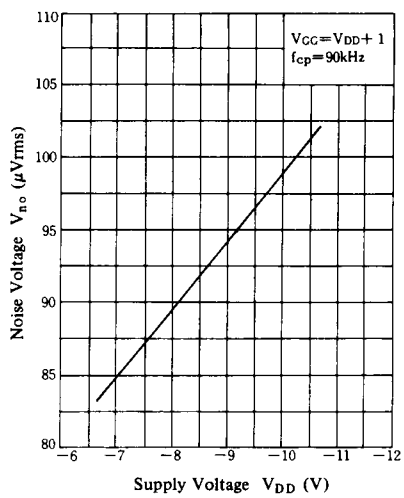
THD—VDD



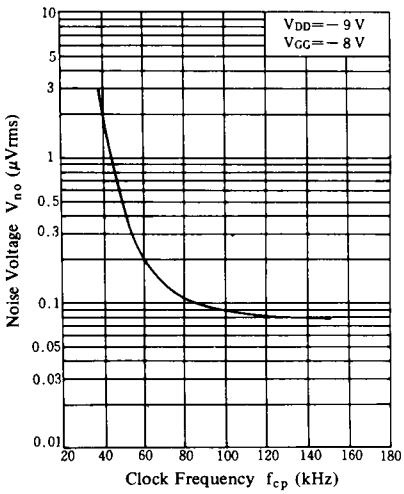
Li—VDD



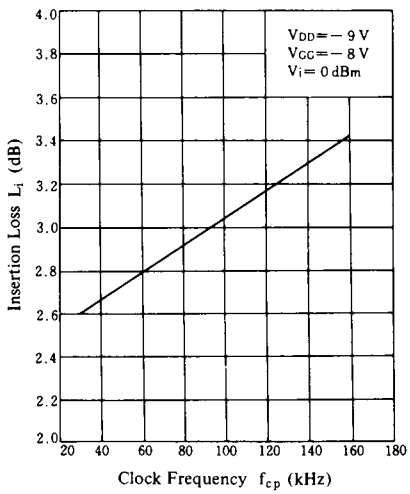
Vno—VDD



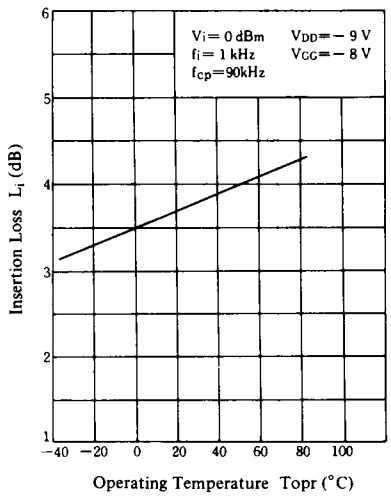
V_{no}—f_{cp}



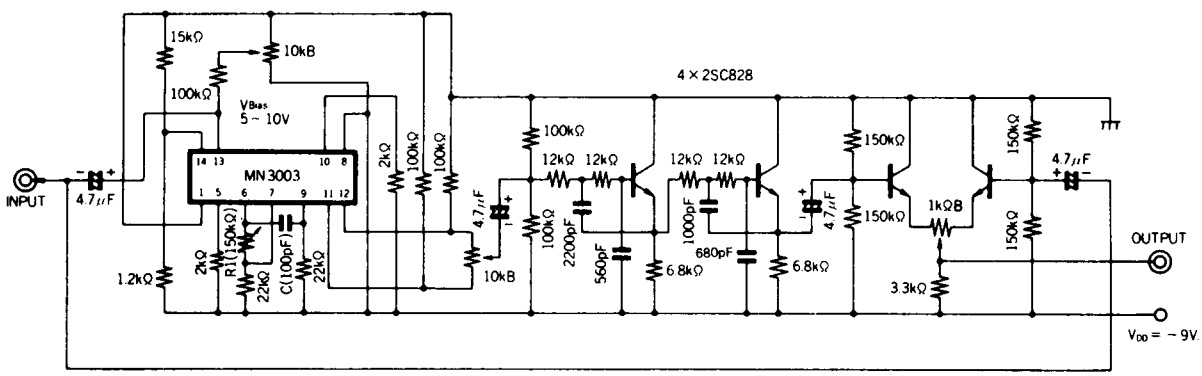
L_i—f_{cp}



L_i—Topr



■ Application Circuit



Chorus Effect Generation Circuit (Incorporating Clock Generator)