MN102LP36K / L36K / LP36Z / L36Z / LP36G / L36G / LP36D / L36D / L360C

Type	**MN102LP36K / L36K / LP36Z / L36Z / LP36G / L36G / LP36D / L36D / L360C** **(For MN102L360C are in production. LP36Z and L36Z, ES are available. The others are under development.)**
ROM (x8-bit / x16-bit)	256K (OTP) / 256K / 128K (OTP) / 128K / 128K (OTP) / 128K / 64K(OTP) / 64K / External
RAM (x8-bit / x16-bit)	10K / 10K / 10K / 10K / 5K / 5K / 5K / 5K / 5K
Minimum Instruction Execution Time	**100ns (at 4.5 to 5.5V, 20MHz)** **200ns (at 2.7 to 3.6V, 10MHz)**
Interrupts	• RESET • Watchdog • Timer Counter 0 to 5 • Fixed-length Serial ch 0,1 Transmission • Fixed-length Serial Ch 0,1 Reception • Timer Counter 6 to 7 • Timer Counter 6 to 7 Compare Capture A • Timer Counter 6 to 7 Compare Capture B • ACT Transfer Finish • External 0 to 7 • Serial ch 0,1 Transmission • Serial ch 0,1 Reception • NMI Pin • A/D Conversion Finish
Timer Counter	**Timer Counter 0: 8-bit x 1** (Timer Output, Event Count) Clock Source 1/1, 1/128 of System Clock, 1/4 of Low Speed Clock, External Clock Interrupt Source Timer Counter 0 Underflow **Timer Counter 1: 8-bit x 1** (Timer Output, Even Count, A/D Conversion Start) Clock Source . . . System Clock, 1/4 of Low Speed Clock, External Clock, Timer Counter 0 Output Interrupt Source.. Timer Counter 1 Underflow **Timer Counter 2 to 3: 8-bit x 1** (Timer Output, Event Count, UART Baud Rate Generation) Clock Source .System Clock, External Clock, Timer Counter 0 Output, Timer Counter 1, 2 Output Interrupt Source Timer Counter 2, 3 Underflow **Timer Counter 4,5: 8-bit x 1** (Timer Output, Event Count) Clock Source . . . . . 1/4 of Low Speed Clock, External Clock, Timer Counter 0 Output, Timer Counter 3, 4 Output Interrupt Source Timer Counter 4, 5 Underflow **Timer Counter 6, 7: 16-bit x 1** (Timer Output, Event Count, Input Capture, Output Compare, PWM Output, 2-phase Encoder Input) Clock Source System Clock, External Clock, Timer Counter 4, 5 Output Interrupt Source . Coincidence with Compare Capture A or at Capture, Coincidence with Compare Capture B or at Capture, Underflow of Timer Counter 6, 7 (Connectable) Timer Counter 0 to 5
Serial Interface	**Serial 0: 7, 8-bit x 1** (Common use with UART, Transfer Direction of MSB/LSB Selectable) Clock Source. 1/16 of Timer Counter 2, 1/16 of Timer Counter 3, External Clock, 1/2 of Timer Counter 2 I^2C Mode (Master Transmission/Reception is Possible in The Single Master System) **Serial 1: 7, 8-bit x 1** (Common use with UART, Transfer Direction of MSB/LSB Selectable) Clock Source . 1/16 of Timer Counter 2, 1/16 of Timer Counter 3, External Clock, 1/2 of Timer Counter 3) I^2C Mode (Master Transmission/Reception is Possible in The Single Master System) **Fixed-length serial 0: 8-bit x 1** Clock Source External Clock Sending Direction LSB **Fixed-length serial 1: 8-bit x 1** Clock Source. . External Clock Sending Direction LSB

I/O Pins	**I/O**	**104** **83**	• Common use 16 (by 8-bits), 8 (by 4-bits), 80 (by-bit) (all models except MN102L360C) • Common use 8 (by 4-bits), 75 (by-bit) (MN102L360C)
A/D Inputs			8-bit x 8ch (with S/H)
D/A Inputs			8-bit x 2ch
PWM			16-bit x 2ch
Notes			Burst ROM interface support, ATC (support between serial 0 ch and built-in RAM)
Package			LQFP128-P-1818C

Electrical Characteristics

A/D Converter Characteristics (at VDD=5V)

Parameter	Symbol	Condition		Limit min	Limit typ	Limit max	Unit
A/D Conversion Relative Error		VDD=5V, VSS=0V	ch0 to 7			±3	LSB
A/D Conversion Time				4 8			µs
Analog Input Voltage	VIA			VSS		VDD	V

(Ta= 25°C, VDD=5.0V, VSS=0V)

A/D Converter Characteristics (at VDD=3V)

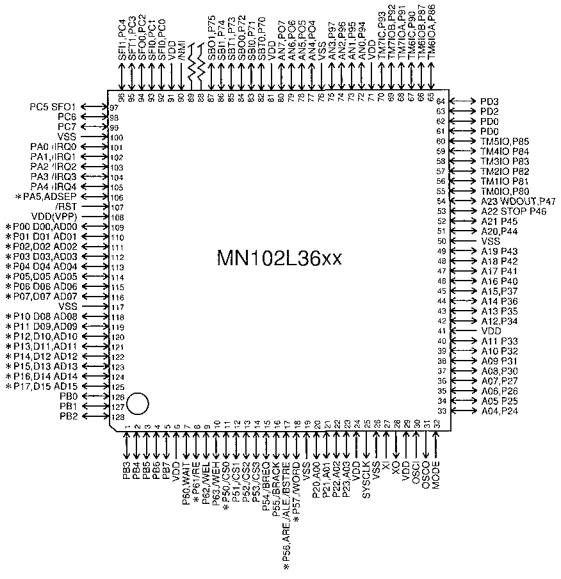
Parameter	Symbol	Condition		Limit min	Limit typ	Limit max	Unit
A/D Conversion Relative Error		VDD=3V, VSS=0V	ch0 to 7			±3	LSB
A/D Conversion Time				9 6			µs
Analog Input Voltage	VIA			VSS		VDD	V

(Ta= 25°C, VDD=3.0V, VSS=0V)

Support Tool

In-Circuit Emulator PX-ICE102L00 + PX-PRB102L36

Pin Assignment



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* Port unusable in MN102L360C