❑ MN102L35G

Type			**MN102L35G (under development)**
ROM (x16-bit)			144K
RAM (x16-bit)			5K
Minimum Instruction Execution Time			**167ns (at 4.75 to 5.25V, 12MHz)**
Interrupts			External (4 lines) Internal (23 lines) Timer x 8, A/D x 1, Undefined command x 1, RESET x 1, OSD x 2, Serial x 2, I^2C x 1, Caption x 2, Remote Control x 1, Address coincidence x 4
Timer Counter			**8-bit timer x 2** **16-bit timer x 2** **Watchdog timer: 17-bit x 1**
Serial Interface			**I^2Cx1** For multimaster mode, Bus line (output) has 2 systems Sync serial / I^2C (master) / UART x 1
Caption			• Built-in sync separator x 2
I/O Pins	**I/O**	**49**	• Common use 49
	Input	**1**	• Common use 1
A/D Inputs			8-bit x 8ch (with S/H)
D/A Inputs			4-bit x 4ch (Analog R, G, B, YM Output)
PWM			8-bit x 6ch
Special Ports			Remote Control Reception (with serial store function)
CRTC			3-layer display (graphics, characters, splits)
Notes			Remote control input discriminant circuit built-in
Package			SDIP064-P-0750

Electrical Characteristics

A/D, D/A Characteristics

Parameter	Symbol	Condition	Limit min	Limit typ	Limit max	Unit
A/D Conversion Absolute Error		AVDD=5V, VSS=0V			±5	LSB
A/D Conversion Time		OSC=at 4MHz	40			µs
A/D Analog Input Voltage	VIA		VSS		VDD	V
D/A Full-scale Output Current	IFS	RL=200Ω VREF=1 2V RIREF=1 2kΩ	45	50	55	mA
D/A Output Voltage Setting Range	VO	RL=200Ω VREF=1 2V RIREF=1 2kΩ	0		11	V
D/A Non-linear Error	NLE	RL=200Ω VREF=1 2V RIREF=1 2kΩ			±0 5	LSB
D/A Differential Non-linear Error	DNLE	RL=200Ω VREF=1 2V RIREF=1 2kΩ			±0 5	LSB
D/A Channel Interval Error	IFS	VREF=1 2V RIREF=1 2kΩ Error from 4-channel average IFS			±5	%

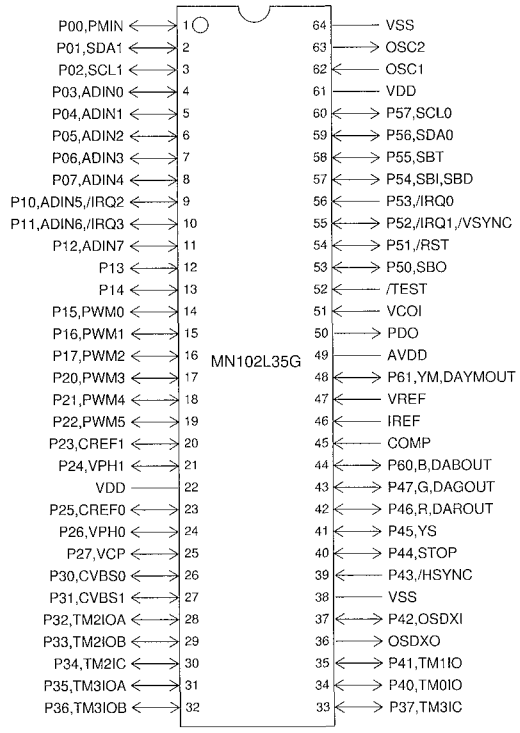
(Ta=25°C, VDD=AVDD=5.0V, VSS=0V, fosc=4MHz)

Support Tool

In-Circuit Emulator

PX-ICE102L00 + PX-PRB102L35

Pin Assignment



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