❑ MN102L2403

Type	**MN102L2403 [ES (Engineering Sample) available]**
ROM (x8-bit / x16-bit)	Maximum 16M in total (Special Register 1K included)
RAM (x8-bit / x16-bit)	External ROM, RAM 3K
Minimum Instruction Execution Time	**100ns (at 4.5 to 5.5V, 20MHz)**
Interrupts	• RESET • Watchdog • Timer Counter 0 to 7 • Timer Counter 8 to 10 • Timer Counter 8 to 10 Compare Capture A • Timer Counter 8 to 10 Compare Capture B • DMA 0 to 5 Transfer finish • External 0 to 7 • Serial ch 0 to 2, 1 Transmission • Serial ch 0 to 2 Reception • $\overline{KI}$ Pin (OR) • A/D Conversion finish • NMI Pin • Address coincidence

Timer Counter

Timer Counter 0 : 8-bit x 1 (Timer Output, Event Count)
- Clock Source . . 1/(1 to 256) of System Clock, External Clock
- Interrupt Source ... . Underflow of Timer Counter 0

Timer Counter 1 : 8-bit x 1 (Timer Output, Event Count, DMA Start up)
- Clock Source 1/(1 to 256) of System Clock, External Clock
- Interrupt Source . . Underflow of Timer Counter 1

Timer Counter 2 : 8-bit x 1 (Timer Output, Event Count, Synchronous Output (4-bit x 2ch))
- Clock Source 1/(1 to 256) of System Clock, External Clock, 1/4 of Low Speed Clock
- Interrupt Source Underflow of Timer Counter 2 4

Timer Counter 3 : 8-bit x 1 (Timer Output, Event Count, A/D Conversion Start up)
- Clock Source 1/(1 to 256) of System Clock, External Clock, 1/4 of Low Speed Clock
- Interrupt Source Underflow of Timer Counter 3

Timer Counter 4 : 8-bit x 1 (Time Output, Event Count, DMA start up)
- Clock Source 1/(1 to 256) of System Clock, External Clock
- Interrupt Source Underflow of Timer Counter 4

Timer Counter 5 to 7 : 8-bit x 1 (Timer Output, Event Count, UART Baud Rate Generator, Synchronous Serial Clock Generator)
- Clock Source . 1/(1 to 256) of System Clock, External Clock
- Interrupt Source Underflow of Timer Counter 5 to 7

Timer Counter 8, 9 : 16-bit x 1 (Timer Output, Event Count, Input Capture, Output Compare, PWM Output, 2-Phase Encoder Input)
- Clock Source . 1/(1 to 256) of System Clock, External Clock
- Interrupt Source . Coincidence with Compare Capture A or at Capture, Coincidence with Compare Capture B or at Capture, Underflow of Timer Counter 8, 9

Timer Counter 10 : 16-bit x 1 (Timer Output, Event Count, Input Capture, Output Compare, PWM Output, Synchronous Output (4-bit x 2ch))
- Clock Source 1/(1 to 256) of System Clock, External Clock
- Interrupt Source .. Coincidence with Compare Capture A or at Capture, Coincidence with Compare Capture B or at Capture

(Connectable) Timer Counter 0 to 7

Serial Interface

Serial 0 : 7,8-bit x 1 (Common use with UART, Transfer direction of MSB/LSB selectable)
- Clock Source 1/2 Timer Counter 5, 1/16 of Timer Counter 5, External Clock, Automatic Baud Rate

Serial 1 : 7,8-bit x 1 (Common use with UART, Transfer direction of MSB/LSB selectable)
- Clock Source . 1/2 Timer Counter 6, 1/16 of Timer Counter 6, 7, External Clock

Serial 2 : 7,8-bit x 1 (Common use with UART, Transfer direction of MSB/LSB selectable)
- Clock Source . . 1/2 of Timer Counter 7, 1/16 of Timer Counter 5, 7, External Clock

UART x 3 (Common use with Serial 0, 1, 2)

I^2C x 3 (Single master)

I/O Pins	**I/O**	**39**	• Common use : 39 (by -bit)
	Input	**13**	• Common use 13 (by-bit)
	Output	**14**	• Common use . 6 (by-bit), 8 (by 4-bit)
A/D Inputs			10-bit x 8ch (with S/H)
PWM			16-bit x 3ch
Notes			Burst ROM Interface, DMA Controller, DRAM Reflesh Controller, DRAM High Speed Page Mode, EDO Mode Support
Package			LQFP128-P-1818B

Electrical Characteristics

A/D Characteristics

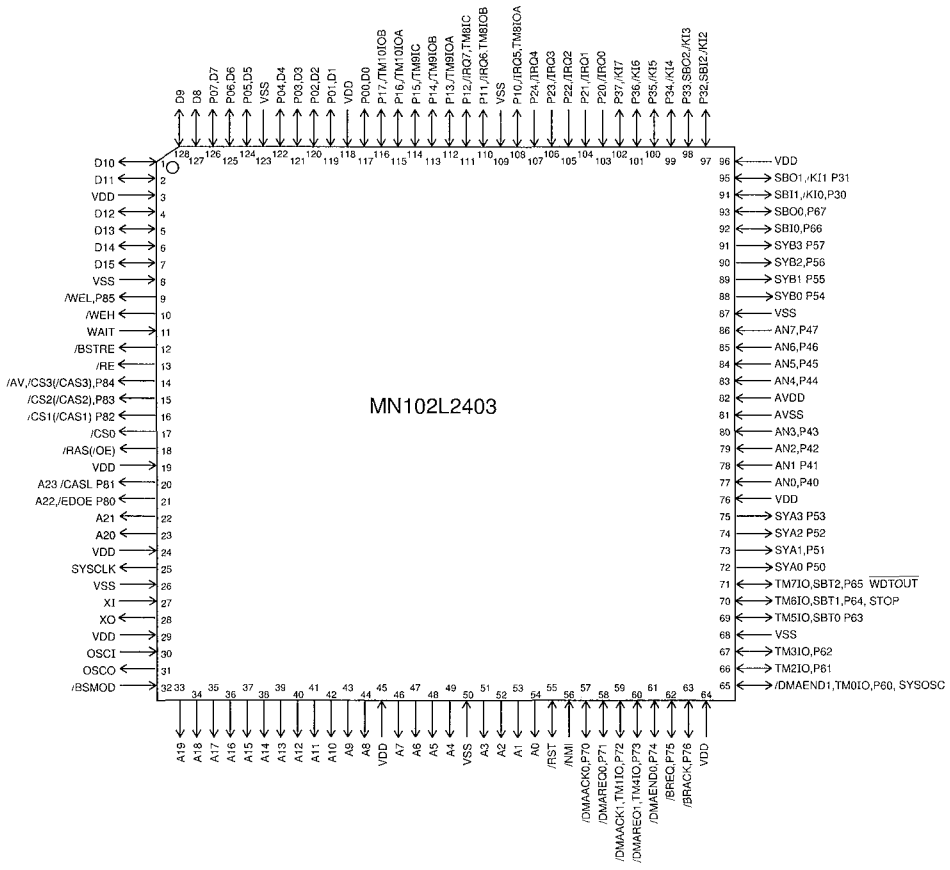
Parameter	Symbol	Condition	Limit min	Limit typ	Limit max	Unit
A/D Conversion Absolute Error		AVDD=5V, AVSS=0V			±4	LSB
A/D Conversion Time			5 6			µs
Analog Input Voltage	VIA		VSS		VDD	V

(Ta=25°C, VDD=5.0V, VSS=0V)

Support Tool

In-Circuit Emulator	PX-ICE102L00 + PX-PRB102L24

Pin Assignment



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