

MN102H460B

Type	MN102H460B [ES (Engineering Sample) available]	
ROM (x8-bit)	External	
RAM (x8-bit)	4K	
Minimum Instruction Execution Time	With Main Clock operated	50ns (at 3.0 to 3.6V, 40MHz) 100ns (at 2.0 to 3.6V, 20MHz)
Interrupts	• $\overline{\text{RST}}$ Pin • Watchdog • NMI Pin • Timer Counter 4 to 15 • Timer Counter 16, 17, 21 • Timer Counter 16 to 20 Compare Capture A • Timer Counter 16 to 20 Compare Capture B • Timer Counter 21 Capture A • Timer Counter 21 Capture B • Timer Counter 21 Capture D • Timer Counter 21 Compare E • Timer Counter 21 Compare F • ATC ch0 to 3 Transfer finish • External 0 to 7 • Serial ch0 to 3 Transmission • Serial ch0 to 3 Reception • $\overline{\text{KT}}$ Pin (OR) • A/D Conversion finish	
Timer Counter	Timer Counter 0 : 8-bit x 1 (Prescalers) Clock Source 1/2 of System Clock, Timer Counter 1 Output Timer Counter 1 : 8-bit x 1 (Prescalers) Clock Source 1/2 of System Clock, Timer Counter 0 Output Timer Counter 2, 3 : 8-bit x 1 (UART Baud Rate Generator) Clock Source 1/2 of System Clock, External Clock Input, Timer Counter 0 Output Timer Counter 4 : 8-bit x 1 (Timer Output, A/D Conversion Start up) Clock Source 1/2 of System Clock, External Clock Input, Timer Counter 0 Output, Timer Counter 1 Output Interrupt Source Underflow of Timer Counter 4 Timer Counter 5, 9 : 8-bit x 1 (UART Baud Rate Generator) Clock Source 1/2 of System Clock, Timer Counter 0 Output, Timer Counter 1 Output Interrupt Source Underflow of Timer Counter 5, 9 Timer Counter 6, 10, 11 : 8-bit x 1 (Timer Output) Clock Source 1/2 of System Clock, External Clock Input, Timer Counter 0 Output Interrupt Source Underflow of Timer Counter 6, 10, 11 Timer Counter 7 : 8-bit x 1 (Timer Output) Clock Source 1/2 of System Clock, External Clock Input, Timer Counter 0 Output Interrupt Source Underflow of Timer Counter 7 Timer Counter 8 : 8-bit x 1 (Timer Output) Clock Source 1/2 of System Clock, External Clock Input, Timer Counter 0 Output, Timer Counter 1 Output Interrupt Source Underflow of Timer Counter 8 Timer Counter 12 : 8-bit x 1 (Timer Output) Clock Source 1/2 of System Clock, External Clock Input with Edge, Timer Counter 0 Output, Timer Counter 1 Output Interrupt Source Underflow of Timer Counter 12 Timer Counter 13 : 8-bit x 1 (Timer Output) Clock Source 1/2 of System Clock, Timer Counter 0 Output, Timer Counter 1 Output Interrupt Source Underflow of Timer Counter 13 Timer Counter 14 : 8-bit x 1 (Timer Output) Clock Source 1/2 of System Clock, External Clock Input with Edge, Timer Counter 0 Output Interrupt Source Underflow of Timer Counter 14	

Timer Counter (Continue)**Timer Counter 15 : 8-bit x 1** (Timer Output)

Clock Source	. 1/2 of System Clock, External Clock Input with Edge, Timer Counter 0 Output
Interrupt Source	. Underflow of Timer Counter 15

Connectable

Timer Counter 0 to 3, 4 to 7, 8 to 11, 12 to 15

Timer Counter 16, 17 : 16-bit x 1 (Timer Output, Event Count, Input Capture, Output Compare PWM Output, 2-Phase Encoder Input)

Clock Source	. 1/2 of System Clock, External Clock Input (with Edge, Timer Counter 17 only), Timer Counter 0 Output, Timer Counter 1 Output (Timer Counter 16 only)
Interrupt Source	Coincidence with Compare Capture A or at Capture Coincidence with Compare Capture B or at Capture Underflow of Timer Counter 16, 17

Timer Counter 18, 19, 20: 16-bit x 1 (Timer Output, Event Count, Input Capture, Output Compare PWM Output, 2-Phase Encoder Input)

Clock Source	. 1/2 of System Clock, External Clock Input, Timer Counter 0 Output, Timer Counter 1 Output
Interrupt Source	Coincidence with Compare Capture A or at Capture Coincidence with Compare Capture B or at Capture Underflow of Timer Counter 18, 19, 20

Timer Counter 21 : 24-bit x 1 (Servo Control)

Clock Source	1/2 of System Clock, Timer Counter 1 Output
Interrupt Source	When capturing to Capture A When capturing to Capture B When capturing to Capture D When coinciding to Compare E When coinciding to Compare F

Serial Interface**Serial 0, 1 : 8-bit x 1** (Transfer direction of MSB / LSB selectable, Transmission / Reception of 7, 8-bit length)

Clock Source	. 1/8 of Timer Counter 2, 1/8, 1/2 of Timer Counter 5, External Clock
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Serial 2, 3 : 8-bit x 1 (Transfer direction of MSB / LSB selectable, Transmission / Reception of 7, 8-bit length)

Clock Source	. 1/8 of Timer Counter 3, 1/8, 1/2 of Timer Counter 9, External Clock
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UART x 4 (Common use with Serial 0 to 3)**I²C x 2** (Common use with Serial 1, 3, Single Master)

I/O Pins	I/O	100	• Common use : 56 (Address Data Separate 8-bit Mode) • Common use : 73 (Address Data Multiplex 8-bit Mode)
	Input	8	• Common use : 8

See the next page for support tool, peripheral function, Pin Assignment and electrical characteristics.

A/D Inputs	10-bit x 12ch (Maximum input is 16) (with S/H)
PWM	16-bit x 5ch (Timer Counter 16 to 20)
ICR	16-bit x 5ch, 24-bit x 1ch (Timer Counter 16 to 21)
OCR	16-bit x 5ch, 24-bit x 1ch (Timer Counter 16 to 21)
Notes	Address / Data Multiplex Bus Interface, Address / Data Separate Bus Interface, 8-bit / 16-bit Bus Width selectable, DRAM Refresh Controller built-in
Package	LQFP128-P-1818B

Electrical Characteristics

A/D Characteristics

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Non-linear Error		10-bit			±4	LSB
A/D Conversion Time		at 40MHz	2.8			µs
Analog Input Voltage	VIA		VSS		VDD	V

(Ta= 25°C, VDD=AVDD=3.3V, VSS=AVSS=0V)

Supply Current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating Supply Current	IDDopr	VI = VDD or VSS, Output release f = 40MHz, VDD=3.3V			50	mA
Supply Current at STOP	IDDS	Pin with pull-up resistor is open All other input pins and Hi-z state input/output pins are simultaneously applied VDD or VSS level			150	µA
Supply Current at HALT	IDDH	f = 40MHz, VDD = 3.3V Output release			25	mA

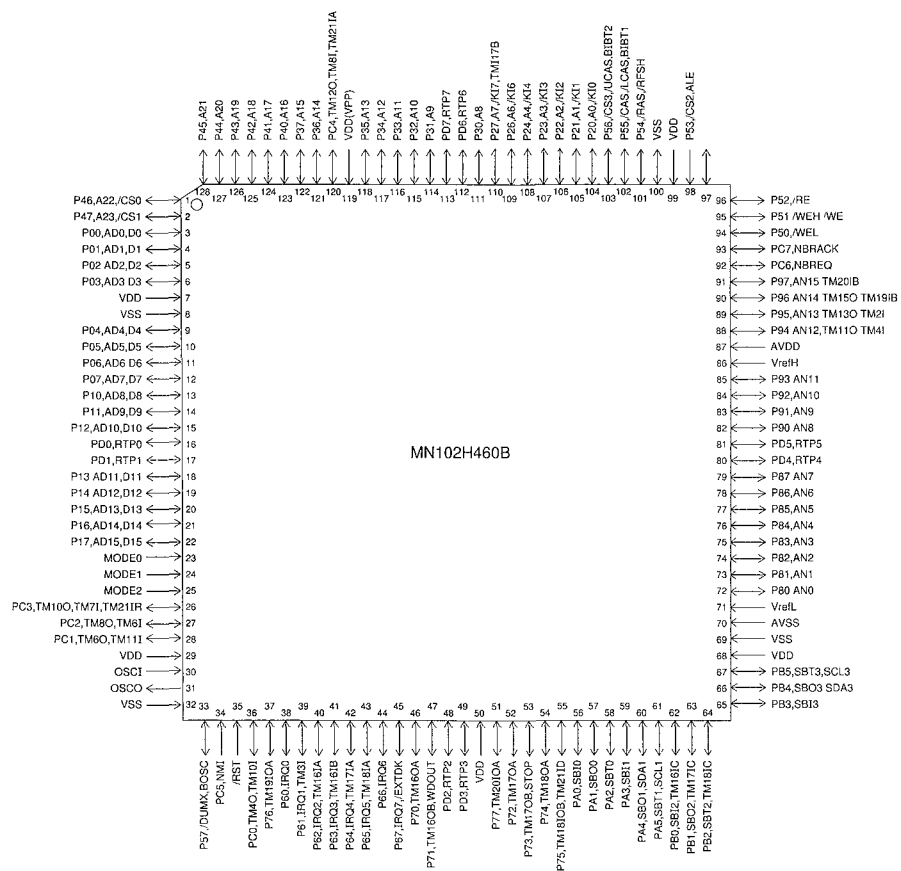
(Ta= -20 to +70°C, VDD=AVDD=3.3V, VSS=AVSS=0V)

Support Tool

In Circuit Emulator

PX-ICE102H460B

Pin Assignment



LQFP128-P-1818B