MJW16206

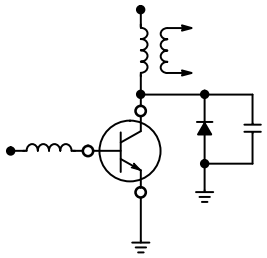
SCANSWITCH™

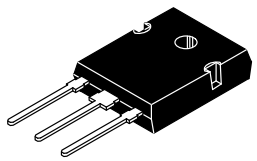
NPN Bipolar Power Deflection Transistors For High and Very High Resolution CRT Monitors

POWER TRANSISTORS
12 AMPERES
1200 VOLTS — V_{CES}
50 and 150 WATTS

The MJF16206 and the MJW16206 are state–of–the–art SWITCHMODE bipolar power transistors. They are specifically designed for use in horizontal deflection circuits for high and very high resolution, monochrome and color CRT monitors.

- **1200 Volt V_{CES} Breakdown Capability**
- Typical Dynamic Desaturation Specified (New Turn–Off Characteristic)
- Maximum Repetitive Emitter–Base Avalanche Energy Specified (Industry First)
- High Current Capability: Performance Specified at 6.5 Amps
  Continuous Rating — 12 Amps Max
  Pulsed Rating — 15 Amps Max
- Isolated MJF16206 is UL Recognized
- Fast Switching: 100 ns Inductive Fall Time (Typ)
  1000 ns Inductive Storage Time (Typ)
- Low Saturation Voltage
  0.25 Volts (Typ) at 6.5 Amps Collector Current
- High Emitter–Base Breakdown Capability For High Voltage Off Drive Circuits — 8.0 V (Min)





CASE 340F–02
TO–247AE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Breakdown Voltage	**V_{CES}**	**1200**	Vdc
Collector–Emitter Sustaining Voltage	$V_{CEO(sus)}$	500	Vdc
Emitter–Base Voltage	V_{EBO}	8.0	Vdc
Isolation Voltage (RMS for 1 sec., T_A = 25°C, Figure 19 Relative Humidity ≤ 30%) Figure 20	V_{ISOL}	— —	V_{rms}
Collector Current — Continuous — Pulsed (1)	I_C I_{CM}	12 15	Adc
Base Current — Continuous — Pulsed (1)	I_B I_{BM}	5.0 10	Adc
Repetitive Emitter–Base Avalanche Energy	$W_{(BER)}$	0.2	mjoules
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derated above 25°C	P_D	150 39 1.49	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	0.67	°C/W
Lead Temperature for Soldering Purposes 1/8″ from the Case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

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REV 2

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector Cutoff Current (V_{CE} = 1200 Vdc, V_{BE} = 0 V) (V_{CE} = 850 Vdc, V_{BE} = 0 V)	I_{CES}	 — —	 — —	 250 25	μAdc
Emitter–Base Leakage (V_{EB} = 8.0 Vdc, I_C = 0)	I_{EBO}	—	—	25	μAdc
Collector–Emitter Sustaining Voltage (Figure 10) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	500	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 1.0 mA, I_C = 0)	$V_{(BR)EBO}$	8.0	11	—	Vdc
ON CHARACTERISTICS (1)					
Collector–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 400 mAdc) (I_C = 6.5 Adc, I_B = 1.5 Adc)	$V_{CE(sat)}$	 — —	 0.15 0.25	 1.0 1.0	Vdc
Base–Emitter Saturation Voltage (I_C = 6.5 Adc, I_B = 1.5 Adc)	$V_{BE(sat)}$	—	0.9	1.5	Vdc
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 10 Adc, V_{CE} = 5.0 Vdc) (I_C = 12 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	 — 5.0 3.0	 24 8.0 6.0	 — 13 —	—
DYNAMIC CHARACTERISTICS					
Dynamic Desaturation Interval (Figure 15) (I_C = 6.5 Adc, I_B = 1.5 Adc, L_B = 0.5 μH)	t_{ds}	—	250	—	ns
Emitter–Base Avalanche Turn–off Energy (Figure 15) (t = 500 ns, R_{BE} = 22 Ω)	$EB_{(off)}$	—	30	—	μjoules
Output Capacitance (V_{CE} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	—	180	350	pF
Gain Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.5 A, f_{test} = 1.0 MHz)	f_T	—	3.0	—	MHz
Collector–Heatsink Capacitance — MJF16206 Isolated Package (Mounted on a 1″ x 2″ x 1/16″ Copper Heatsink, V_{CE} = 0, f_{test} = 100 kHz)	$C_{c–hs}$	—	17	—	pF
SWITCHING CHARACTERISTICS					
Inductive Load (Figure 15) (I_C = 6.5 A, I_B = 1.5 A) Storage Fall Time	 t_{sv} t_{fi}	 — —	 1000 100	 2250 250	ns

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

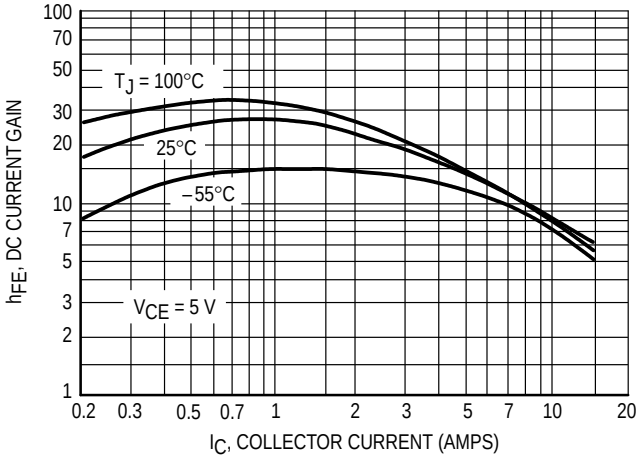


Figure 1. Typical DC Current Gain

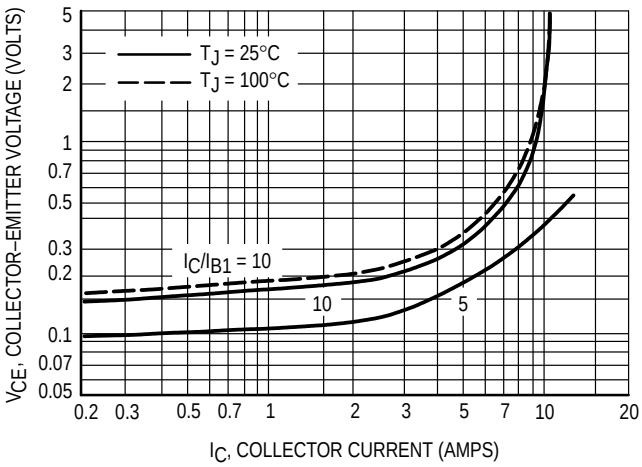


Figure 2. Typical Collector–Emitter Saturation Voltage

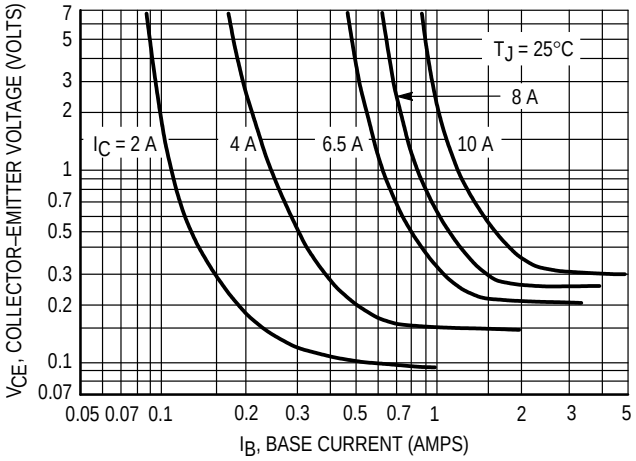


Figure 3. Typical Collector Saturation Region

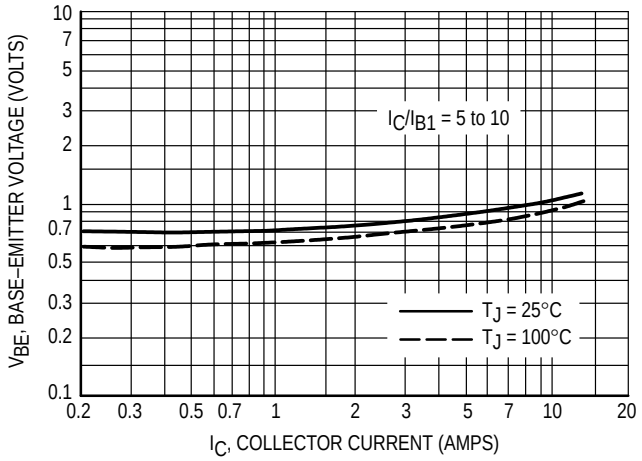


Figure 4. Typical Base–Emitter Saturation Voltage

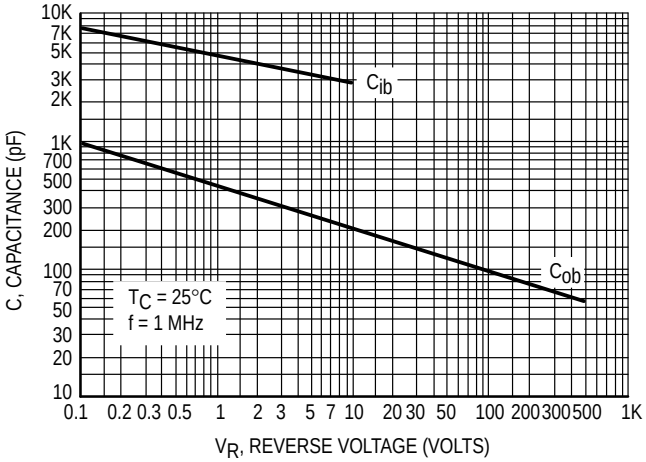


Figure 5. Typical Capacitance

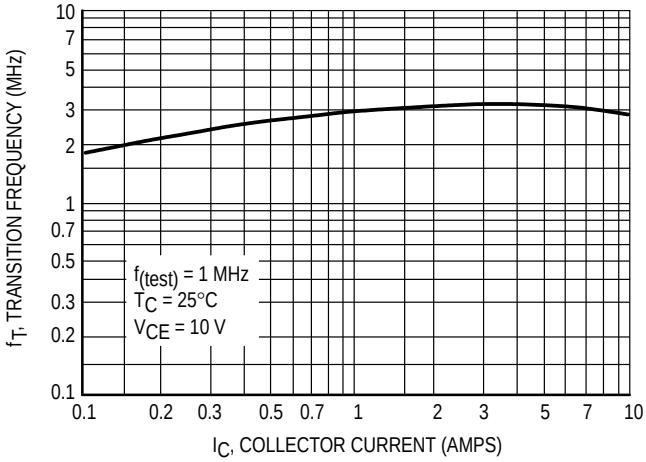
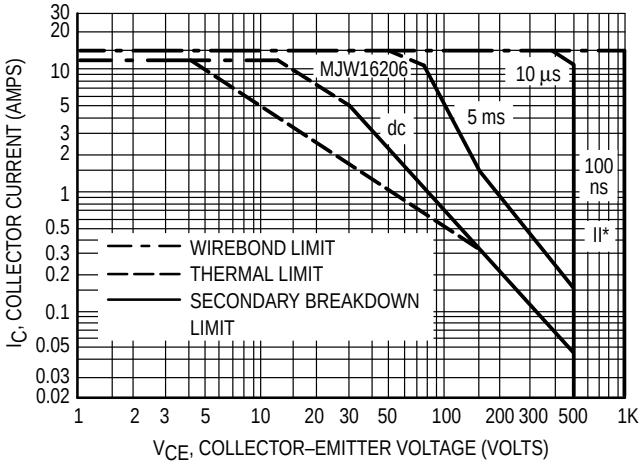


Figure 6. Typical Transition Frequency

SAFE OPERATING AREA INFORMATION



*REGION II — EXPANDED FBSOA USING MUR8100E, ULTRAFAST RECTIFIER (SEE FIGURE 12)

Figure 7. Maximum Forward Biased Safe Operating Area

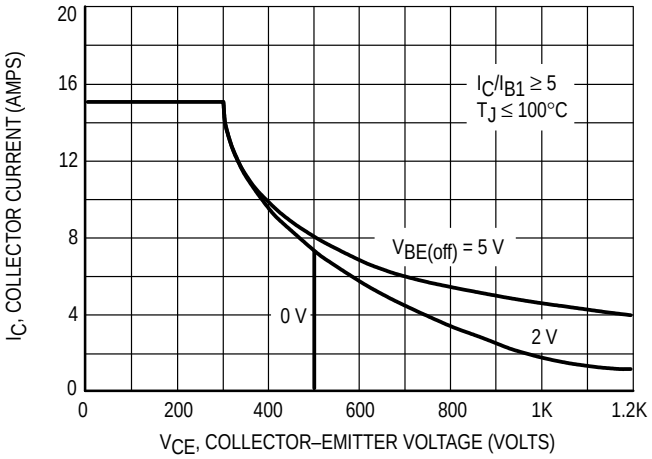


Figure 8. Maximum Reverse Bias Safe Operating Area

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

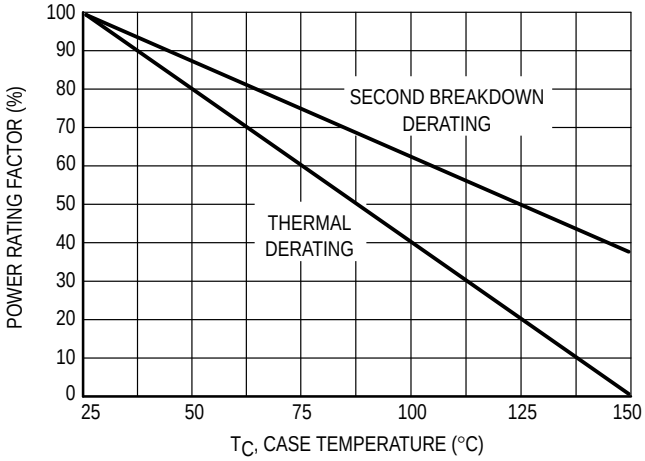


Figure 9. Power Derating

REVERSE BIAS

Inductive loads, in most cases, require the emitter–to–base junction be reversed biased because high voltage and high current must be sustained simultaneously during turn–off. Under these conditions, the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage–current condition allowable during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 8 gives the RBSOA characteristics.

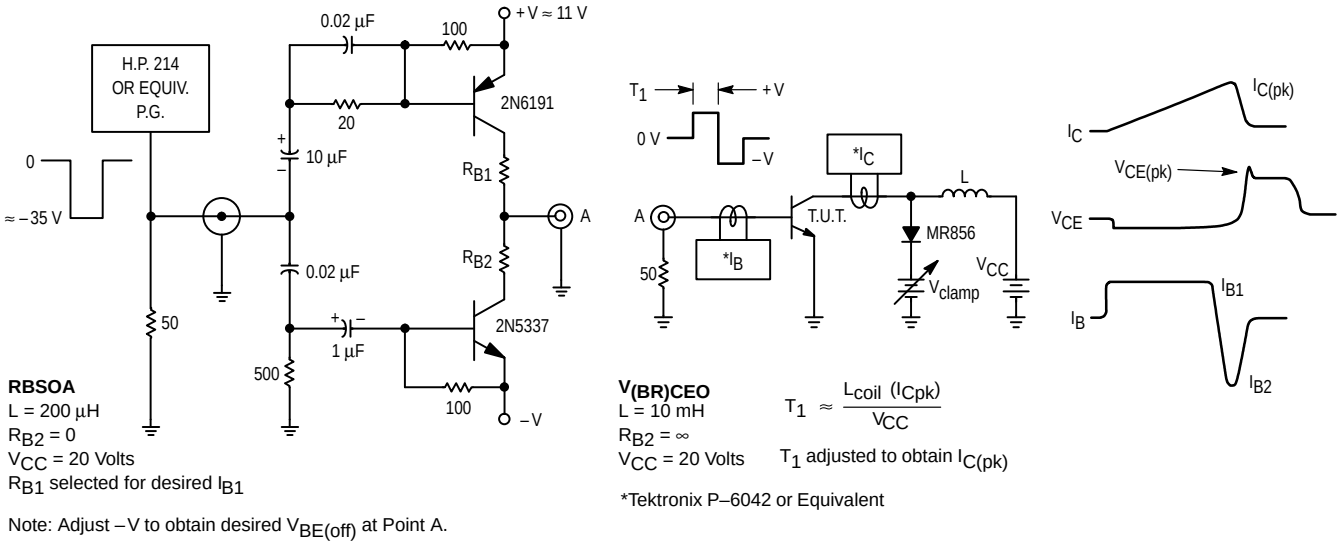


Figure 10. RBSOA/$V_{(BR)CEO(sus)}$ Test Circuit

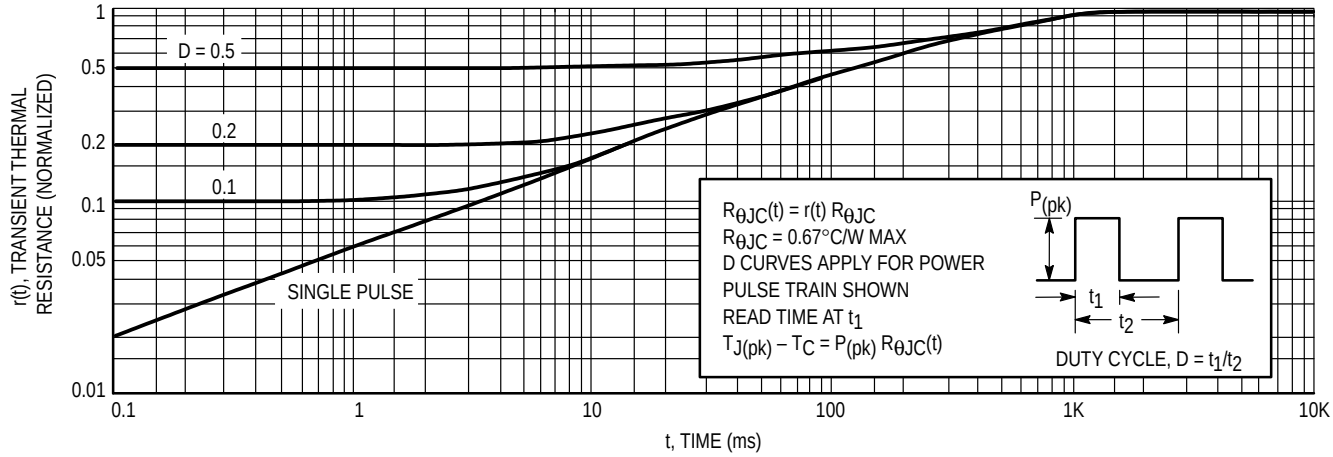
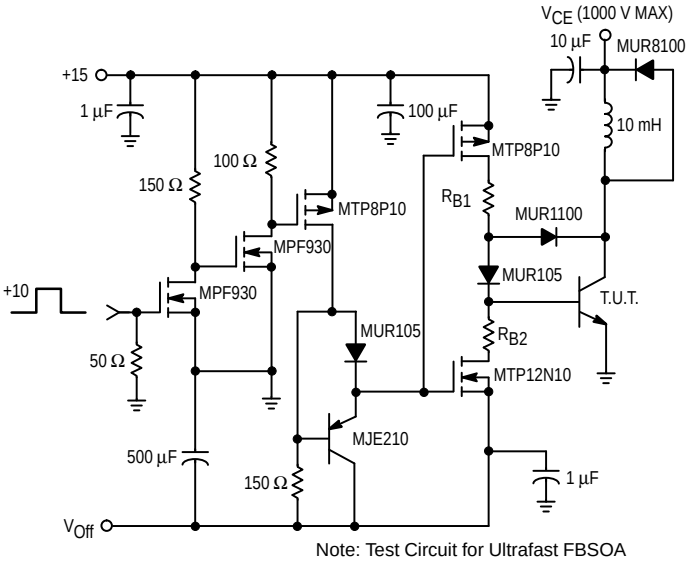


Figure 11. Thermal Response



Note: Test Circuit for Ultrafast FBSOA
R_{B2} = 0 and V_{Off} = –5 Volts

Figure 12. Switching Safe Operating Area

DYNAMIC DESATURATION

The SCANSWITCH series of bipolar power transistors are specifically designed to meet the unique requirements of horizontal deflection circuits in computer monitor applications. Historically, deflection transistor design was focused on minimizing collector current fall time. While fall time is a valid figure of merit, a more important indicator of circuit performance as scan rates are increased is a new characteristic, “dynamic desaturation.” In order to assure a linear collector current ramp, the output transistor must remain in hard saturation during storage time and exhibit a rapid turn–off transition. A sluggish transition results in serious consequences. As the saturation voltage of the output transistor increases, the voltage across the yoke drops. Roll off in the collector current ramp results in improper beam deflection and distortion of the image at the right edge of the screen. Design changes have been made in the structure of the SCANSWITCH series of devices which minimize the dynamic desaturation interval. Dynamic desaturation has been defined in terms of the time required for the V_{CE} to rise from 1.0 to 5.0 volts (Figures 13 and 14) and typical performance at optimized drive conditions has been specified. Optimization of device structure results in a linear collector Current ramp, excellent turn–off switching performance, and significantly lower overall power dissipation.

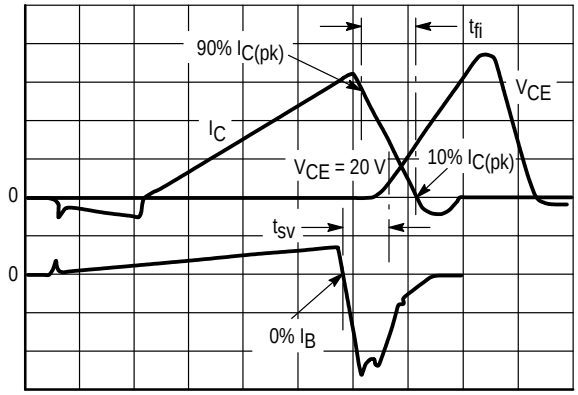


Figure 13. Deflection Simulator Switching Waveforms From Circuit in Figure 15

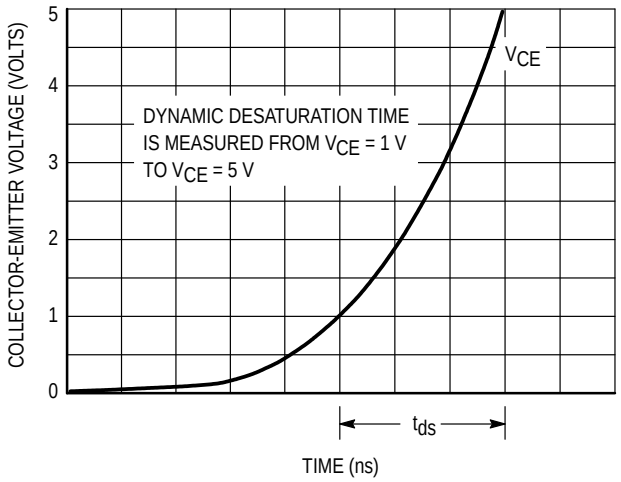


Figure 14. Definition of Dynamic Desaturation Measurement

EMITTER–BASE TURN–OFF ENERGY

Typical techniques for driving horizontal outputs rely on a pulse transformer to supply forward base current, and a turn–off network that includes a series base inductor to limit the rate of transition from forward to reverse drive. An alternate drive scheme has been used to characterize the SCANSWITCH series of devices (see Figure 15). This circuit produces a ramp of base drive, eliminating the heavy overdrive at the beginning of the collector current ramp and underdrive just prior to turnoff produced by typical drive strategies. This high performance drive has two additional important advantages. First, the configuration of T_1 allows L_B to be placed outside the path of forward base current making it unnecessary to expend energy to reverse current flow as in a series base inductor. Second, there is no base resistor to limit forward base current and hence no power loss associated with setting the value of the forward base current. The process of generating the ramp stores rather than dissipates energy. Tailoring the amount of energy stored in T_1 to the amount of energy, $EB_{(off)}$, that is required to turn–off the output transistor results in essentially lossless operation. [Note: B+ and the primary inductance of T_1 (L_P) are chosen such that $1/2\ L_P\ I_b^2 = EB_{(off)}$].

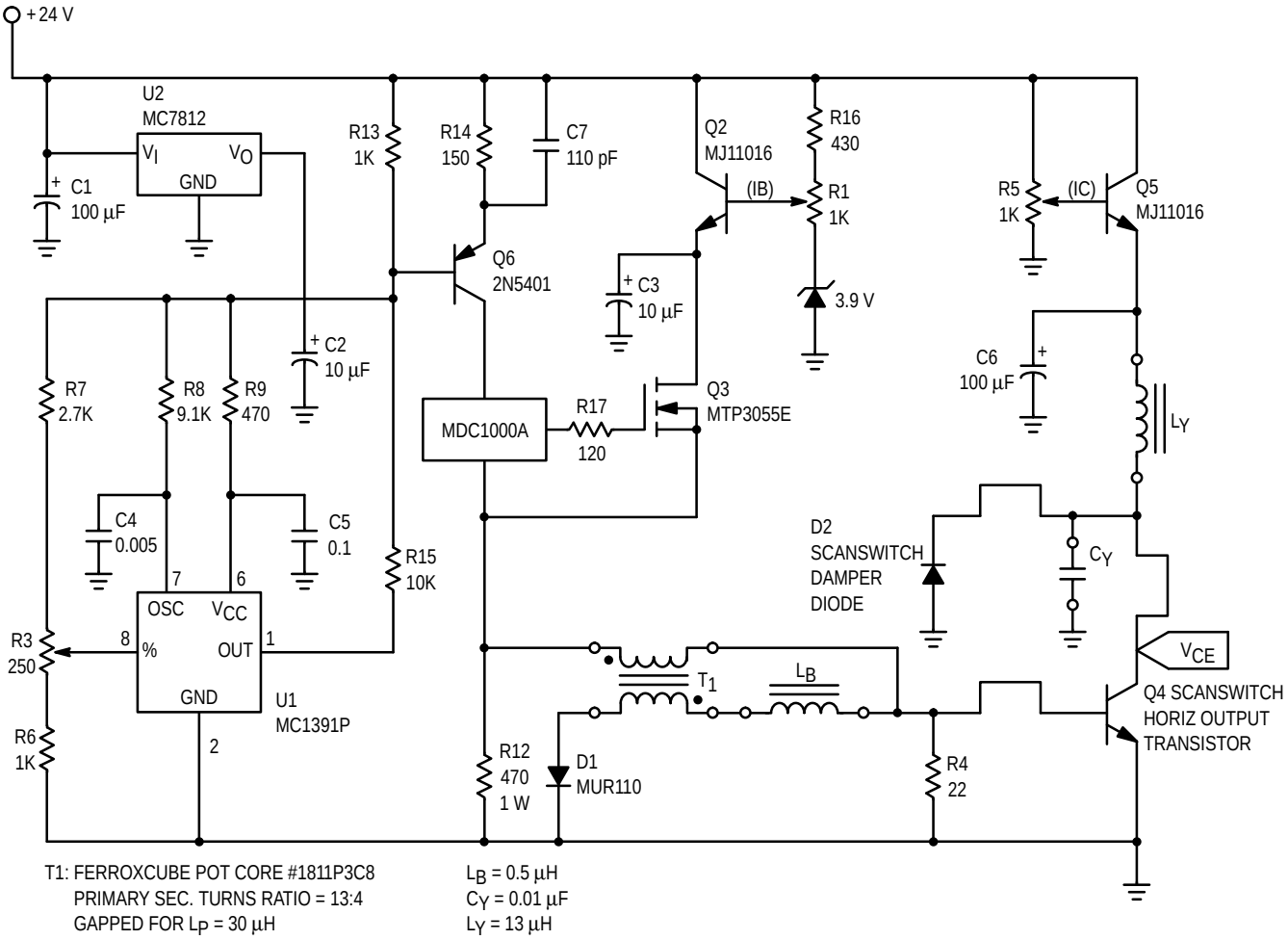
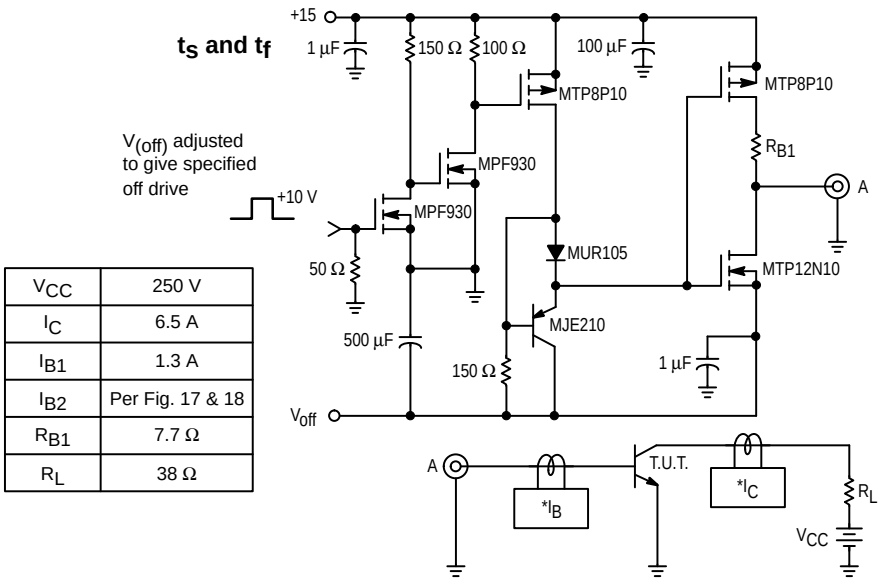


Figure 15. High Resolution Deflection Application Simulator



V_{CC}	250 V
I_C	6.5 A
I_{B1}	1.3 A
I_{B2}	Per Fig. 17 & 18
R_{B1}	7.7 Ω
R_L	38 Ω

Figure 16. Resistive Load Switching

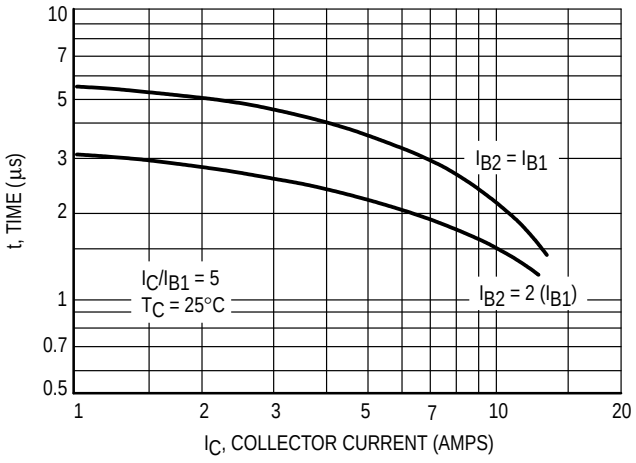


Figure 17. Typical Resistive Storage Time

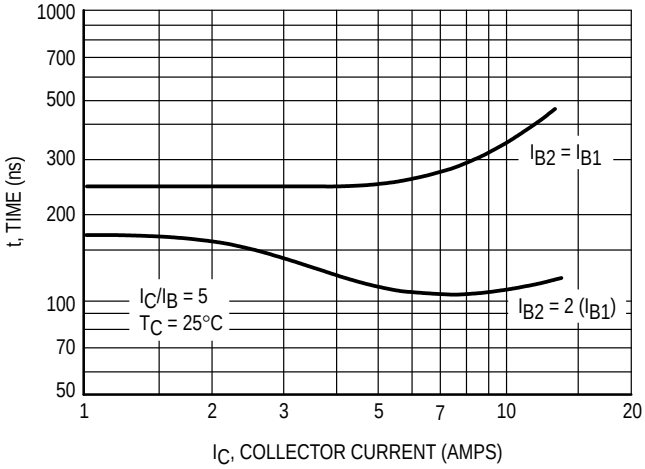


Figure 18. Typical Resistive Fall Time

TEST CONDITIONS FOR ISOLATION TESTS*

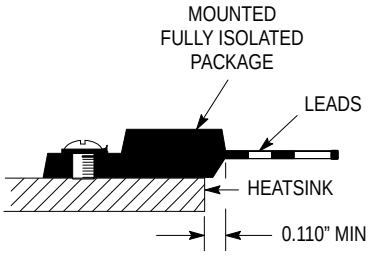


Figure 19. Screw or Clip Mounting Position for Isolation Test Number 1

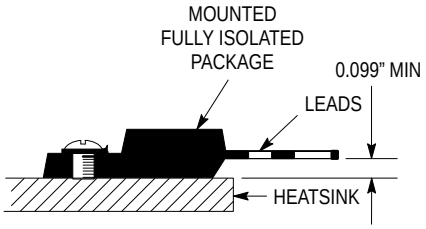
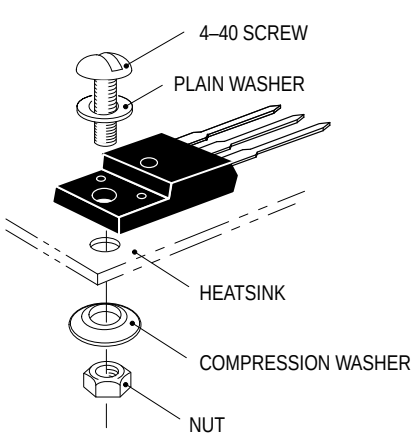


Figure 20. Screw or Clip Mounting Position for Isolation Test Number 2

* Measurement made between leads and heatsink with all leads shorted together.

MOUNTING INFORMATION**



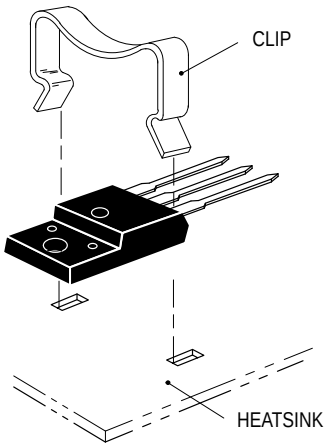


Figure 21. Typical Mounting Techniques*

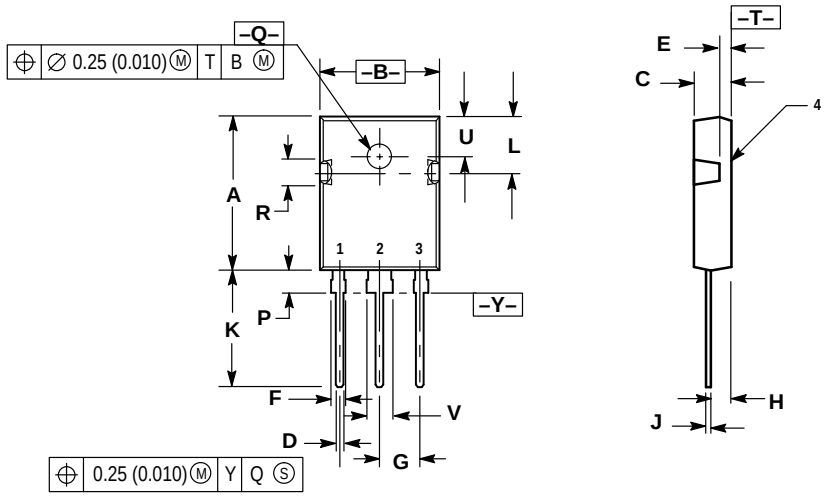
Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4-40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4-40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.40	20.90	0.803	0.823
B	15.44	15.95	0.608	0.628
C	4.70	5.21	0.185	0.205
D	1.09	1.30	0.043	0.051
E	1.50	1.63	0.059	0.064
F	1.80	2.18	0.071	0.086
G	5.45 BSC		0.215 BSC	
H	2.56	2.87	0.101	0.113
J	0.48	0.68	0.019	0.027
K	15.57	16.08	0.613	0.633
L	7.26	7.50	0.286	0.295
P	3.10	3.38	0.122	0.133
Q	3.50	3.70	0.138	0.145
R	3.30	3.80	0.130	0.150
U	5.30 BSC		0.209 BSC	
V	3.05	3.40	0.120	0.134

STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 340F–03
TO–247AE
ISSUE E

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