MJE5850
MJE5851*
MJE5852*

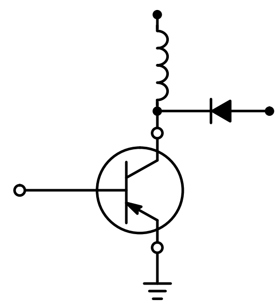
*Motorola Preferred Device

Designer's™ Data Sheet
SWITCHMODE Series
PNP Silicon Power Transistors

8 AMPERE
PNP SILICON
POWER TRANSISTORS
300, 350, 400 VOLTS
80 WATTS

The MJE5850, MJE5851 and the MJE5852 transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



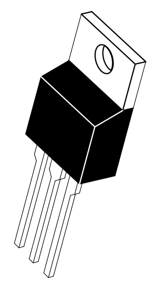
Fast Turn–Off Times

100 ns Inductive Fall Time @ 25°C (Typ)
125 ns Inductive Crossover Time @ 25°C (Typ)

Operating Temperature Range –65 to +150°C

100°C Performance Specified for:

Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	MJE5850	MJE5851	MJE5852	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	300	350	400	Vdc
Collector–Emitter Voltage	V_{CEV}	350	400	450	Vdc
Emitter Base Voltage	V_{EB}		6.0		Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}		8.0 1 6		Adc
Base Current — Continuous Peak (1)	I_B I_{BM}		4.0 8.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D		80 0.640		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		–65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)	MJE5850 MJE5851 MJE5852	$V_{CEO(sus)}$	300 350 400	— —	— —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	— —	— —	0.5 2.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with base reverse biased		RBSOA	See Figure 13			
***ON CHARACTERISTICS**						
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5 Vdc) (I_C = 5.0 Adc, V_{CE} = 5 Vdc)		h_{FE}	15 5	— —	— —	—
Collector–Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 1.0 Adc) (I_C = 8.0 Adc, I_B = 3.0 Adc) (I_C = 4.0 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{CE(sat)}$	— — —	— — —	2.0 5.0 2.5	Vdc
Base–Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 1.0 Adc) (I_C = 4.0 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	—	270	—	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 4.0 A, I_{B1} = 1.0 A, t_p = 50 µs, Duty Cycle ≤ 2%)	t_d	—	0.025	0.1	µs
Rise Time		t_r	—	0.100	0.5	µs
Storage Time	(V_{CC} = 250 Vdc, I_C = 4.0 A, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, t_p = 50 µs, Duty Cycle ≤ 2%)	t_s	—	0.60	2.0	µs
Fall Time		t_f	—	0.11	0.5	µs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_{CM} = 4 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	—	0.8	3.0	µs
Crossover Time		t_c	—	0.4	1.5	µs
Fall Time		t_{fi}	—	0.1	—	µs
Storage Time	(I_{CM} = 4 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	—	0.5	—	µs
Crossover Time		t_c	—	0.125	—	µs
Fall Time		t_{fi}	—	0.1	—	µs

* Pulse Test: PW = 300 µs. Duty Cycle ≤ 2%

TYPICAL ELECTRICAL CHARACTERISTICS

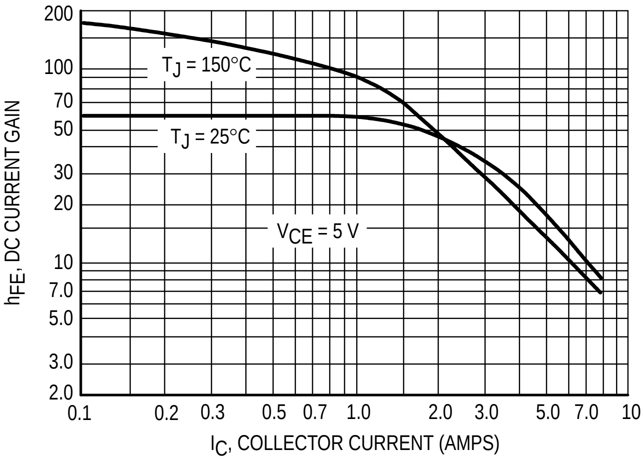


Figure 1. DC Current Gain

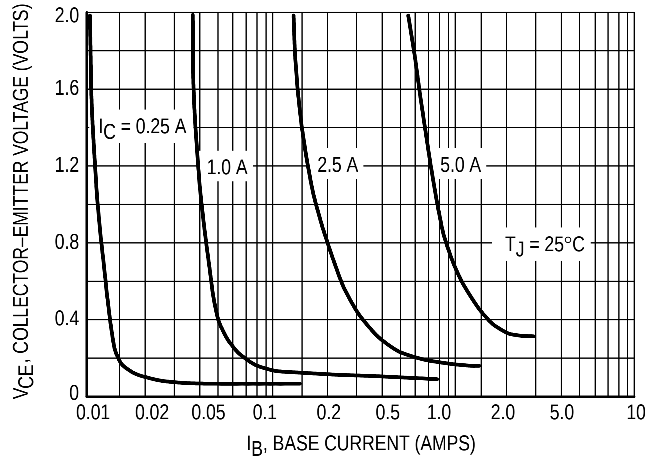


Figure 2. Collector Saturation Region

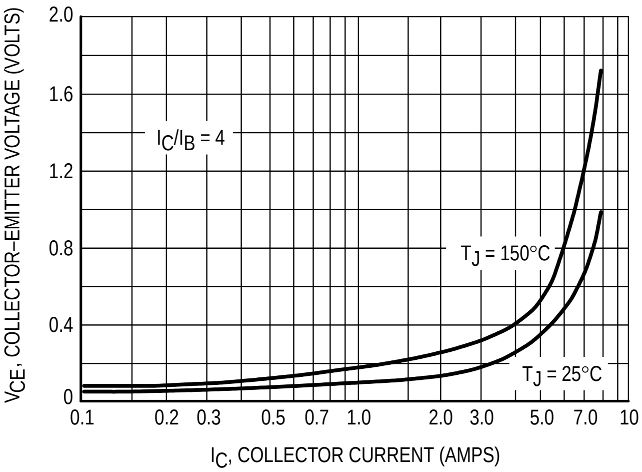


Figure 3. Collector–Emitter Saturation Voltage

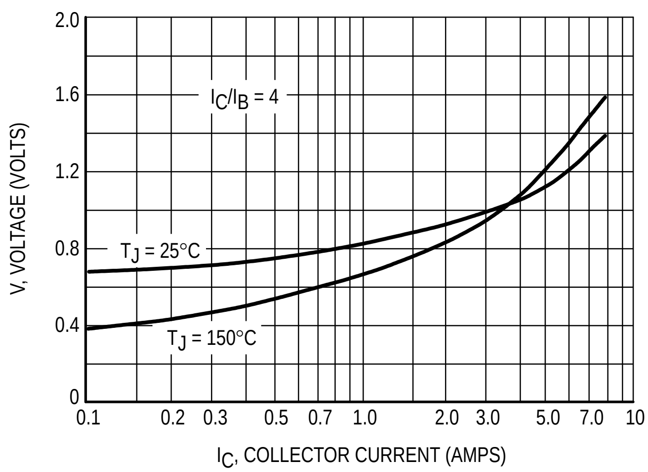


Figure 4. Base–Emitter Voltage

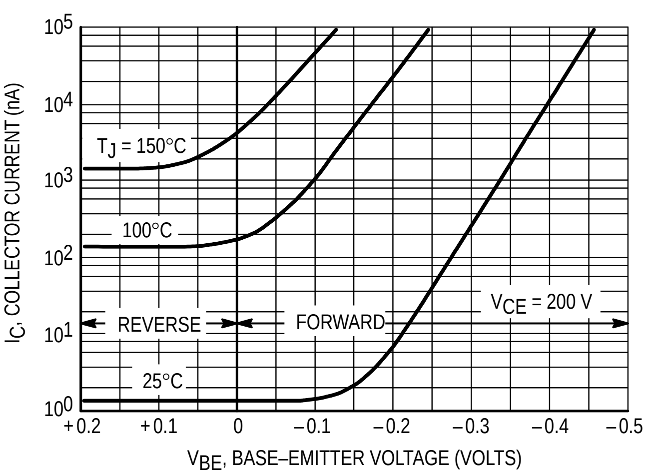


Figure 5. Collector Cutoff Region

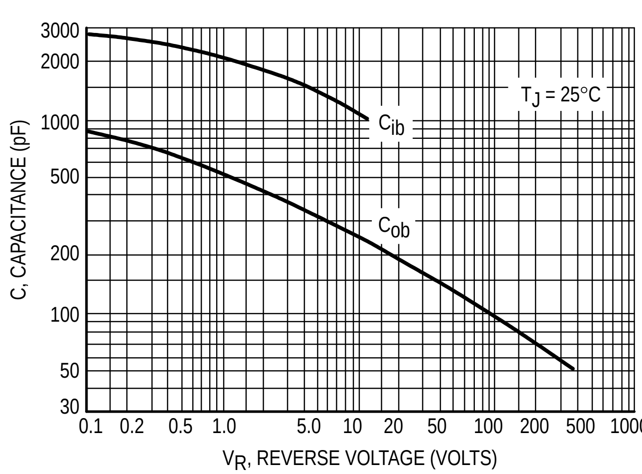
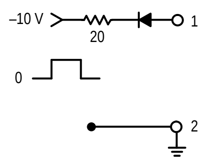
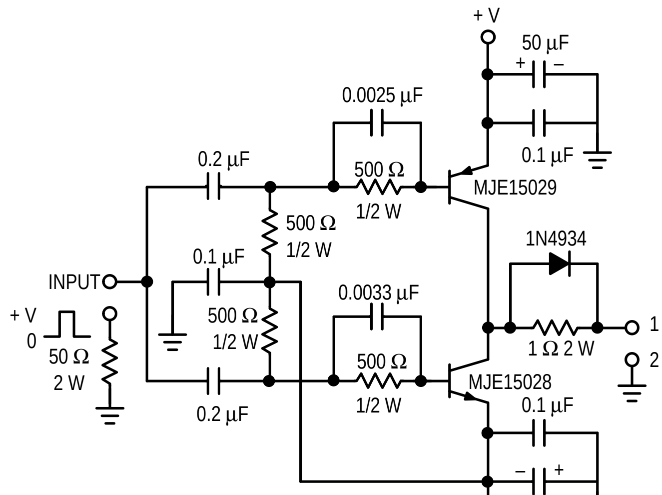
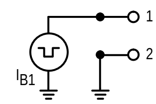
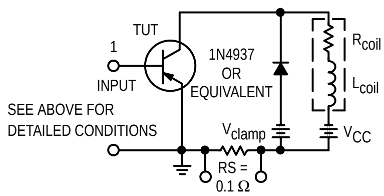
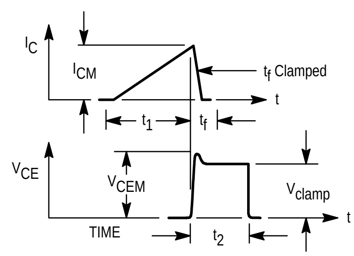
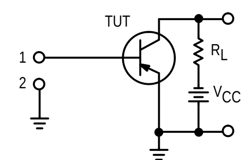


Figure 6. Capacitance

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	 –V adjusted to obtain desired I_{B1} +V adjusted to obtain desired $V_{BE(off)}$	**TURN–ON TIME**  I_{B1} adjusted to obtain the forced h_{FE} desired **TURN–OFF TIME** Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 62 Ω Pulse Width = 10 µs
TEST CIRCUITS	**INDUCTIVE TEST CIRCUIT** 	**OUTPUT WAVEFORMS**  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}\,(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}\,(I_{CM})}{V_{Clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	**RESISTIVE TEST CIRCUIT** 

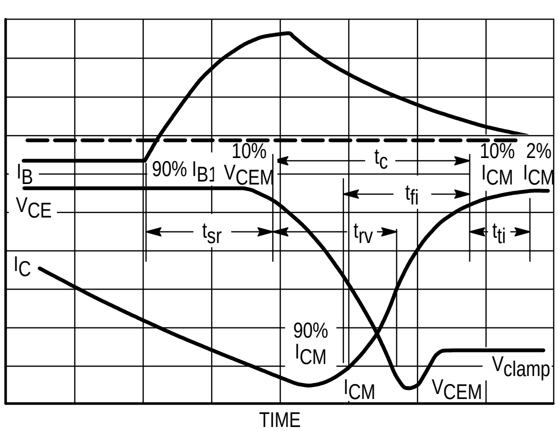


Figure 7. Inductive Switching Measurements

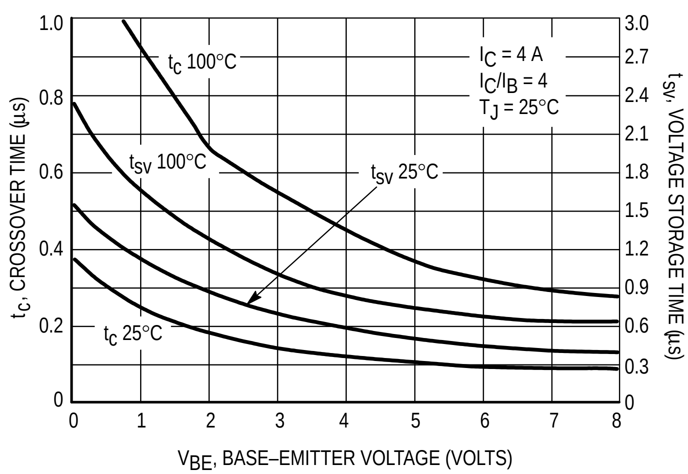


Figure 8. Inductive Switching Times

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
t_{rv} = Voltage Rise Time, 10–90% V_{CEM}
t_{fi} = Current Fall Time, 90–10% I_{CM}
t_{ti} = Current Tail, 10–2% I_{CM}
t_c = Crossover Time,10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222A:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

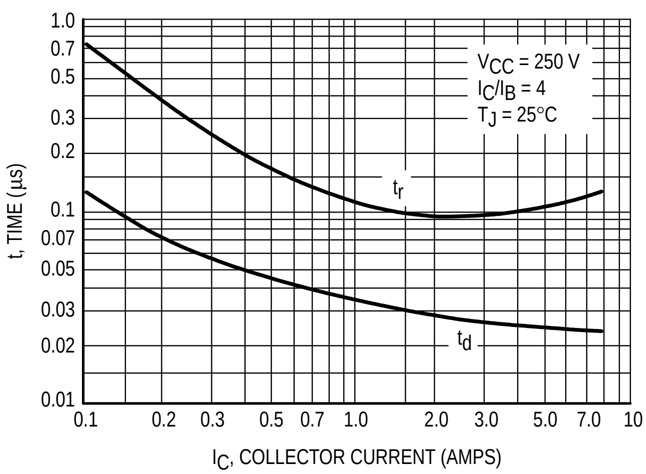


Figure 9. Turn–On Switching Times

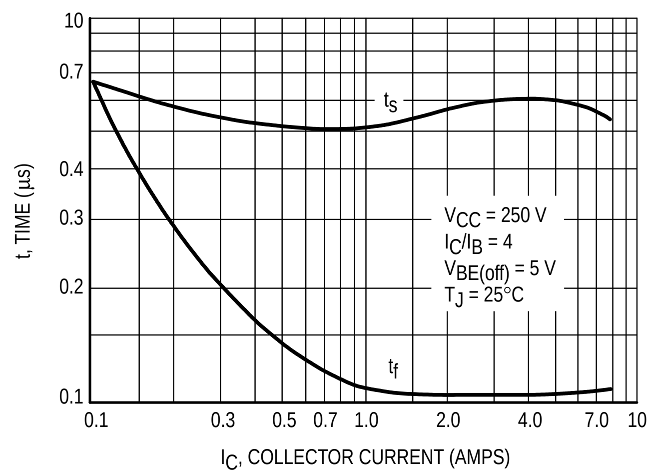


Figure 10. Turn–Off Switching Time

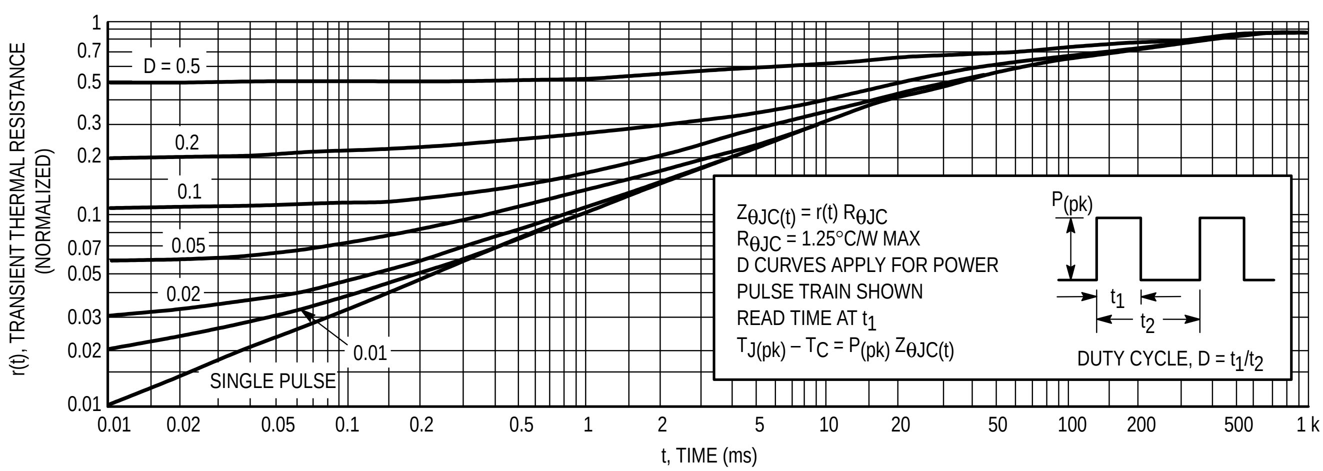


Figure 11. Typical Thermal Response [$Z_{\theta JC}(t)$]

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

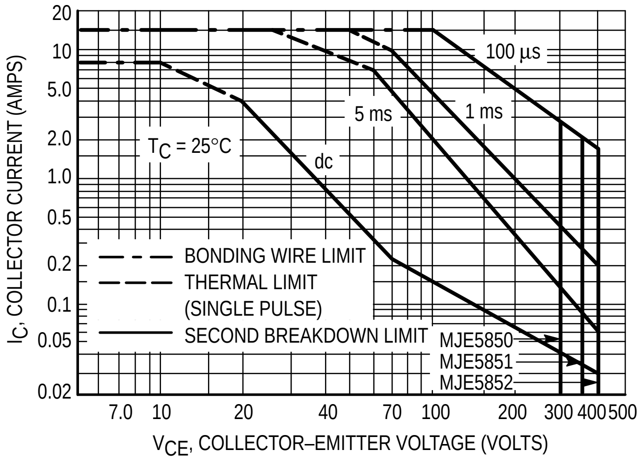


Figure 12. Maximum Forward Bias Safe Operating Area

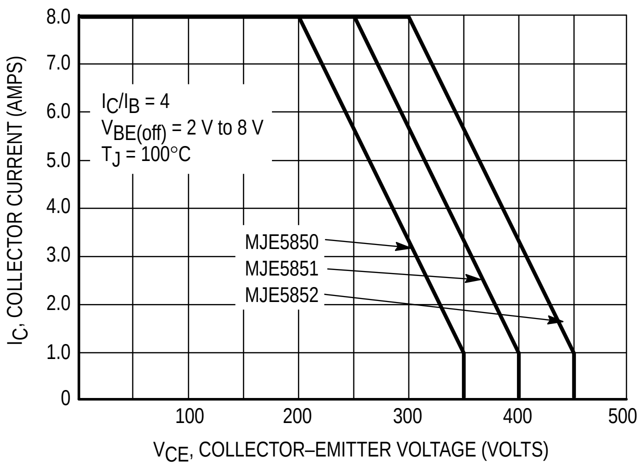


Figure 13. RBSOA, Maximum Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate $I_C – V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current condition allowable during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.

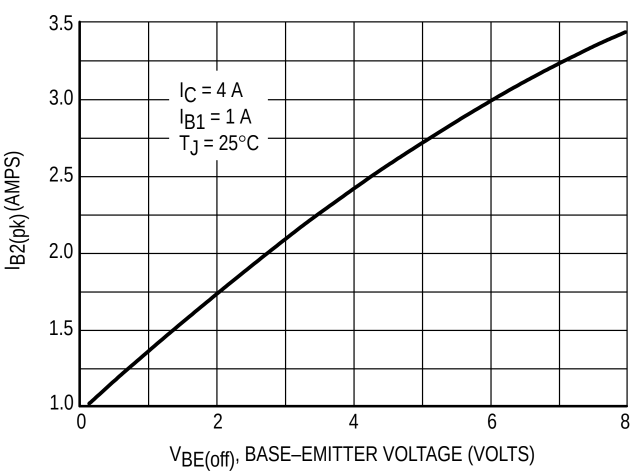


Figure 14. Peak Reverse Base Current

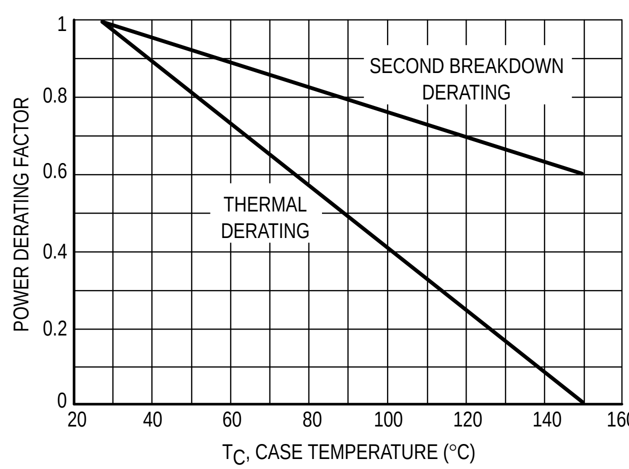
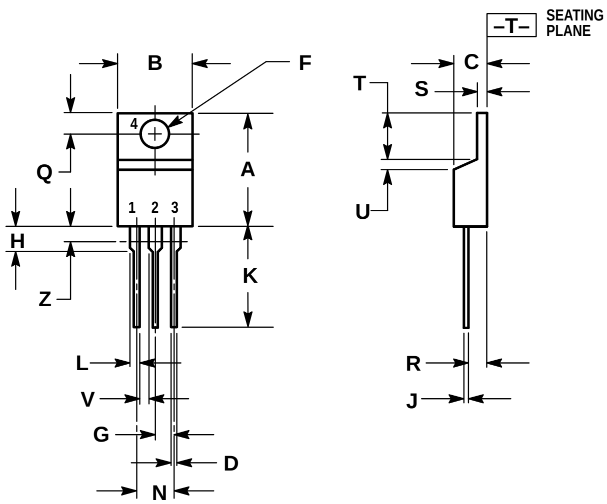


Figure 15. Forward Bias Power Derating

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A–06
TO–220AB
ISSUE Y

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