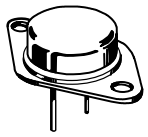
MJ410

High Voltage NPN Silicon Transistors

5 AMPERE POWER TRANSISTOR NPN SILICON 200 VOLTS 100 WATTS

. . . designed for medium to high voltage inverters, converters, regulators and switching circuits.

- High Collector–Emitter Voltage — V_{CEO} = 200 Volts
- DC Current Gain Specified @ 1.0 and 2.5 Adc
- Low Collector–Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.8 Vdc @ I_C = 1.0 Adc



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	200	Vdc
Collector–Base Voltage	V_{CB}	200	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak	I_C	5.0 10	Adc
Base Current	I_B	2.0	Adc
Total Device Dissipation @ T_C = 75°C Derate above 75°C	P_D	100 1.33	Watts W/°C
Operating Junction Temperature Range	T_J	–65 to +150	°C
Storage Temperature Range	T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.75	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	200	—	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	I_{CEO}	—	0.25	mAdc
Collector Cutoff Current (V_{CB} = 200 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	I_{CEX}	—	0.5	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	 30 10	 90 —	—
Collector–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	—	0.8	Vdc
Base–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{BE(sat)}$	—	1.2	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.5	—	MHz

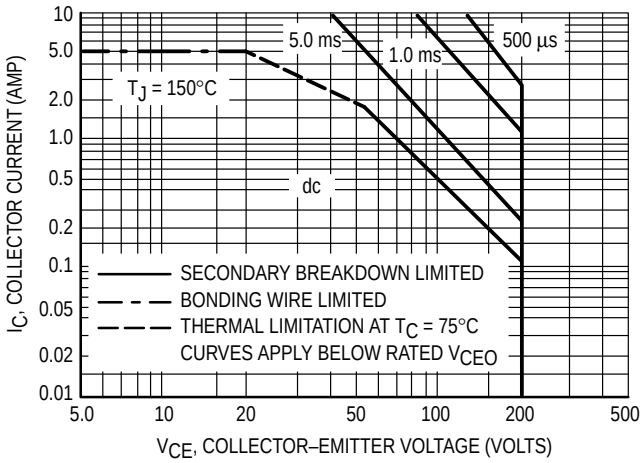


Figure 1. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation then the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values than the limitations imposed by second breakdown.

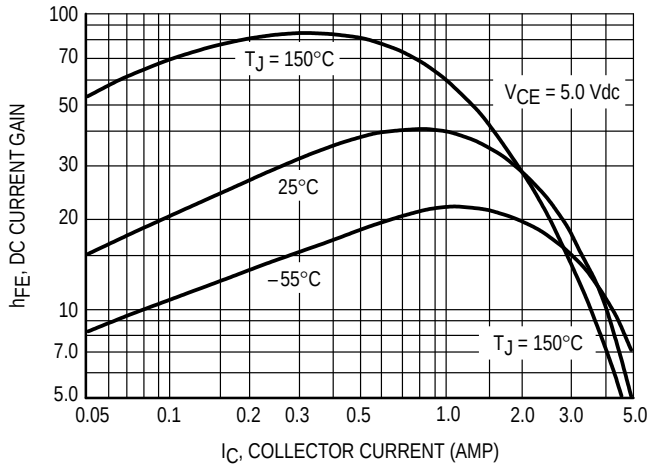


Figure 2. DC Current Gain

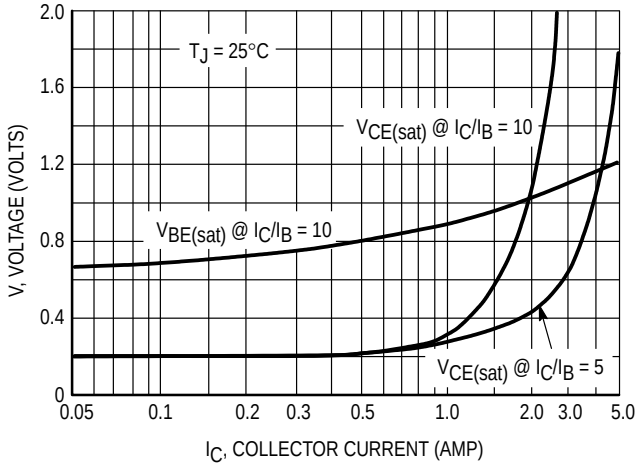


Figure 3. “On” Voltages

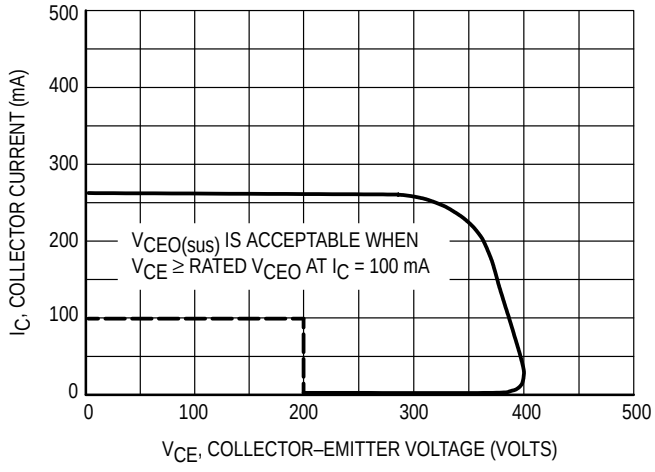


Figure 4. Sustaining Voltage Test Load Line

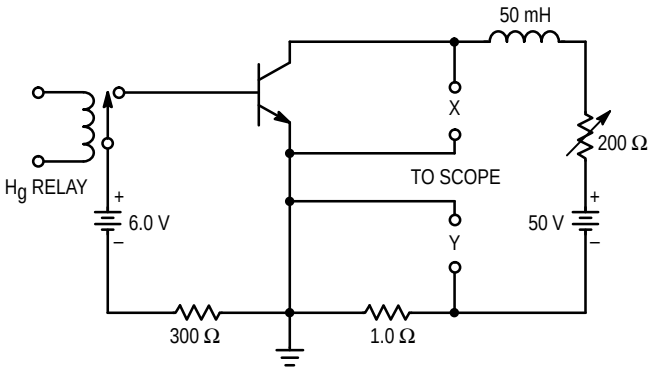
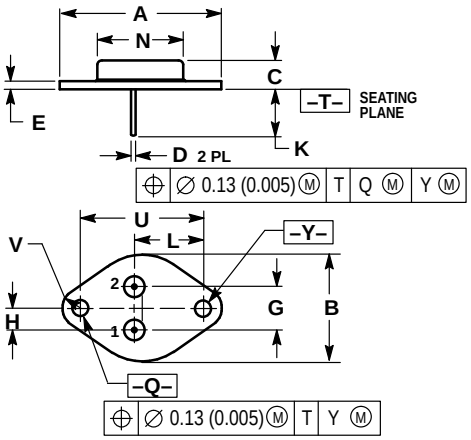


Figure 5. Sustaining Voltage Test Circuit

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

CASE 1–07
TO–204AA (TO–3)
ISSUE Z

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