MJ16018*
MJW16018*

*Motorola Preferred Device

POWER TRANSISTORS
10 AMPERES
800 VOLTS
125 AND 175 WATTS

Designer's™ Data Sheet

NPN Silicon Power Transistors

1.5 kV SWITCHMODE Series

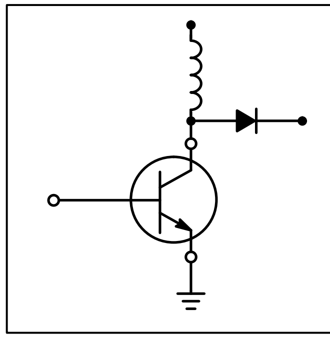
These transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line–operated switchmode applications.

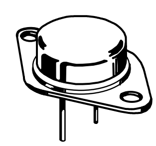
Typical Applications:

- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

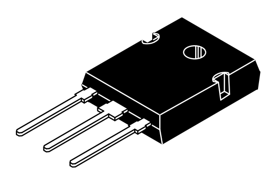
Features:

- Collector–Emitter Voltage — V_{CEV} = 1500 Vdc
- Fast Turn–Off Times
  80 ns Inductive Fall Time — 100°C (Typ)
  110 ns Inductive Crossover Time — 100°C (Typ)
  4.5 µs Inductive Storage Time — 100°C (Typ)
- 100°C Performance Specified for:
  Reverse–Biased SOA with Inductive Load
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents





CASE 1–07
TO–204AA
MJ16018



CASE 340F–03
TO–247AE
MJW16018

MAXIMUM RATINGS

Rating	Symbol	MJ16018	MJW16018	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	800		Vdc
Collector–Emitter Voltage	V_{CEV}	1500		Vdc
Emitter–Base Voltage	V_{EB}	6		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	10 15		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	8 12		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above T_C = 25°C	P_D	 175 100 1	 125 50 1	 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	–55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	1	°C/W
Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275		°C

(1) Pulse Test: Pulse Width = 5 µs, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS[1]					
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 50 mA, I_B = 0)	$V_{CEO(sus)}$	800	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 1500 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 1500 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	 — —	 — —	 0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)	I_{EBO}	—	—	0.1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 13			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 14			
ON CHARACTERISTICS[1]					
Collector–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 2 Adc) (I_C = 10 Adc, I_B = 5 Adc) (I_C = 5 Adc, I_B = 2 Adc, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 — — —	 1 5 1.5	Vdc
Base–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 2 Adc) (I_C = 5 Adc, I_B = 2 Adc, T_C = 100°C)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain (I_C = 5 Adc, V_{CE} = 5 Vdc)	h_{FE}	4	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 kHz)	C_{ob}	—	—	450	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Inductive Load (Table 1)							
Storage Time	Baker Clamped (I_C = 5 Adc, I_{B1} = 2 Adc, $V_{BE(off)}$ = 2 Vdc, $V_{CE(pk)}$ = 400 Vdc) PW = 25 μs	(T_J = 25°C)	t_{sv}	—	4000	8000	ns
Fall Time			t_{fi}	—	60	200	
Crossover Time			t_c	—	90	300	
Storage Time		(T_J = 100°C)	t_{sv}	—	4500	9000	
Fall Time			t_{fi}	—	80	250	
Crossover Time			t_c	—	110	375	
Resistive Load (Table 1)							
Delay Time	Baker Clamped (I_C = 5 Adc, V_{CC} = 250 Vdc, I_{B1} = 2 Adc, I_{B2} = 2 Adc, R_{B2} = 3 Ω, PW = 25 μs, Duty Cycle ≤ 2%)		t_d	—	85	200	ns
Rise Time			t_r	—	900	2000	
Storage Time			t_s	—	4500	9000	
Fall Time			t_f	—	200	400	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

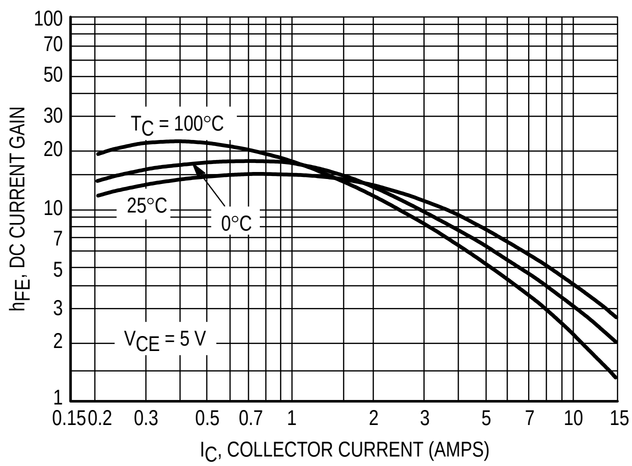


Figure 1. DC Current Gain

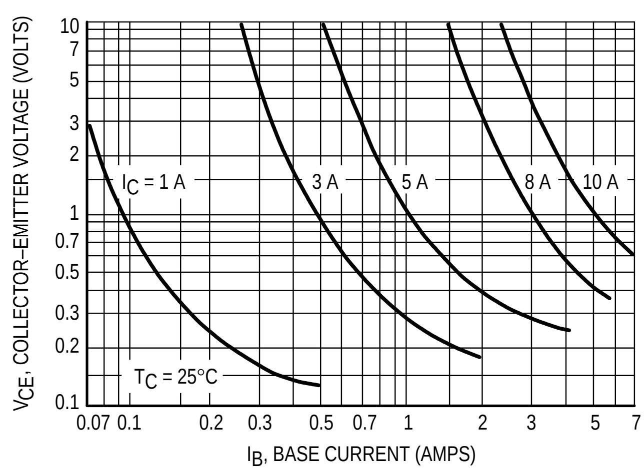


Figure 2. Collector Saturation Region

TYPICAL STATIC CHARACTERISTICS

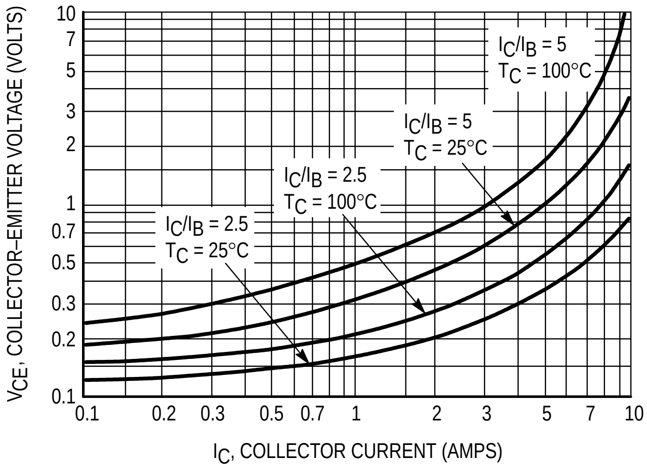


Figure 3. Collector–Emitter Saturation Region

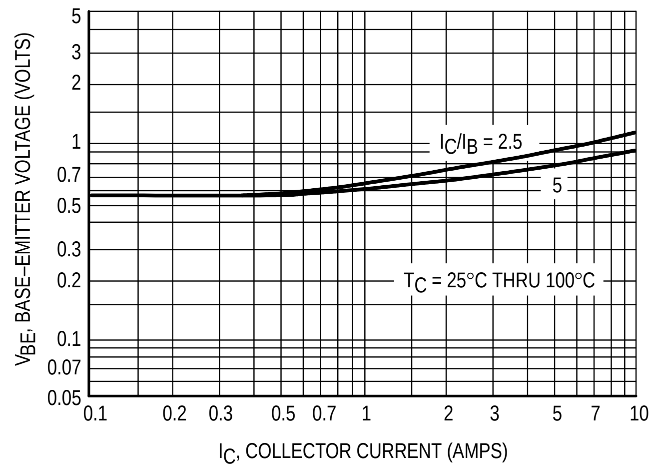


Figure 4. Base–Emitter Saturation Region

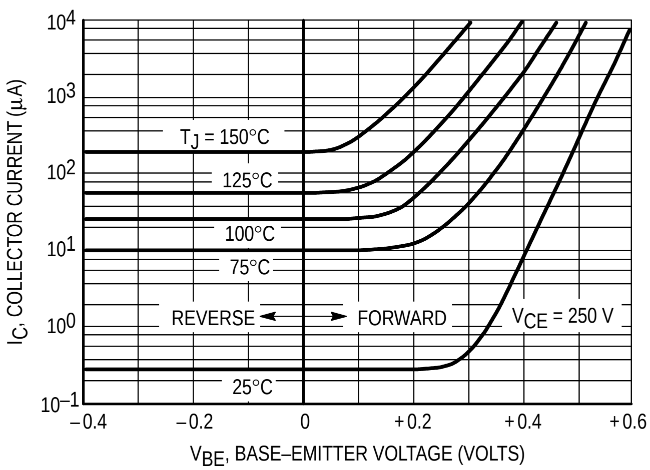


Figure 5. Collector Cutoff Region

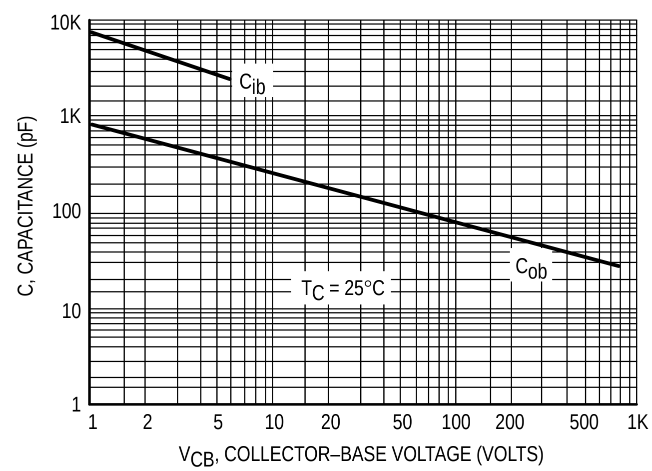


Figure 6. Typical Capacitance

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

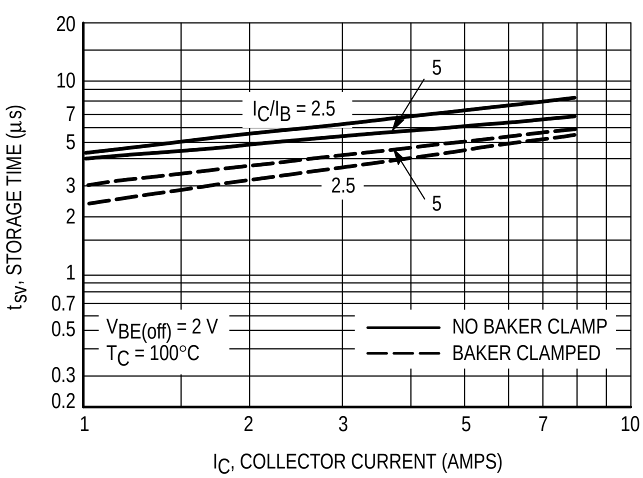


Figure 7. Storage Time

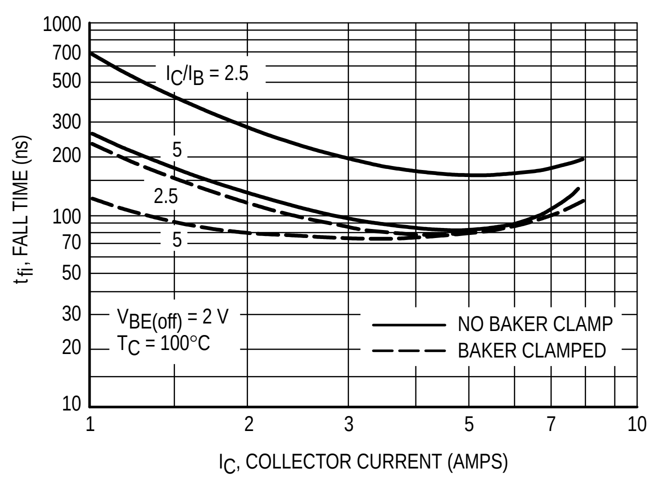


Figure 8. Inductive Switching Fall Time

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

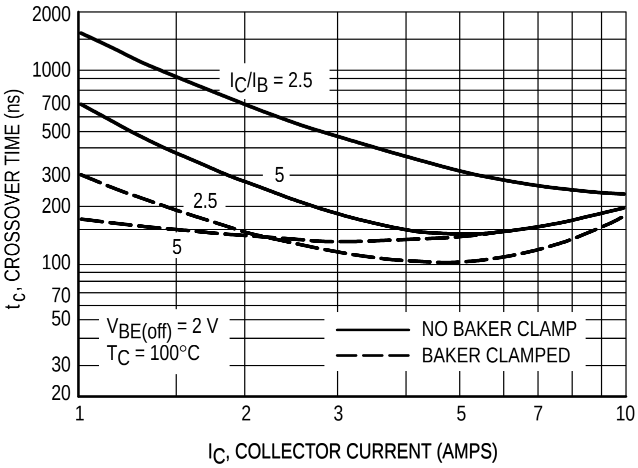


Figure 9. Inductive Switching Crossover Time

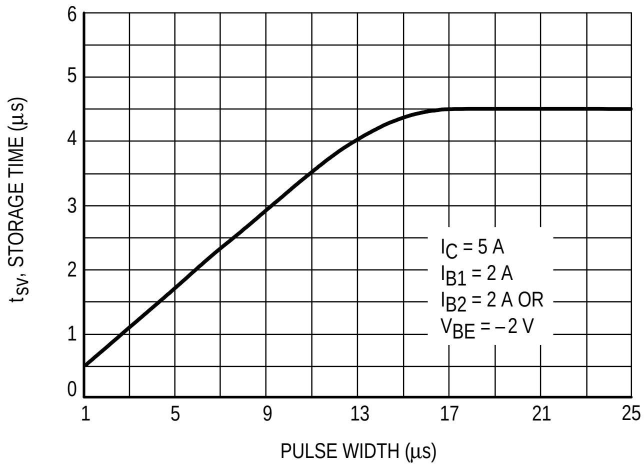


Figure 10. (t_{sv}) Storage Time versus I_{B1} Pulse Width

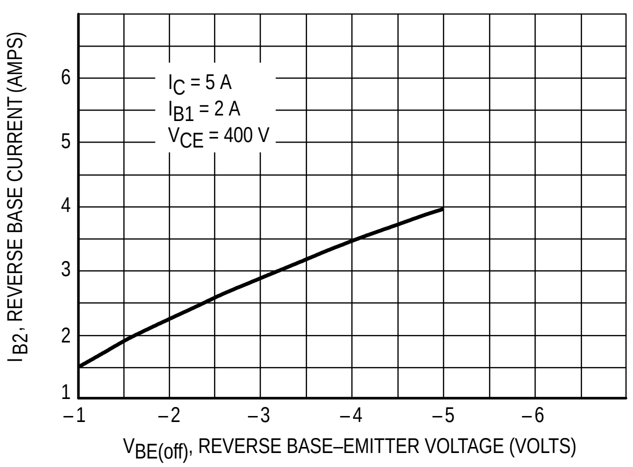


Figure 11. Reverse Base Current versus Off Voltage

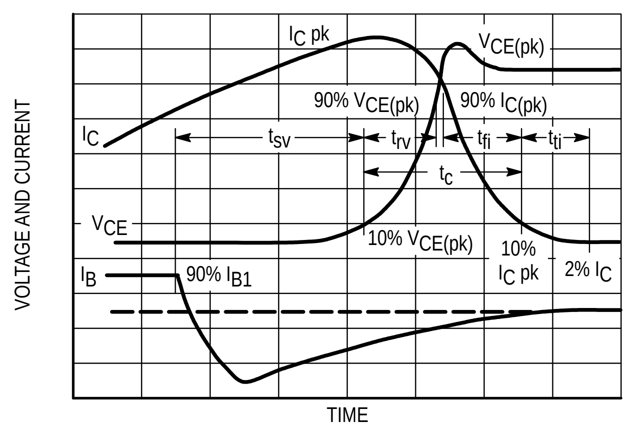


Figure 12. Inductive Switching Measurements

GUARANTEED SAFE OPERATING AREA LIMITS

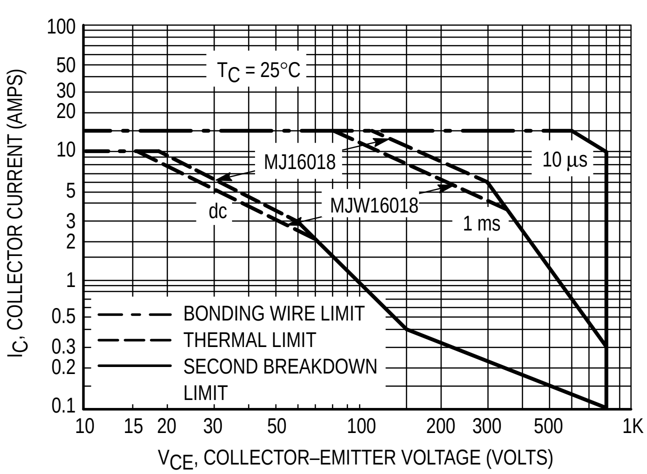


Figure 13. Maximum Forward Bias Safe Operating Area

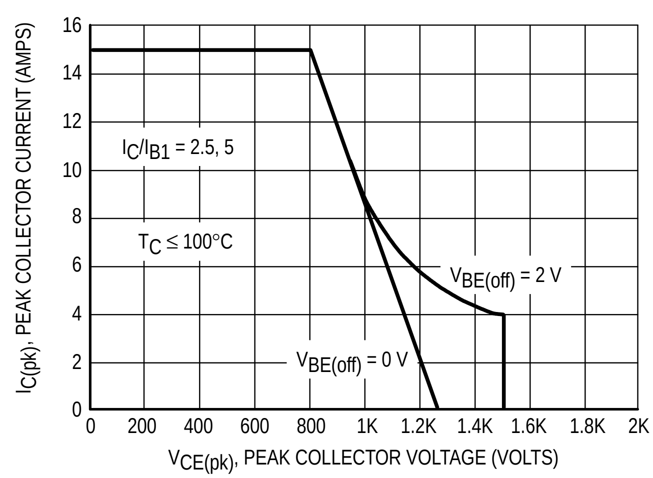


Figure 14. Maximum Reverse Bias Safe Operating Area

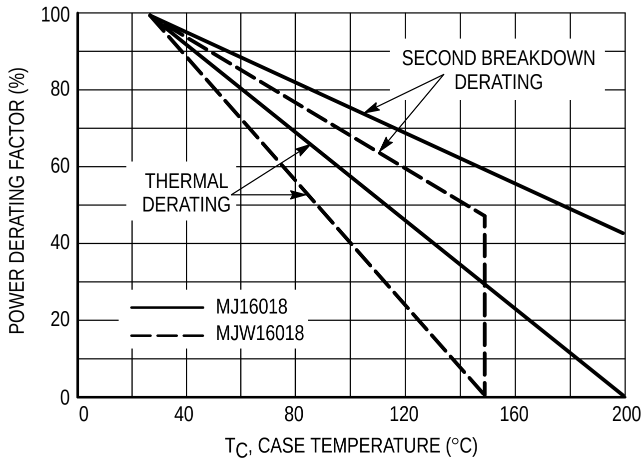


Figure 15. Power Derating

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 16. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base–to–emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

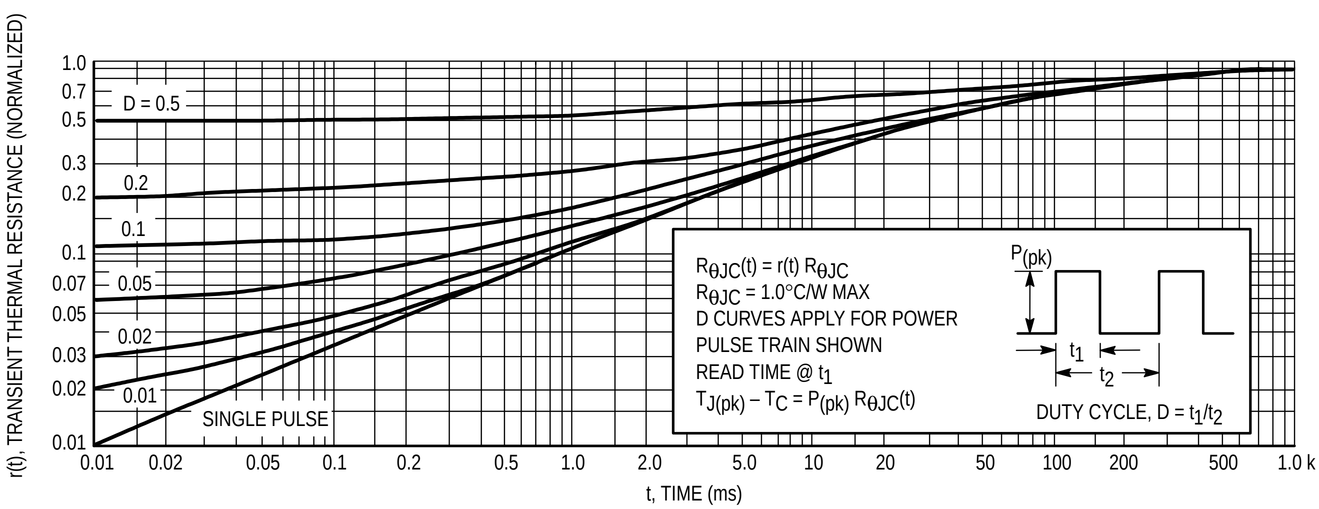


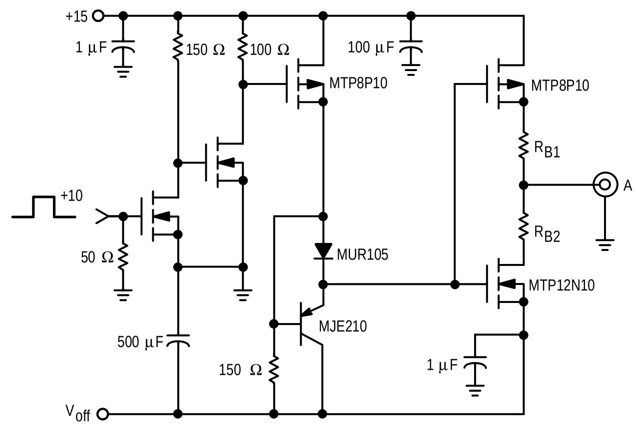
Figure 16. Thermal Response

Table 1. Test Conditions for Dynamic Performance

Input Conditions

$V_{CEO(sus)}$ / RBSOA / Inductive Switching

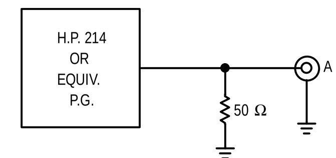
Drive Circuit

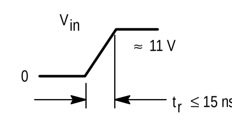


Note: Adjust V_{off} to obtain desired $V_{BE(off)}$ at Point A

Resistive Switching

For t_d and t_r:



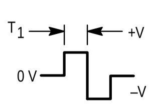


For t_s and t_f:
Inductive Switching Drive Circuit

Circuit Values

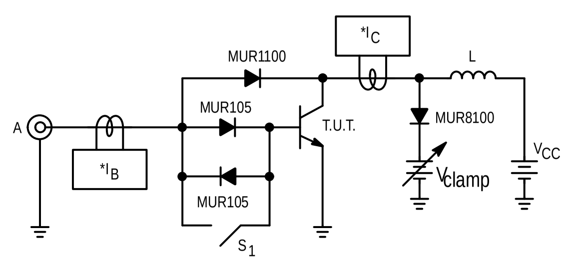
$V_{CEO(sus)}$	RBSOA	Inductive Switching	Resistive Switching
L = 10 mH $R_{B2} = \infty$ V_{CC} = 20 Volts $I_{(pk)}$ = 50 mA S_1 Closed	L = 200 µH R_{B2} = 0 V_{CC} = 20 Volts R_{B1} selected for desired I_{B1} S_1 Closed	L = 200 µH R_{B2} = 0 when $V_{BE(off)}$ is specified or selected for desired I_{B2} $V_{CC} \approx$ 20 Volts, Adjusted to obtain desired IC R_{B1} selected for desired I_{B1} S_1 = Open for baker clamp condition	**for t_d and t_r** V_{CC} = 250 Volts R_B selected for desired I_{B1} R_L selected for desired I_C **for t_s and t_f** V_{CC} = 250 Volts R_B = 0 R_{B1} & R_{B2} selected for I_{B1} & I_{B2} R_L selected for desired I_C

Test Circuit



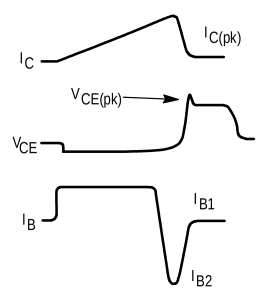
$T_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$

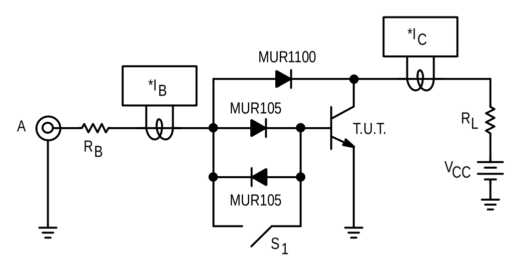
T_1 adjusted to obtain $I_{C(pk)}$



*Tektronix AM503
P6302 or Equivalent

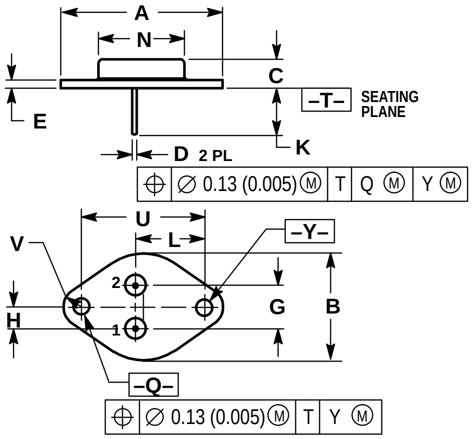
Scope — Tektronix
7403 or Equivalent





*Tektronix AM503
P6302 or Equivalent

PACKAGE DIMENSIONS

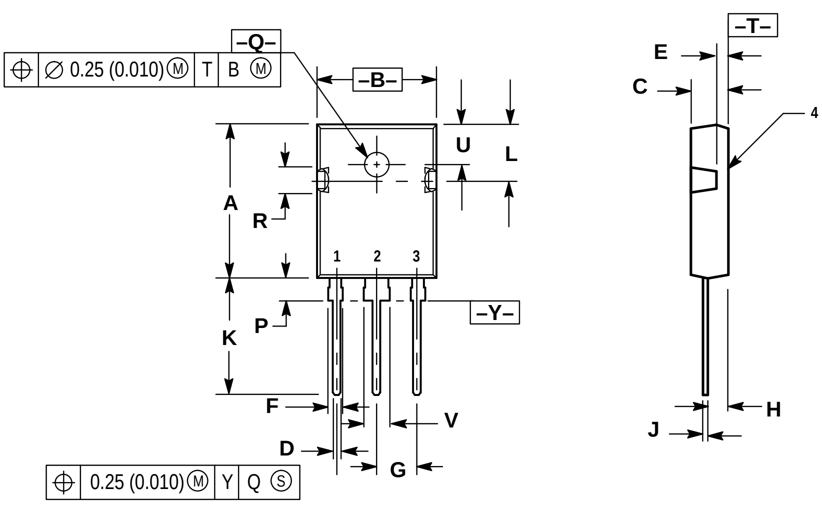


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.550 REF		39.37 REF	
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

CASE 1–07
TO–204AA (TO–3)
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.40	20.90	0.803	0.823
B	15.44	15.95	0.608	0.628
C	4.70	5.21	0.185	0.205
D	1.09	1.30	0.043	0.051
E	1.50	1.63	0.059	0.064
F	1.80	2.18	0.071	0.086
G	5.45 BSC		0.215 BSC	
H	2.56	2.87	0.101	0.113
J	0.48	0.68	0.019	0.027
K	15.57	16.08	0.613	0.633
L	7.26	7.50	0.286	0.295
P	3.10	3.38	0.122	0.133
Q	3.50	3.70	0.138	0.145
R	3.30	3.80	0.130	0.150
U	5.30 BSC		0.209 BSC	
V	3.05	3.40	0.120	0.134

STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 340F–03
TO–247AE
ISSUE E

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