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512K x 8 FLASH

MFM8516 - 70/90/12/15

Issue 4.7 : November 1998

Description

The MFM8516 is a 4M Bit CMOS 5V only Flash monolithic device organised : 512K x 8. The device offers fast access times of 70/90/120 and 150ns and 5V program/erase.

The device has a 64 KByte sector size. The Program and Erase procedure is simplified via automatic program and erase algorithms.

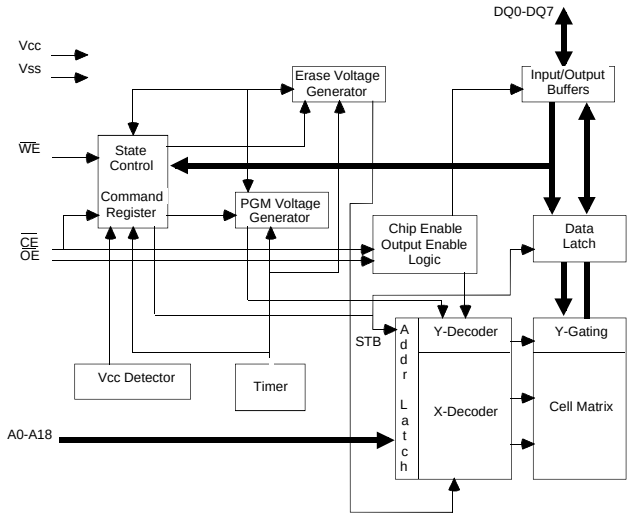
The MFM8516 has a 10K cycle write erase cycle endurance (100K cycle E-Part) and a 10 year data retention time.

524,288 bit FLASH EEPROM

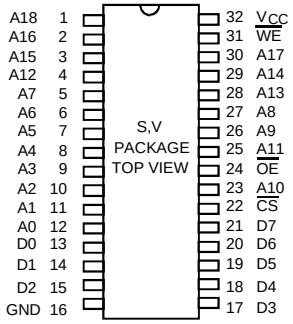
Features

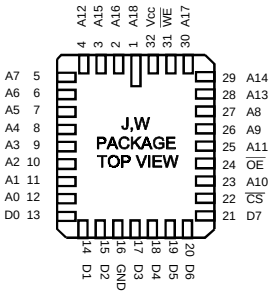
- 4 Megabit FLASH memory.
- Fast Access Times of 70/90/120/150 ns.
- Operating Power 247.50 mW (max),
  Low Power Standby (CMOS) 632.50µW (max).
- Automatic Write/Erase by Embedded Algorithm - end of Write/Erase indicated by DATA Polling and Toggle Bit.
- Flexible Sector Erase Architecture - 64K byte sector size, with hardware protection of any number of sectors.
- Byte Program of 16µs (Typ), Sector Program of 2s (Typ)
- Erase/Write Cycle Endurance, Standard 10,000 (min)
  Extended 100,000 (min)
- 10 year data retention.
- May be screened in accordance with MIL-STD-883.

Block Diagram



Pin Definitions





Package Details

Pin Count	Description	Package Type
32	Dual In-line	S
32	JLCC (J Leaded Chip Carrier)	J
32	LCC (Leadless Chip Carrier)	W
32	Vertical-in-Line	V

Pin Functions

A0-A18	Address Inputs
D0-D7	Data Inputs/Outputs
$\overline{CS}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power (+5V)
GND	Ground

DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

		unit
Voltage on any pin w.r.t. Gnd	-2.0 to +7	V
Supply Voltage (2)	-2.0 to +7	V
Voltage on A9 w.r.t. Gnd (3)	-2.0 to +14	V
Storage Temperature	-65 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied.

(2) Minimum DC voltage on any input or I/O pin is -0.5V. Maximum DC voltage on output and I/O pins is Vcc+0.5V During transitions voltage may overshoot by +/-2V for up to 20ns

(3) Minimum DC input voltage on A9 is -0.5V during voltage transitions, A9 may overshoot Vss to -2V for periods of up to 20ns, maximum DC input voltage in A9 is 13.5V which may overshoot to 14.0V for periods up to 20ns

Recommended Operating Conditions

Parameter		*min*	*typ*	*max*	*unit*
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage (TTL)	V_{IH}	2.0	-	V_{CC}+0.5	V
Input Low Voltage (TTL)	V_{IL}	-0.5	-	0.8	V
Input High Voltage (CMOS)	V_{IH}	$0.7V_{CC}$	-	V_{CC}+0.3	V
Input Low Voltage (CMOS)	V_{IL}	-0.5	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (-I suffix)
	T_{AM}	-55	-	125	°C (-M\MB suffix)

DC Electrical Characteristic (T_A=-55°C to +125°C,V_{CC}=5V ± 10%)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
I/P Leakage Current Address, $\overline{OE}$	I_{LI1}	V_{CC} = V_{CC} max, V_{IN} = 0V or V_{CC}	-	-	±1	µA
A9 Input Leakage Current	I_{LI2}	V_{CC} = V_{CC} max, A9 = 12.5V	-	-	50	µA
Other Pins	I_{LI3}	V_{CC} = V_{CC} max, V_{IN} = 0V or V_{CC}	-	-	±1	µA
Output Leakage Current	I_{LO}	V_{CC} = V_{CC} max, V_{OUT} = 0V or V_{CC}	-	-	±1	µA
V_{CC} Operating Current	I_{CCO}	$\overline{CS}$ = V_{IL}, $\overline{OS}$ = V_{IH}, I_{OUT} = 0mA, *f* = 6MHz	-	-	45	mA
V_{CC} Program/Erase Current	I_{CCP}	Programming in Progress	-	-	65	mA
Standby Supply Current TTL	I_{SB}	V_{CC} = V_{CC} max, $\overline{CS}$ = V_{IH} $\overline{OE}$ = V_{IH}	-	-	1.5	mA
CMOS	I_{SB1}	V_{CC} = V_{CC} max, $\overline{CS}$ = V_{CC}+0.5, $\overline{OE}$ = V_{IL}	-	-	115	µA
Autoselect / Sector Protect Voltage	V_{ID}	V_{CC} = 5.0V	11.5	-	12.5	V
Output Low Voltage	V_{OL}	I_{OL} = 10mA. V_{CC} = V_{CC} min.	-	-	0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -2.5mA. V_{CC} = V_{CC} min.	2.4	-	-	V
Low V_{CC} Lock-Out Voltage	V_{LKO}		3.2	-	4.2	V

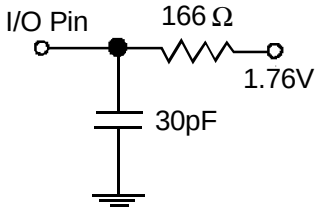
Capacitance (T_A=25°C,f=1MHz)

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	C_{IN1}	V_{IN} = 0V	-	10	pF
Control Pin Capacitance	C_{IN2}	V_{PP} = 0V	-	12	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	-	12	pF

Note: These parameters are calculated, not measured.

AC Test Conditions

* Input pulse levels : 0.0V to 3.0V
* Input rise and fall times : 5 ns
* Input and output timing reference levels : 1.5V
* VCC = 5V +/- 10%



AC OPERATING CONDITIONS

Read Cycle

Parameter	*Symbol*	70			90			
		min	typ	max	min	typ	max	Unit
Read Cycle Time	t_{RC}	70	-	-	90	-	-	ns
Address to output delay	t_{ACC}	-	-	70	-	-	90	ns
Chip enable to output	t_{CE}	-	-	70	-	-	90	ns
Output enable to output	t_{OE}	-	-	30	-	-	35	ns
Output enable to output High	Zt_{DF}	-	-	20	-	-	20	ns
Output hold time from address	t_{OH}	0	-	-	0	-	-	ns

$\overline{CS}$ or $\overline{OE}$ whichever occurs first

Parameter	*Symbol*	120			150			
		min	typ	max	min	typ	max	Unit
Read Cycle Time	t_{RC}	120	-	-	150	-	-	ns
Address to output delay	t_{ACC}	-	-	120	-	-	150	ns
Chip enable to output	t_{CE}	-	-	120	-	-	150	ns
Output enable to output	t_{OE}	-	-	50	-	-	55	ns
Output enable to output High	Zt_{DF}	-	-	30	-	-	35	ns
Output hold time from address	t_{OH}	0	-	-	0	-	-	ns

$\overline{CS}$ or $\overline{OE}$ whichever occurs first

Write/Erase/Program

Parameter	*Symbol*	*70*			*90*			
		min	typ	max	min	typ	max	unit
Write Cycle time (2)	t_{WC}	70	-	-	90	-	-	ns
Address Setup time	t_{AS}	0	-	-	0	-	-	ns
Address Hold time	t_{AH}	45	-	-	45	-	-	ns
Data Setup Time	t_{DS}	30	-	-	45	-	-	ns
Data hold Time	t_{DH}	0	-	-	0	-	-	ns
Output Enable Setup Time	t_{OES}	0	-	-	0	-	-	ns
Read Recover before Write	t_{GHWL}	0	-	-	0	-	-	ns
$\overline{CS}$ setup time	t_{CE}	0	-	-	0	-	-	ns
$\overline{CS}$ hold time	t_{CH}	0	-	-	0	-	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	35	-	-	45	-	-	ns
$\overline{WE}$ Pulse Width High	t_{WPH}	20	-	-	20	-	-	ns
Byte Programming operation	t_{WHWH1}	-	16	-	-	16	-	µs
Sector Erase operation (1)	t_{WHWH2}	-	2	30	-	2	30	sec
Chip Erase operation (1)	t_{WHWH3}	-	14	120	-	14	120	sec
Vcc setup time (2)	t_{VCS}	50	-	-	50	-	-	µs

Parameter	*Symbol*	*120*			*150*			
		min	typ	max	min	typ	max	unit
Write Cycle time (2)	t_{WC}	120	-	-	150	-	-	ns
Address Setup time	t_{AS}	0	-	-	0	-	-	ns
Address Hold time	t_{AH}	50	-	-	50	-	-	ns
Data Setup Time	t_{DS}	50	-	-	50	-	-	ns
Data hold Time	t_{DH}	0	-	-	0	-	-	ns
Output Enable Setup Time	t_{OES}	0	-	-	0	-	-	ns
Read Recover before Write	t_{GHWL}	0	-	-	0	-	-	ns
$\overline{CS}$ setup time	t_{CE}	0	-	-	0	-	-	ns
$\overline{CS}$ hold time	t_{CH}	0	-	-	0	-	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	50	-	-	50	-	-	ns
$\overline{WE}$ Pulse Width High	t_{WPH}	20	-	-	20	-	-	ns
Byte Programming operation	t_{WHWH1}	-	16	-	-	16	-	µs
Sector Erase operation (1)	t_{WHWH2}	-	2	30	-	2	30	sec
Chip Erase operation (1)	t_{WHWH3}	-	14	120	-	14	120	sec
Vcc setup time (2)	t_{VCS}	50	-	-	50	-	-	µs

Notes: (1) This does not include the preprogramming time.
(2) Not 100% tested.

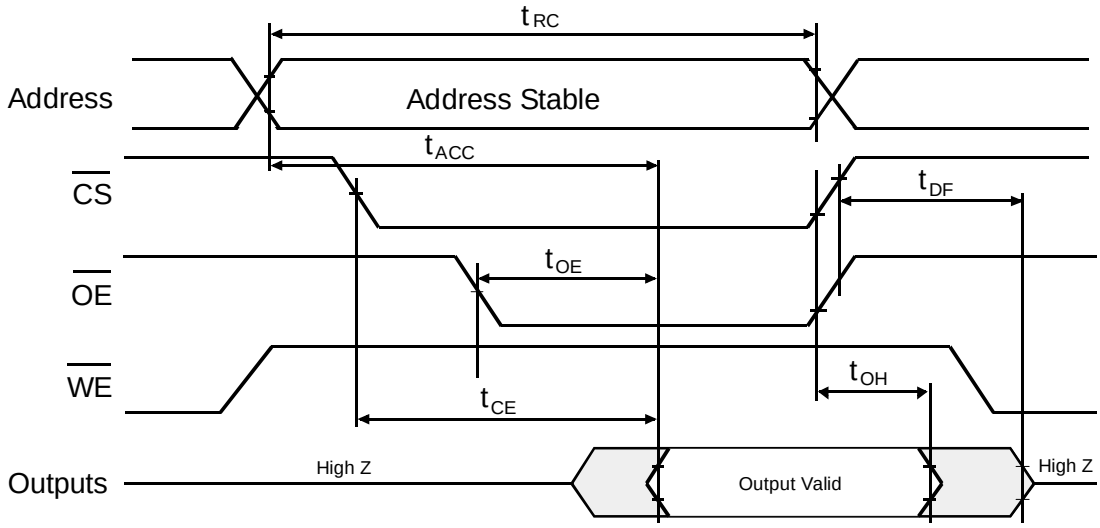
Write/Erase/Program Alternate $\overline{CS}$ controlled Writes

Parameter	*Symbol*	*70*			*90*			
		min	typ	max	min	typ	max	unit
Write Cycle time (2)	t_{WC}	70	-	-	90	-	-	ns
Address Setup time	t_{AS}	0	-	-	0	-	-	ns
Address Hold time	t_{AH}	45	-	-	45	-	-	ns
Data Setup Time	t_{DS}	30	-	-	45	-	-	ns
Data hold Time	t_{DH}	0	-	-	0	-	-	ns
Output Enable Setup Time	t_{OES}	0	-	-	0	-	-	ns
Read Recover before Write	t_{GHEL}	0	-	-	0	-	-	ns
$\overline{WE}$ setup time	t_{WS}	0	-	-	0	-	-	ns
$\overline{WE}$ hold time	t_{WH}	0	-	-	0	-	-	ns
$\overline{CS}$ Pulse Width	t_{CP}	35	-	-	45	-	-	ns
$\overline{CS}$ Pulse Width High	t_{CPH}	20	-	-	20	-	-	ns
Programming operation	t_{WHWH1}	-	16	-	-	16	-	us
Sector Erase operation (1)	t_{WHWH2}	-	2	30	-	2	30	sec
Chip Erase operation (1)	t_{WHWH3}	-	14	120	-	14	120	sec
Vcc setup time (2)	t_{VCS}	-	50	-	-	50	-	us

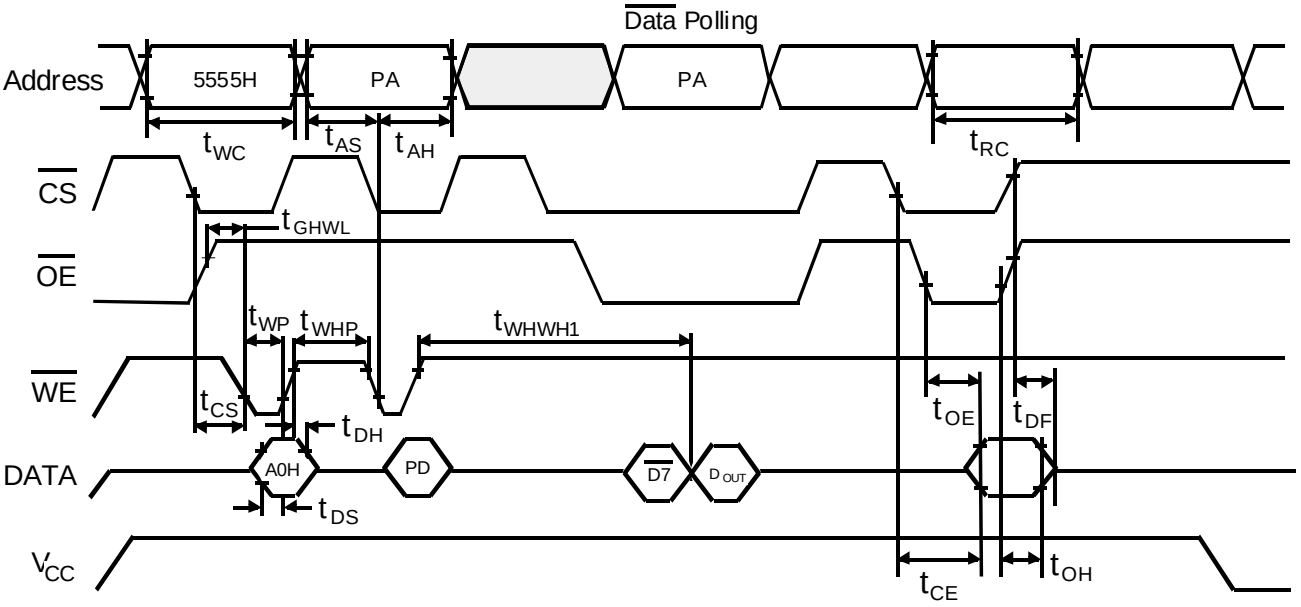
Parameter	*Symbol*	*120*			*150*			
		min	typ	max	min	typ	max	unit
Write Cycle time (2)	t_{WC}	120	-	-	150	-	-	ns
Address Setup time	t_{AS}	0	-	-	0	-	-	ns
Address Hold time	t_{AH}	50	-	-	50	-	-	ns
Data Setup Time	t_{DS}	50	-	-	50	-	-	ns
Data hold Time	t_{DH}	0	-	-	0	-	-	ns
Output Enable Setup Time	t_{OES}	0	-	-	0	-	-	ns
Read Recover before Write	t_{GHEL}	0	-	-	0	-	-	ns
$\overline{WE}$ setup time	t_{WS}	0	-	-	0	-	-	ns
$\overline{WE}$ hold time	t_{WH}	0	-	-	0	-	-	ns
$\overline{CS}$ Pulse Width	t_{CP}	50	-	-	50	-	-	ns
$\overline{CS}$ Pulse Width High	t_{CPH}	20	-	-	20	-	-	ns
Programming operation	t_{WHWH1}	-	16	-	-	16	-	us
Sector Erase operation (1)	t_{WHWH2}	-	2	30	-	2	30	sec
Chip Erase operation (1)	t_{WHWH3}	-	14	120	-	14	120	sec
Vcc setup time (2)	t_{VCS}	-	50	-	-	50	-	us

Note: (1) Does not include pre-programming time.
(2) Not 100% tested.

AC Waveforms for Read Operation



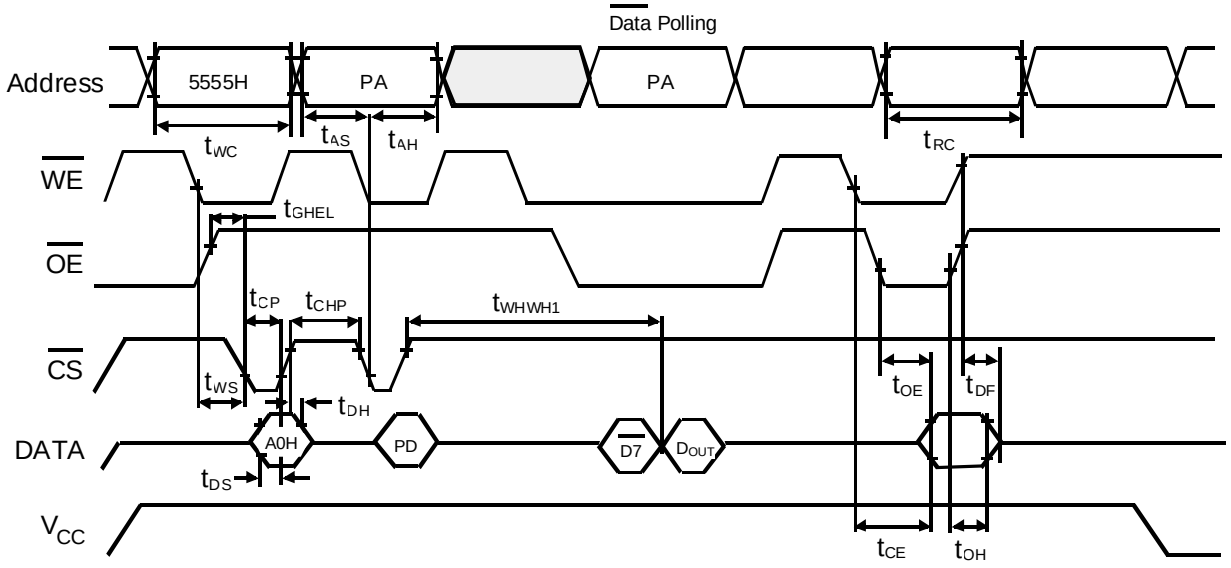
AC Waveforms Program



Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

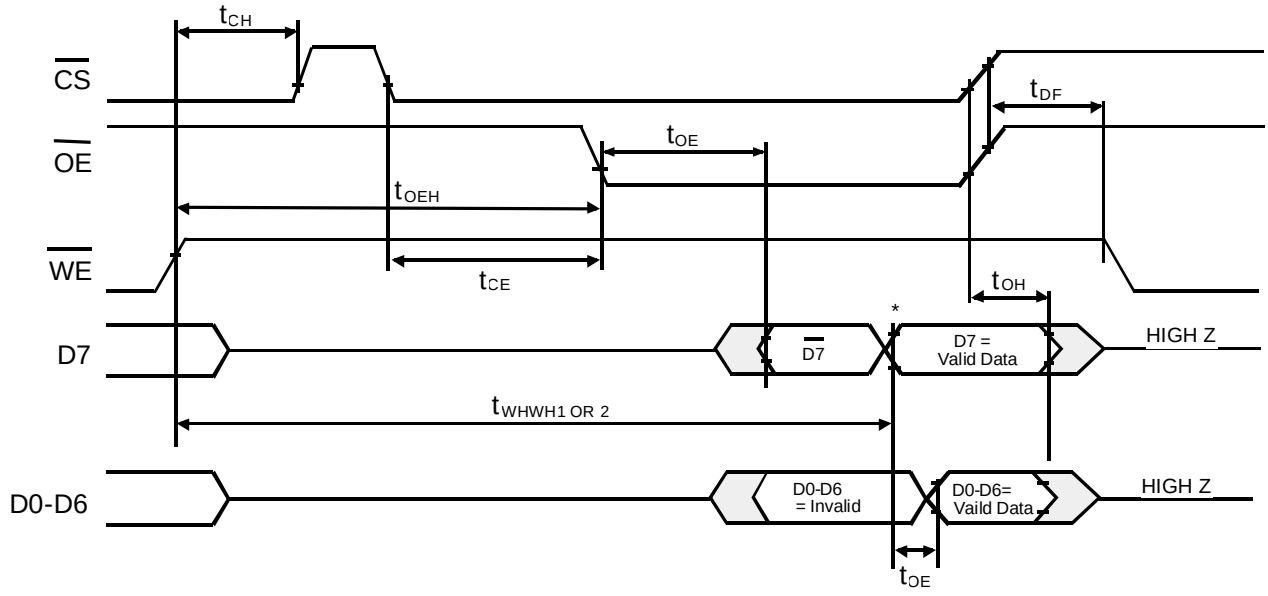
A.C Waveforms - Alternate $\overline{CS}$ controlled Program operation timings



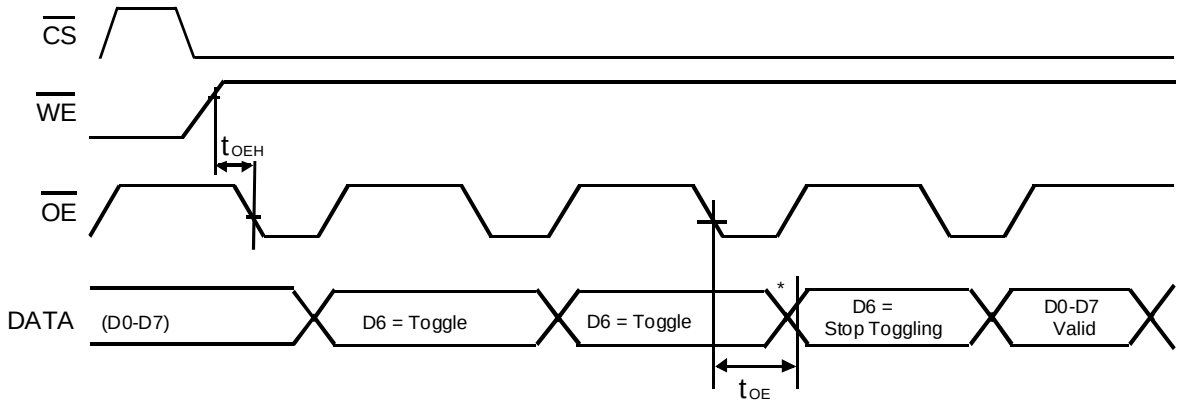
NOTES:

1. PA is address of memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

AC Waveforms for Data Polling During Embedded Algorithm Operations

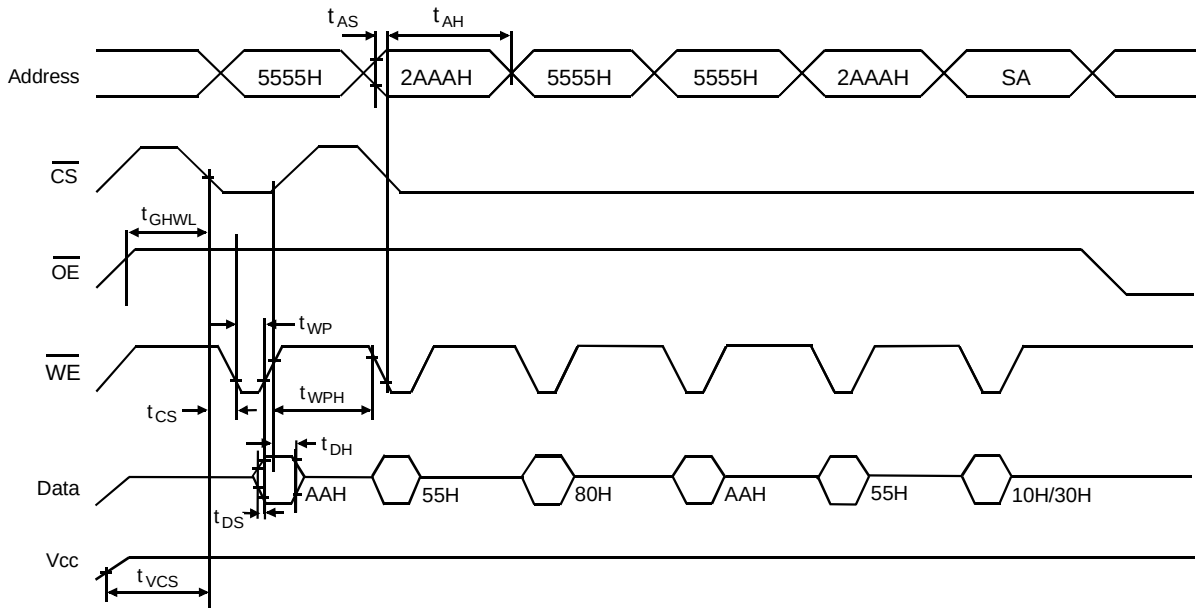


AC Waveforms for Toggle Bit During Embedded Algorithm Operations



* D6 stops toggling (the device has completed the embedded operations)

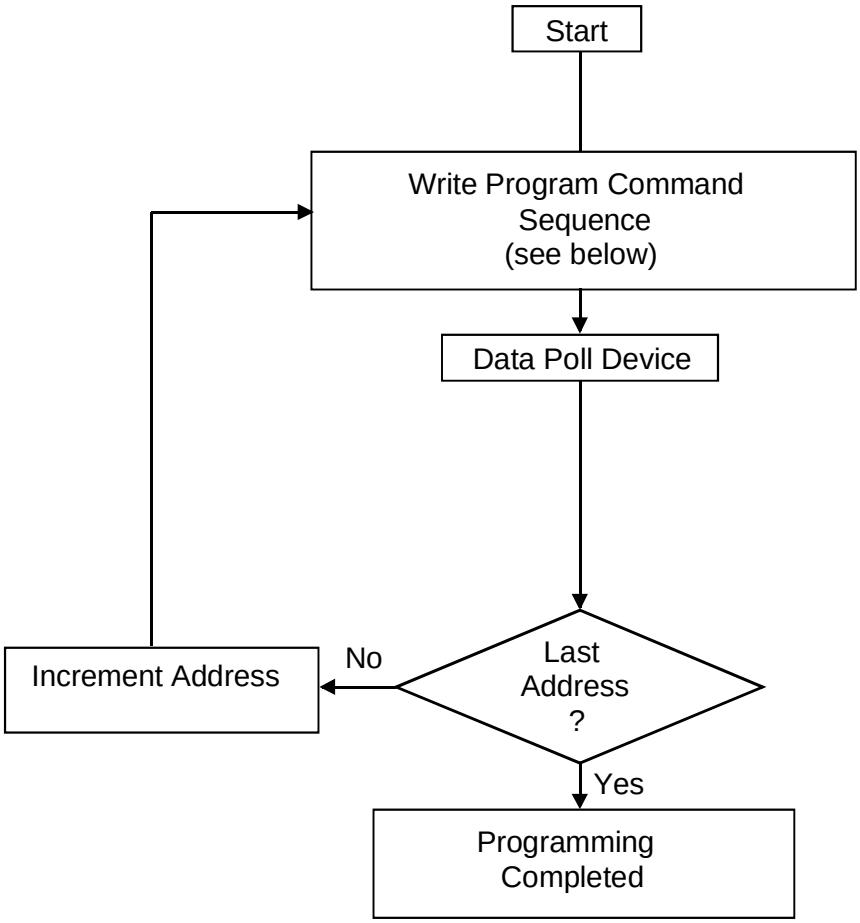
AC Waveforms Chip / Sector Erase



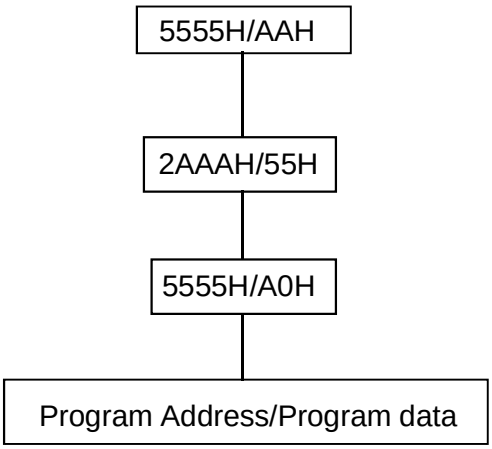
NOTES:

1. SA is the address for sector erase. Addresses = don't care for Chip Erase.

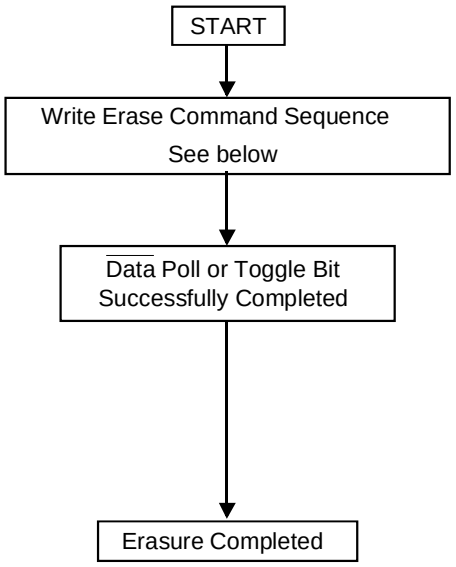
EMBEDDED PROGRAMMING ALGORITHM



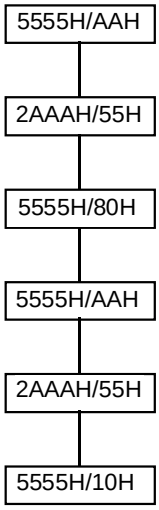
Program Command Sequence (Address /Command)



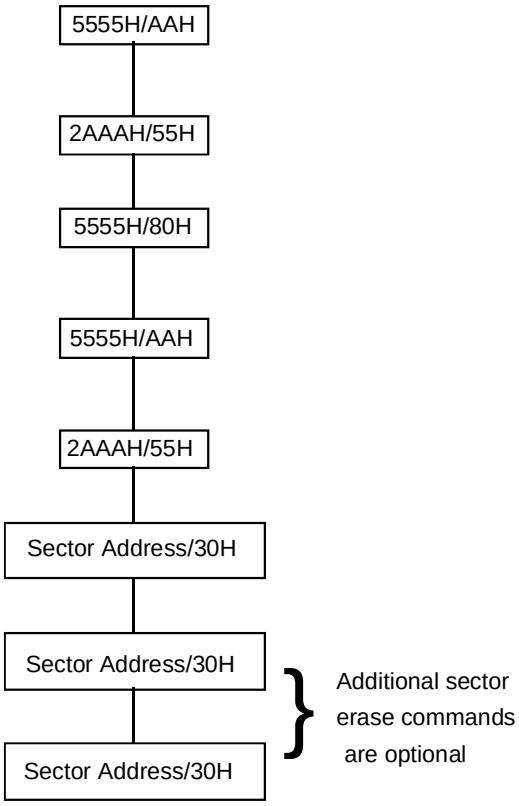
EMBEDDED ERASE ALGORITHM



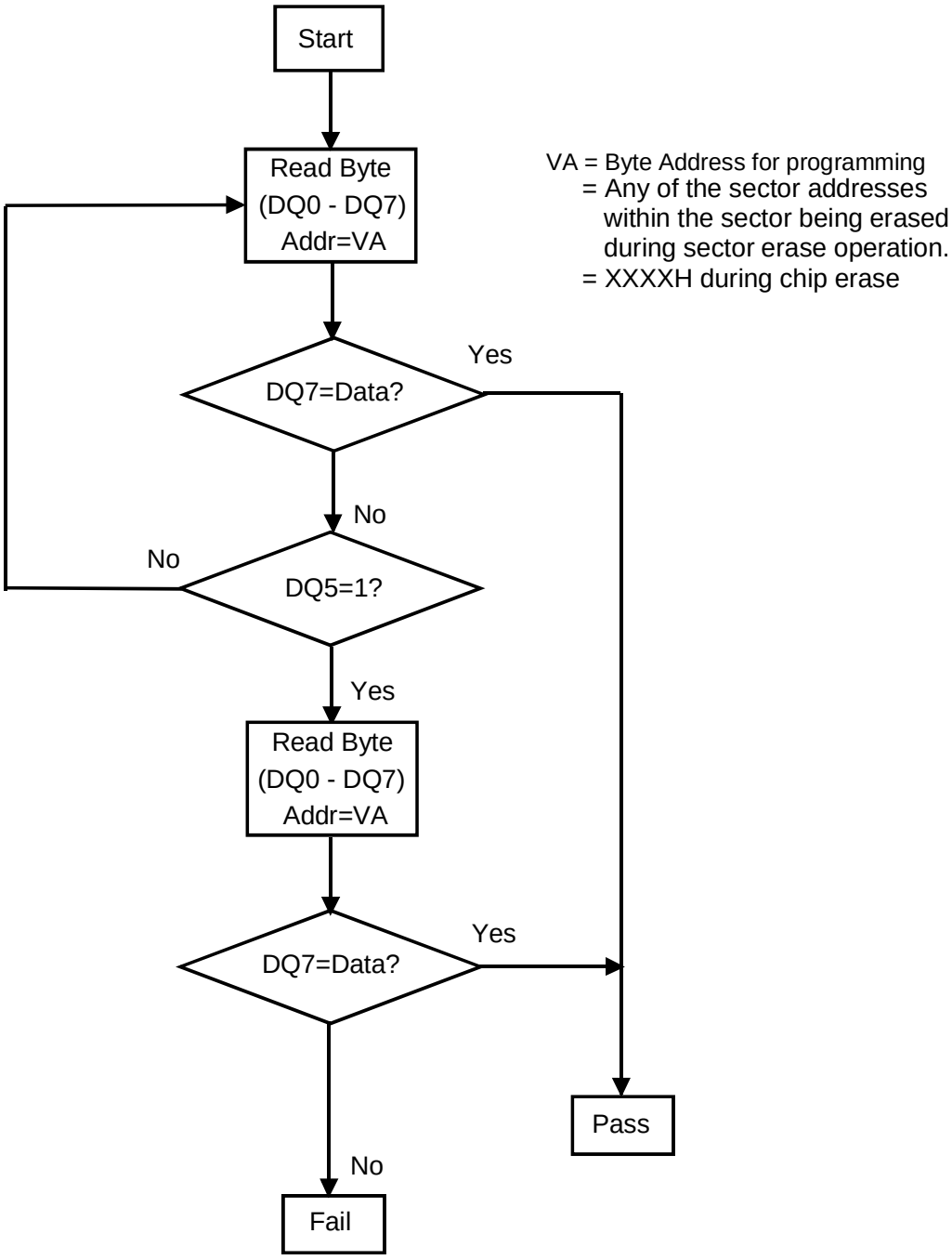
Chip Erase Command Sequence
(Address/Command):



Individual Sector/Mulitiple Sector
Erase Command Sequence
(Address/Command):

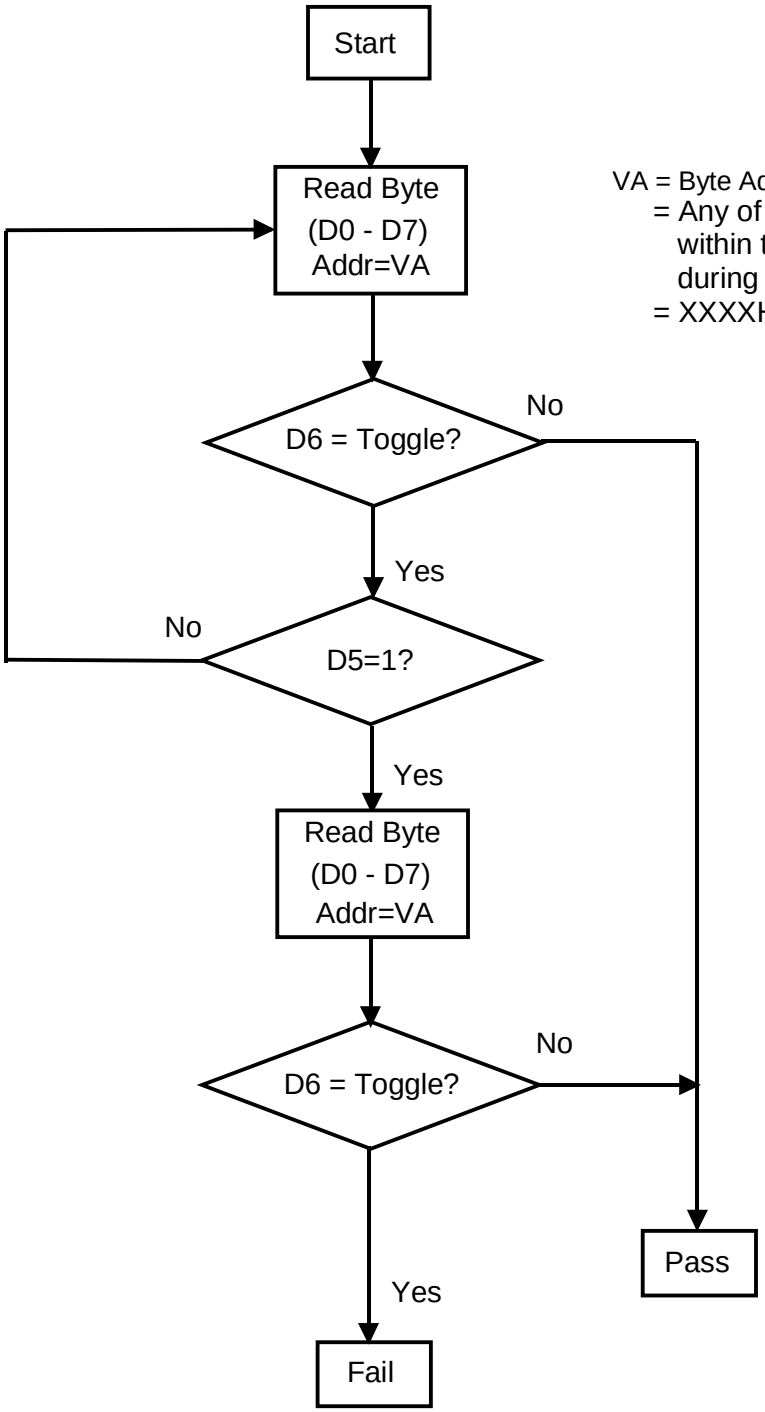


DATA POLLING ALGORITHM



Note : DQ7 is rechecked even if DQ5 = "1" beceause DQ7 may change simultaneously with DQ5.

TOGGLE BIT ALGORITHM



Note : D6 is rechecked even if D5 = "1" because D6 may stop toggling at the same time as D5 changing to "1"

DEVICE OPERATION

Read Mode

The MFM8516 has two control functions which must be satisfied in order to obtain data at the outputs
$\overline{CS}$ is the power control and should be used for device selection.
$\overline{OE}$ is the output control and should be used to gate data to the output pins if the device is selected.

Standby Mode

Two standby modes are available : CMOS standby : $\overline{CS}$ held at Vcc +/- 0.5V
TTL standby : $\overline{CS}$ held at V_{IH}

In the standby mode the outputs are in a high impedance state independent of the $\overline{OE}$ input. If the device is deselected during erasure or programming the device will draw active current until the operation is completed.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

This mode is intended for use by programming equipment. This mode is functional over the full military temperature range. The autoselect codes as follows :

Type	A18	A17	A16	A6	A1	A0	Code (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
Sector Protection	Sector Address			V_{IL}	V_{IH}	V_{IL}	01H*	0	0	0	0	0	0	0	1

* Outputs 01H at protected sector address

To activate this mode the programming equipment must force V_{ID} on address A9 . All addresses are don't care apart from A0, A1 & A6.

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The register is a latch used to store the commands along with the address and data information required to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL} while $\overline{CS}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CS}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CS}$, whichever happens first.

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. The following table defines these register command sequences.

Command Sequence Read/Reset	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	XXXH	F0H										
Read/Reset	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Autoselect	3	5555H	AAH	2AAAH	55H	5555H	90H						
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	Data				
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
Sector Erase Suspend		Erase can be suspended during sector erase with Addr (don't care) Data (B0H)											
Sector Erase Resume		Erase can be resumed after suspend with Addr (Don't Care), Data (30H)											

NOTES:

1. Address bit A_{15},A_{16},A_{17}, A_{18}=X=Don't care. Write Sequences may be initiated with A_{15} in either state.

2. Address bit A_{15},A_{16},A_{17}, A_{18}=X=Don't care for all address commands except for Program Address (PA) and Sector Address (SA).

3. RA=Address of the memory location to be read.

   PA=Address of memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.

   SA=Address of the sector to be erased. The combination of A_{18}, A_{17} and A_{16} will uniquely select any sector.

4. RD=Data read from location RA during read operation.

   PD=Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$

5. Read and byte program functions to non-erasing sectors are allowed in the Erase Suspend mode.

Read / Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

Sector Protection

The MFM8516 features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 8). The sector protect feature is enabled using programming equipment at the users site. The device is shipped with all sectors unprotected.

It is also possible to determine if a sector is protected in the system by writing the Autoselect command. Performing a read operation at the address location XX02H, where the higher order addresses (A16, A17, A18) are the sector addresses will produce a logical "1" at D0 for a protected sector.

Sector Address Table

	A18	A17	A16	Address Range
SA0	0	0	0	00000h-0FFFFh
SA1	0	0	1	10000h-1FFFFh
SA2	0	1	0	20000h-2FFFFh
SA3	0	1	1	30000h-3FFFFh
SA4	1	0	0	40000h-4FFFFh
SA5	1	0	1	50000h-5FFFFh
SA6	1	1	0	60000h-6FFFFh
SA7	1	1	1	70000h-7FFFFh

Sector Unprotect

The MFM8516 also features a sector unprotect mode so that a potected sector may be unprotected to incorporate any changes in the code. The sector unprotect is enabled using programming equipment at the user's site. It is also possible to determine if a sector is unprotected in the system by writing the autoselect command and A6 is set at V_{IH}. Performing a read operation at address location XXX2H, where the higher order addresses (A18, A17, and A16) define a particular sector address, will produce 00H at data outputs (D0 - D7) for an unprotected sector.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally a desired system design practice.

The device contains an autoselect operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register.

Following command write, scanning the sector addresses on A16, A17, & A18 while A6, A1 & A0 = 0, 1, 0 will produce a logical "1" at device output D0 for a protected sector.

To terminate the operation, it is necessary to write the read/reset command sequence into the register.

Byte Programming

The device is programmed on a byte-by-byte basis. Programming is a four bus cycle operation. There are two "unlock" write cycle. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CS}$, whichever happens later, while the data are latched on the rising edge of $\overline{WE}$ or $\overline{CS}$ whichever happens first. The rising edge of $\overline{WE}$ or $\overline{CS}$ begins programming. Upon executing the Embedded Program Algorithm Command sequence the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin. The automatic programming operation is completed when the data on D7 is equivalent to data written to this bit (see Write Operations Status) at which time the device returns to the read mode and addresses are no longer latched. $\overline{Data}$ Polling must be performed at the memory location which is being programmed.

Programming is allowed in any address sequence and across sector boundaries.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock"write cycles. These are followed by writing the "Set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (data) is latched on the rising edge of $\overline{WE}$. A time-out of 80µs from the rising edge of the last sector erase command will initiate the sector erase command(s).

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 80µs, otherwise the command will not be accepted. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be-enabled after the last Sector Erase command is written. A time-out of 80µs from the rising edge of the last $\overline{WE}$ will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{WE}$ occurs within the 80us time-out window the timer is reset. Any command other than Sector Erase or Erase Suspend during this period and afterwards will reset the device to read mode, ignoring the previous command string. Resetting the device after it has begun execution will result in the data of the operated sectors being undefined. In that case, restart the erase on those sectors and allow them to complete. Loading the sector erase buffer may be done in any sequence and with any number of sectors.

Sector erase doesn't require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The automatic sector erase begins after the 100µs time-out from the rising edge of the $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on D7 is "1" (see Written Operation Status Section) at which time the device returns to read mode. Data polling must be preformed at an address within any of the sectors being erased.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase doesn't require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The systems is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on D7 is "1" (See Written Operation Section) at which time the device returns to read the mode.

Erase Suspend

Erase suspend allows the user to interrupt a Sector Erase operation and then perform data reads or programs to a sector not being erased. This command is only applicable during the Sector Erase operation which includes the time-out period for sector erase. The Erase Suspend command will be ignored if written during Chip Erase operation or Embedded Program Algorithm. Writing the Erase Suspend command during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Any other command written during the Erase Suspend mode will be ignored except the Erase Resume command. Writing the Erase Resume command resumes the erase operation. The addresses are "don't-cares" when writing the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of 15µs to suspend the erase operation. When the device has entered the erase-suspend mode, D7 bit will be a logic '1', and D6 will stop toggling. The user must use the address of the erasing sector for reading D6 and D7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the device defaults to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspend sector while the device is in the erase-suspend-read mode will cause D2 to toggle.

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Byte Program. This program mode is known as the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular Byte Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-program mode will cause D2 to toggle. The end of the erase-suspend-program operation is detected by $\overline{\text{Data}}$ Polling of D7, or by the Toggle bit (D6) which is the same as the regular Byte Program operation. Note that D7 must be read from the byte program address while D6 can be read from any address.

To resume the operation of Sector Erase, the Resume command should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

WRITE OPERATIONS STATUS

	Status		**D7**	**D6**	**D5**	**D3**
In Progress	Byte Programming in Embedded Algorithm		$\overline{\text{D7}}$	Toggle	0	0
	Embedded Erase Algorithm		0	Toggle	0	1
	Erase Suspended Mode	Erase Suspended Sector	1	No Tog	0	1
		Non-Erase Suspended Sector	Data	Data	Data	Data
Exceeded Time Limits	Byte-Programming in Embedded Algorithm		$\overline{\text{D7}}$	Toggle	1	0
	Embedded Erase Algorithm		0	Toggle	1	1
	Program in Erase Suspended Mode		$\overline{\text{D7}}$	Toggle	1	1

Operating Modes

The following modes are used to control the device.

OPERATION	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	I /O
Read(1)	L	L	H	A0	A1	A6	A9	D_{OUT}
Standby	H	X	X	X	X	X	X	High Z
Output Disable	L	H	H	X	X	X	X	High Z
Write	L	H	L	A0	A1	A6	A9	Din
Verify Sector Protect	L	L	H	L	H	L	V_{ID}	Code
Auto-Select Device Unprotected Code	L	L	H	H	H	L	V_{ID}	Code

1) L=V_{IL}, H=$V_{IH,}$ X=Don't Care

NOTE: 1) $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL} , $\overline{OE}$ at V_{IH} initiates write operation.

D7 $\overline{Data}$ Polling

The MFM8516 features $\overline{Data}$ Polling as a method to indicate to the host system that the Embedded Algorithms are in progress or completed. During the Embedded Programming Algorithm, an attempt to read the device will produce complement data of the data last written to D7. Upon completion of the Embedded Programming Algorithm an attempt to read the device will produce the true data last written to D7. During the Embedded Erase Algorithm, During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the D7 output.

For chip erase, the $\overline{Data}$ Polling is valid after the rising edge of the six $\overline{WE}$ pulse in the six write pulse sequence. For sector erase, the $\overline{Data}$ Polling is valid after the last rising edge of the sector erase $\overline{WE}$ pulse. $\overline{Data}$ Polling must be performed at sector address within any of the sectors being erased or not a protected sector. Otherwise, the status may not be valid. Once the Embedded Algorithm operation is close to being completed, the device data pins (D7) may change asynchronously while $\overline{OE}$ is asserted low. This means that the device is driving status information on D7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the D7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operation and D7 has a valid data, the data outputs on D0-D6 may still be invalid. The valid data on D0-D7 will be read on the successive read attempts.

The $\overline{Data}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time-out.

D6 Toggle Bit

The MFM8516 also features the "toggle bit" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read data from the device will result in D6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, D6 will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle bit is valid after the rising edge of the forth $\overline{WE}$ pulse in the four write pulse sequence. For chip erase, the Toggle bit is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erare $\overline{WE}$ pulse. The Toggle Bit is active during the sector time-out.

D5 Exceeding Time Limits

D5 will indicate if the program or erase time has exceeded the specified limits. Under these conditions D5 will produce "1", indicating the program or erase cycle was not successfully completed . $\overline{Data}$ Polling is the only operating function of the device under this condition. The $\overline{CS}$ circuit will partially power down the device under these conditions (to approximately 2mA). The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions .

If this failure occurs during sector erase operations, it specifies that a particular sector is bad and may not be re-used. The device must be reset to use other sectors. Write the reset command sequence and execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this failure occurs during chip erase operation , it specifies that the device chip or combination of sectors are bad.

If this failure occurs during the byte programming operation, it specifies that the entire sectors containing that byte is bad and may not be re-used.

The D5 failure condition may also appear if the user tries to program a non blank location without erasing. In this case the device locks out and never completes the embedded algorithm operation. Hence the system never reads a valid data on D7 and D6 never stops toggling. Once the device has exceeded timing limits, the D5 bit will indicate '1'

D3 Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. D3 will remain low until the time-out is complete. $\overline{Data}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{Data}$ Polling or the Toggle Bit indicates the device has been written with a valid erase command, D3 may be used to determine if the sector erase timer window is still open. If D3 is high the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{Data}$ Polling or Toggle Bit. If D3 is low , the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of D3 prior to and following each subsequent sector erase command. If D3 were high on the second status check, the command may not have been accepted.

DATA PROTECTION

The MFM8516 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the internal state machine in the Read mode. Also, with its controls register architecture , alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from Vcc power up and power down transitions or system noise.

Low V_{cc} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power up and power down, a write cycle is locked out for $V_{CC}<V_{LKO}$. When $V_{CC}<V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes will be ignored until the $V_{CC}>V_{LKO}$.

Write Pulse "Glitch" Protection

Noise pulses of less than 5ns (typical) on $\overline{OE}$, $\overline{CS}$, $\overline{WE}$ will not initiate a write cycle

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE}=V_{IL}$, $\overline{CS}=V_{IH}$ or $\overline{WE}=V_{IH}$. To initiate a write cycle $\overline{CS}$ and $\overline{WE}$ must be logical zero while $\overline{OE}$ is a logical one.

Power Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CS} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

Sector Protect

Sectors of the MFM8516 may be hardware protected at the users factory. The protection circuitry will disable both program and erase functions for the protected sector(s). Requests to program or erase a protected sector will be ignored by the device.

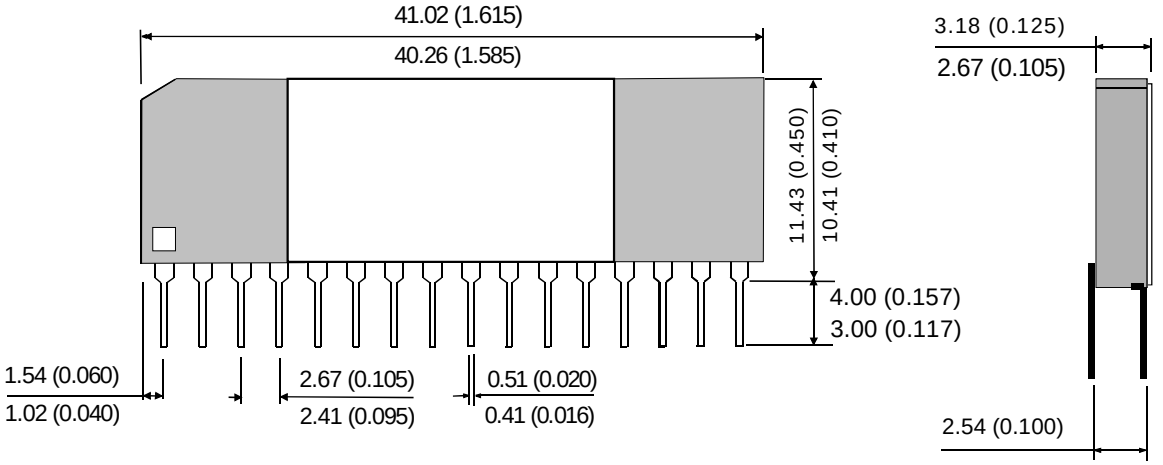
ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min	Typ	Max		
Sector Erase Time		1 (Note 1)	15	sec	Excludes 00H programming prior to erasure.
Chip Erase Time		8	120	sec	Excludes 00H programming prior to erasure.
Byte Programming Time		7 (Note 1)	1000	µs	Excludes System-level overhead.
Chip Programming Time		3.6 (Note 1)	25 (Note 2)	sec	Excludes system-level overhead.

Notes: (1) 25^{O}C, 5V V_{CC}, 10,000 cycles.
(2) The Embedded Algorithms allow for 2.5ms byte program time.

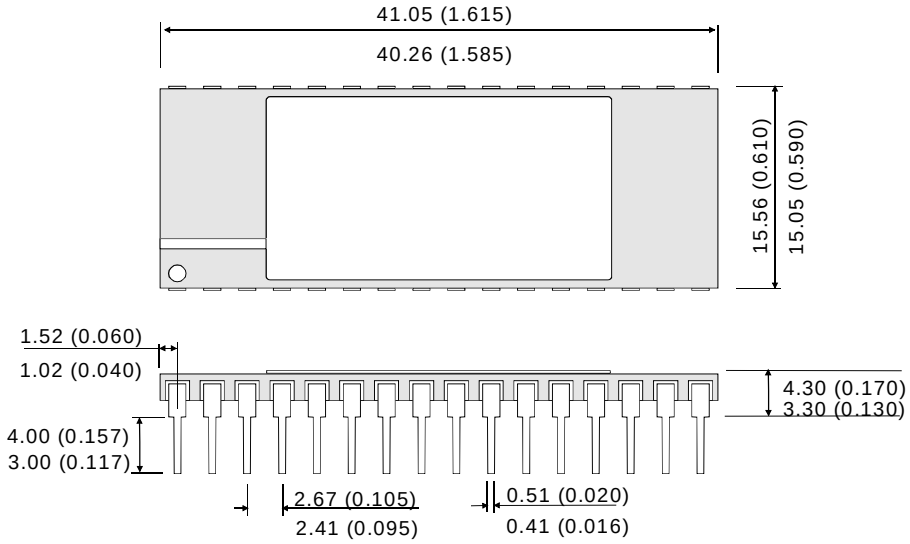
PACKAGE DETAILS

32 pin Ceramic Vertical in Line - 'V' Package



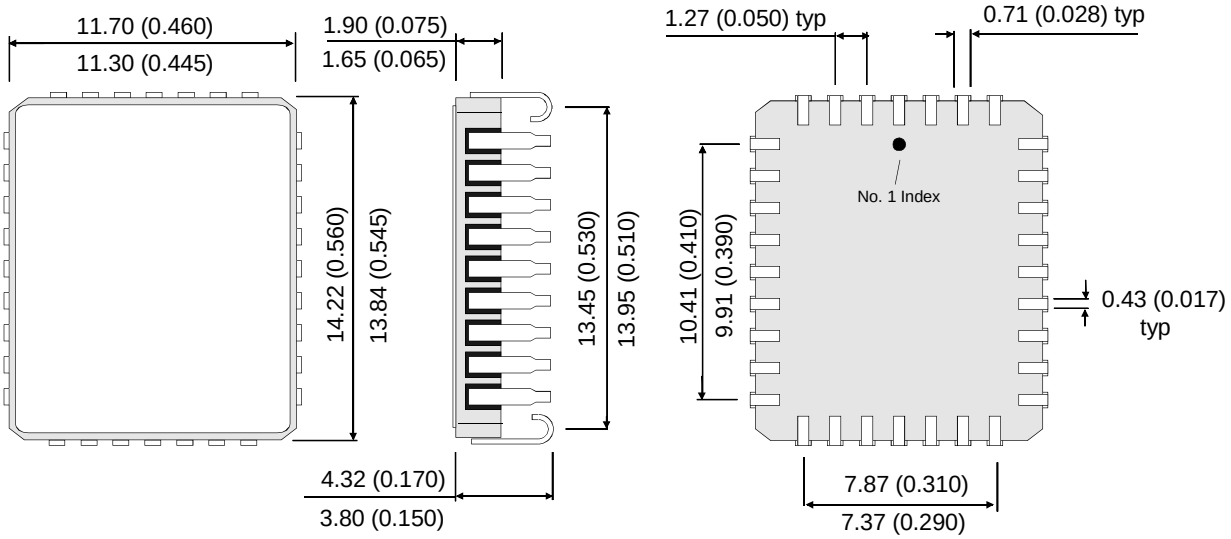
Minimum order product - Refer to factory

32 pin 0.6" Dual-In-Line (DIL) - 'S' Package

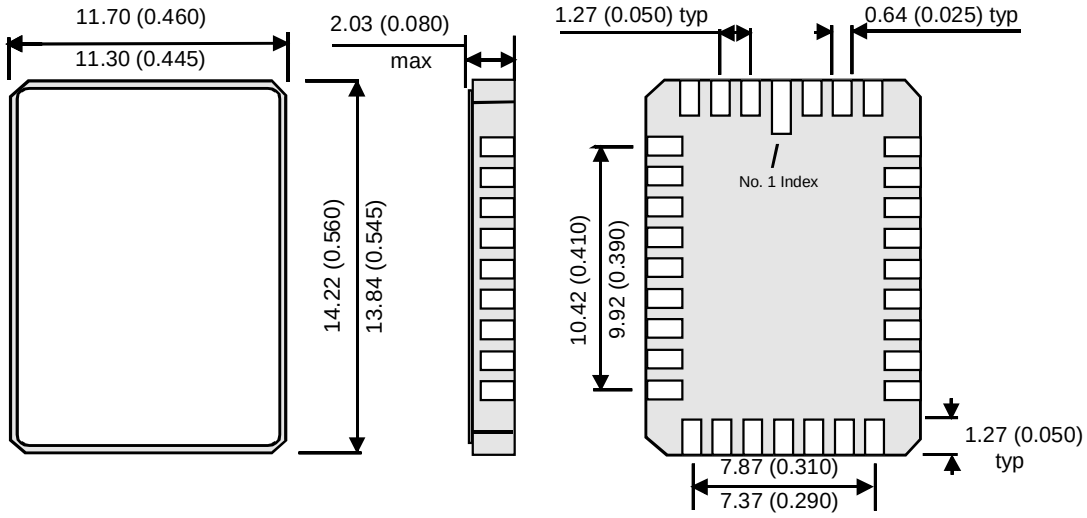


PACKAGE DETAILS

32 Pin J-Leaded Chip Carrier (JLCC) - 'J' Package



32 Pad Leadless Chip Carrier (LCC) - 'W' Package



Minimum order product - Refer to factory

SCREENING

Military Screening Procedure

Component Screening Flow for high reliability product using methods from 5004.

MB COMPONENT SCREENING FLOW

SCREEN	*TEST METHOD*	*LEVEL*
Mechanical		
Temperature cycle	1010 Condition C (10 Cycles,-65˚C to +150˚C)	100%
Constant acceleration	2001 Condition E (Y, only) (30,000g)	100%
Pre-Burn-in electrical	Per applicable device specifications at T_A=+25˚C	100%
Burn-in	Method 1015,Condition D,T_A=+125˚C,160hrs min	100%
Endurance Write Cycle endurance and Data Retention performance	As per internal specification	
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25˚C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25˚C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25˚C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at post-burn-in at T_A=+25˚C	5%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
External Visual	2009 Per vendor or customer specification	100%

ORDERING INFORMATION

MFM8516JMB - 90E

Write Cycle Endurance	E	=	100,000 cycles (min)
	Blank	=	10,000 cycles (min)
Speed	70	=	70 ns
	90	=	90 ns
	12	=	120 ns
	15	=	150 ns
Temp. range/screening	Blank	=	Commercial Temperature
	I	=	Industrial Temperature
	M	=	Military Temperature
	MB	=	Processed in accordance with MIL-STD-883
Packages	V	=	32 pin Ceramic Vertical in Line
	S	=	32 pin Ceramic Dual In-line
	J	=	32 pad Ceramic JLCC
	W	=	32 pad Ceramic LCC
Organisation	8516	=	512Kx 8 Flash Memory
Technology	F	=	FLASH Memory