1024-Bit EEPROM

Electrically erasable programmable read-only memory (EEPROM) in N-channel floating-gate technology with a capacity of 128 words, 8 bits each.

The MDA 2062 is intended for use as a reprogrammable non-volatile memory in conjunction with the CCU 2030/2050/2070 series Central Control Units of the DIGIT 2000 Digital TV System, the MAA 4000 Remote-Control and PLL-Tuning Microcomputers for TV receivers or the SAA 1280, SAA 1290 and SAA 1293 Remote-Control and Tuning ICs. It serves for storing the tuning information as well as several analog settings, further alignment information given in the factory when producing the TV set. The stored information remains stored even with the supply voltages switched off. Reading and programming operations are executed via the IM bus (see section 7.). Input and output signals are TTL level. An address option input provides the possibility to operate two memories in parallel, to obtain a total storage capacity of 2048 bits.

1. Functional Description

1.1. Memory Operation

The internal memory address space ranges from address 128 to address 255. Addresses 4 and 14 provide special functions.

To read a stored data word, the desired memory address has to be entered to the memory address register first. This is done by serially entering the IM bus address 128 (optionally 132) (during Ident = L), followed by the memory address (during Ident = H) in a single IM bus operation.

With the memory address register set, the memory data may be read. This, in turn, is done by entering the IM bus address 129 (optionally 133) to the device (during Ident = L). Immediately after this, within the same IM bus operation (during Ident = H) the open-drain Data output will conduct to serially transmit the respective 8-bit memory data.

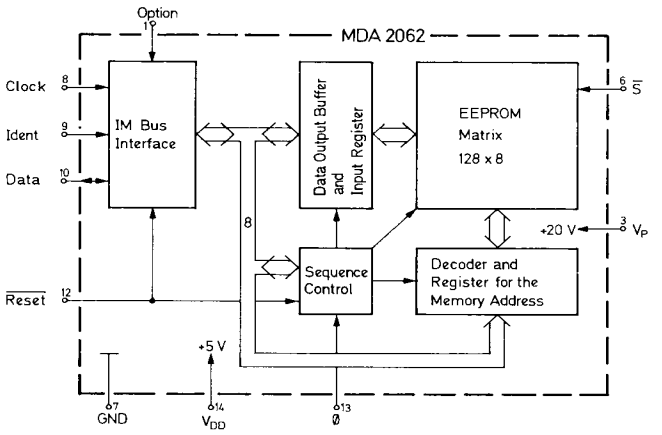

Fig. 1: Block diagram of the MDA 2062 EEPROM

Reprogramming a memory location is done in two steps, a) and b), that are identical except for the data word to be entered. Step a) resets all bits to "1", and step b) programs the desired data into the selected memory location.

a) First, the desired memory address is entered in the way described above. Second, the actual programming is initiated by serially entering the IM bus address 131 (optionally 135) followed by the data word to be stored, which is 255 for step a). The device will now internally time its programming sequence of approx. 16 periods of the 1 kHz memory clock. During this "busy" time all inputs are blocked from affecting the programming except for the $\overline{\text{Reset}}$ input. A $\overline{\text{Reset}}$ = L signal will immediately cancel any programming operation as well as any bus operation in progress.

The busy state may be interrogated by reading bit 1 of address location 14. A high level of this "busy-bit" indicates that programming is still under way. The IM bus operation for entering address 14 should always directly precede reading the busy-bit.

Reading any other address location during the busy state will produce erroneous data at the Data output. An address change operation during the busy state will not change the memory address register content. The intended start of another programming operation during the busy time will not be executed.

b) After time-out, normal operation may be resumed, e. g. by performing the second step of a programming sequence, i. e. by programming the desired 8-bit data word into the respective memory address location. This is done by restoring the proper memory address first, if necessary, and then by serially entering the IM bus address 131 (optionally 135) followed by the desired 8-bit data word. The device will again time its own programming sequence as described under a). After time-out the new data may be verified.

1.2. Redundancy

The MDA 2062 EEPROM contains circuitry that allows to replace up to two rows of the memory matrix, each containing 4 bytes of memory, by redundant rows SR 1 and SR 2. This substitution can be done in the field, by the user.

To prepare for activation of SR 1, memory address location 192 must contain the 5 LSB of the memory address containing the defect, which identifies the row to be substituted. Furthermore, bit 5 has to be set to "0", which identifies the data to be redundancy relevant (see Fig. 2).

To prepare for activation of SR 2, memory address location 160 must contain the equivalent data.

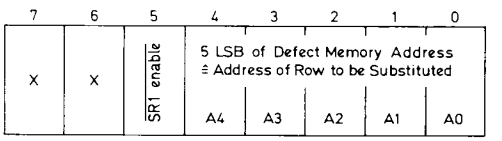

Fig. 2: Activation of redundant row SR 1

The activation itself of the redundant rows is done by reading the content of memory address locations 192 and 160. This transfers the repair information stored nonvolatilely in the memory array to volatile repair registers.

It is important to note that the repair registers are cleared (bit 5 set to "1") by any $\overline{\text{Reset}}$ = L signal. Thus, any LH transition of the $\overline{\text{Reset}}$ signal must immediately be followed by reading the memory address locations 192 and 160, which restores the repair information to the repair registers.

SR 2 may be substituted by SR 1, whereas SR 1 cannot be substituted. As well, row 0 which contains the memory address locations 192 and 160 cannot be substituted.

SR 1 and SR 2 are part of the memory matrix portion that is not protectable by the $\overline{S}$ signal. Memory address locations 192 and 160 are part of the protectable portion.

1.3. Testing

The MDA 2062 EEPROM contains circuitry designed to facilitate testing of the various functions. By programming data into address location 4, the device is switched to one or more of a number of test modes. A detailed description is given in section 6.

1.4. Protected Matrix

The programming matrix contains a protectable portion. Addresses 128 to 134, 160 to 166, 192 to 198 and 224 to 230 can only be programmed if the "Safe" input $\overline{S}$ (pin 6) is at high potential. In that way, this portion of the memory is protected against inadvertent reprogramming even if such false informations were received via the IM bus. The second part of the programming matrix is not protected.

1.5. Shipment

Parts are shipped with all bits set to "1", except for addresses 192 and 160 which may contain repair information. The content of memory address locations 192 and 160, if different from 255, should not be altered, as this will result in defective rows appearing within the memory address space.

2. Outline Dimensions and Pin Connections

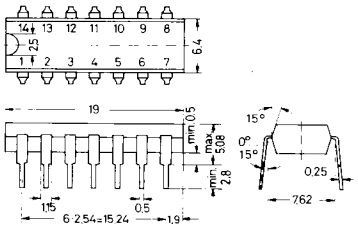

Fig. 3:
MDA 2062 in 14-pin Dil Plastic Package TO-116, 20 A 14 according to DIN 41870

Weight approx. 1.2 g Dimensions in mm

Pin Conncetions

1	Option Input
2	NC
3	Programming Voltage V_P
4	NC
5	NC
6	Safe Input $\overline{S}$
7	Ground, 0
8	IM Bus Clock Input
9	IM Bus Ident Input
10	IM Bus Data Input/Output
11	NC
12	$\overline{\text{Reset}}$ Input
13	Memory Clock Input
14	Supply Voltage V_{DD}

3. Electrical Characteristics

All voltages are referred to pin 7.

Absolute Maximum Ratings

	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.5 to +6	V
Programming Voltage	V_P	(V_{DD} − 0.8 V) to +22 V	—
V_P Supply Current	I_P	7	mA
Input Voltages	V_I	−0.3 V to V_{DD}	—
Output Current	I_{10}	5	mA
Ambient Operating Temperature Range	T_A	0 to +65	°C
Storage Temperature Range	T_S	−40 to +125*	°C

* Stored data may be affected by T_S above +85 °C.

Recommended Operating Conditions

		Symbol	Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	4.75	5.0	5.25	V
Programming Voltage when non-programming		V_P	(V_{DD} −0.7 V)	—	21	V
when programming		V_P	19	20	21	V
Programming Current Limit (see Fig. 4)		I_{Pmax}	—	—	5	mA
Input Voltages Pins 1, 6, 8, 9, 10 and 13		V_{IL}	—	—	0.8	V
		V_{IH}	2.4	—	—	V
Pin 12		V_{IL}	—	—	1.3	V
		V_{IH}	2.4	—	—	V
Memory Clock Frequency		f_{13}	0.9	1.0	1.1	kHz
Memory Clock Input Ratio		R_{13}	0.2	—	99.8	%
V_{DD} Rise Time	see Fig. 4	t_1	—	—	500	ms
V_P Rise Time		t_2	0.01	—	500	ms
$V_P - V_{DD}$ Delay Time		t_3	—	—	50	ms
$V_{DD} - V_{12}$ Delay Time		t_4	0	—	—	ms
V_{DD} Fall Time		t_5	—	—	500	ms
V_P Fall Time		t_6	0.01	—	500	ms
$V_{12} - V_{DD}$ Delay Time		t_7	0	—	—	ms
$V_{DD} - V_P$ Delay Time		t_8	—	—	50	ms

Recommended Operating Conditions, continued

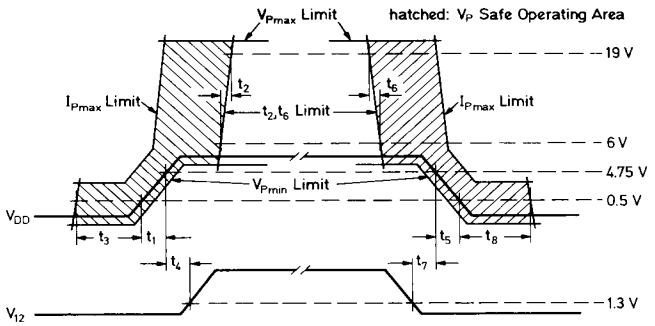

Fig. 4: Power on/off timing

Characteristics at $V_{DD} = 5$ V, $V_P = 20$ V, $f_{13} = 1$ kHz, $T_A = 25$ °C

	Symbol	Min.	Typ.	Max.	Unit
Current Consumption Pin 14	I_{DD}	10	–	40	mA
Pin 3, Programming Mode	I_P	0.3	–	2	mA
Non-Programming Mode	I_P	10	–	40	µA
Input Leakage Current Pins 8, 9, 12 and 13 at $V_{IH} = 5$ V	$-I_{IH}$	–	–	10	µA
IM Bus High Level Output Leakage Current at $V_{OH} = 5$ V, Pin 10	$-I_{OH}$	–	–	10	µA
IM Bus Low Level Output Voltage at $I_{OL} = 3$ mA, Pin 10	V_{OL}	–	–	0.4	V
Input Internal Pull-Down Current at $V_{IH} = 5$ V, Pins 1 and 6	I_{IH}	35	–	260	µA
Erase or Write Time at $f_{13} = 1$ kHz	t_P	15.9	–	17.1	ms

4. Inner Configuration of the Connection Pins

The following figures schematically show the circuitry at the various pins. The integrated protection structures are not shown. The letter "E" means enhancement, the letter "D" depletion.

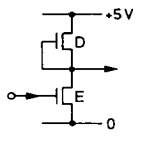

Fig. 6:
Pins 8, 9, 12 and 13, Inputs

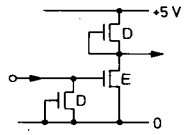

Fig. 5:
Pins 1 and 6, Inputs

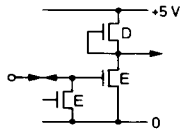

Fig. 7:
Pin 10, Input/Output

5. Description of the Connections and the Signals

Pin 1 – Option Input
Fig. 5 shows the internal configuration of this input. With Pin 1 at ground potential (low) or floating, the MDA 2062 reacts upon the IM bus addresses 128, 129 and 131. With pin 1 continuously at V_{DD} potential (high), the MDA 2062 reacts upon this IM bus addresses 132, 133 and 135 (see Fig. 8). In this way, parallel operation of two MDA 2062 is permitted, to obtain 2048 bits of non-volatile storage directly accessible via the IM bus. Pin 1 is internally tied to ground via a transistor equivalent to a 40 kΩ resistor.

Pins 2, 4, 5 and 11 – NC
These pins are not connected internally.

Pin 3 – Programming Voltage V_P
A programming voltage of + 20 V (± 5 %) is required. The current consumption during programming is approximately 1 mA. During non-programming operations, pin 3 may be held at any level between (V_{DD} – 0.7 V) and + 21 V. It may also be left floating. The MDA 2062 EEPROM **must not** be inserted or removed from a socket with $V_P \geq 6$ V. During power on/off sequences, current from the V_P supply should be limited to $I_{P\,max} = 5$ mA.

Pin 6 – Safe Input $\overline{S}$
Fig. 5 shows the internal configuration of this input. Normally, with pin 6 at ground potential (low), one portion of the programming matrix is protected so that this part of the memory cannot be reprogrammed inadvertently. Only when pin 6 receives high potential continuously, the protected portion of the memory matrix can be programmed. Pin 6 is internally tied to ground via a transistor equivalent to a 40 kΩ resistor.

Pin 7 – Ground, 0
This pin must be connected to the negative of the supplies.

Pins 8 to 10 – IM Bus Connections
These pins serve to connect the MDA 2062 EEPROM to the IM bus (see section 7.), via which it communicates with the CCU 2030/2050/2070 or MAA 4030 series µC or the SAA 1280/SAA 1290/SAA 1293. Pins 8 (IM Bus Clock Input) and 9 (IM Bus Ident Input) are inputs as shown in Fig. 6 and pin 10 (IM Bus Data) is an input/output as shown in Fig. 7. The signal diagram for the IM bus is illustrated in Figs. 8 and 11. The required addresses which the MDA 2062 EEPROM receives from the microcomputer, are also shown in Fig. 8.

Pin 12 – $\overline{\text{Reset}}$ Input
This input has a configuration as shown in Fig. 6. Via this input, the MDA 2062, together with the other circuits belonging to the system, receives the $\overline{\text{Reset}}$ signal which is derived from V_{DD} via an external RC circuit. A low level is required during power-up and power-down procedures. Low level at pin 12 (max. 1.3 V) cancels a programming procedure and an IM bus operation in progress. The memory address register is not, the repair register is erased. During operation, pin 12 requires high level (min. 2.4 V).

Pin 13 – Memory Clock Input
Via this input (Fig. 6) the MDA 2062 receives a 1 kHz clock signal from pin 3 of the CCU 2030, CCU 2050, CCU 2070 or MAA 4030 microcomputer or the SAA 1280/SAA 1290/SAA 1293.

Pin 14 – Supply Voltage V_{DD}
The supply voltage required is + 5 V (± 5 %), and the current consumption in active operation is approx. 30 mA.

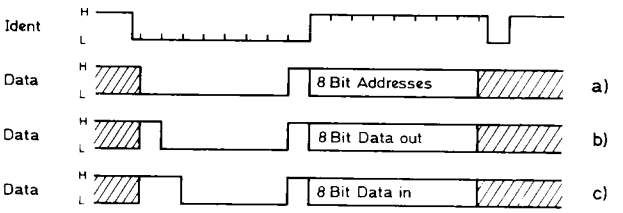

Fig. 8: Signal diagram for the IM bus

	Pin 1 low	Pin 1 high	
a) enter memory address:	128	132	followed by address
b) reading:	129	133	followed by data out
c) programming:	131	135	followed by data in

6. Test Functions

This description of the test byte is not part of the specification. It contains no information necessary for normal (intended) use of the MDA 2062 memory. It is only intended as a description of the various functions of the test byte that are designed for factory use, but it does not specify such properties. The description is subject to change.

Address location 4 contains a test byte which governs test mode operation of the MDA 2062. The test byte is set by performing the IM bus operation for entering address 4, followed by an IM bus programming operation with the desired test data word. The test byte is valid during all following IM bus operations until changed or set to 0 by a $\overline{\text{Reset}}$ = L signal. The test byte shall not be changed during the busy time of a programming operation. Fig. 9 shows the bit arrangement of the test byte. Set bit 5 for activation of the test byte!

Block Programming
Three block program modes can be activated by the test byte, in conjunction with the memory address loaded into the memory address register:

	memory address 7 6 5 4 3 2 1 0	
1) all bytes are selected (including 8 bytes in redundant rows):	1 x x x x x 0 x	(e. g. 128)
2) all even-numbered bytes are selected (redundant bytes are not predetermined, they have to be defined as even bytes):	1 x x x x x 1 0	(e. g. 130)
3) all odd-numbered bytes are selected (redundant bytes are not predetermined):	1 x x x x x 1 1	(e. g. 131)

7	6	5	4	3	2	1	0
Block programming enable	Read reference shift −0.3 V	Test Byte enable	Read reference shift −0.6 V	Ramp disable	Read reference shift +0.3 V	Redundancy disable	Read reference shift +0.6 V

Fig. 9: Functions of the 8 bits in the test byte

Thus, programming all selected bytes with the same desired data is done within one programming sequence. The complete sequence is:

Enter Address 4
Program Test byte (e. g. 160)
Enter Address 128, 130 or 131
Program Data

A checkerboard pattern is programmed with two programming operations after loading the test byte:

Enter Address 130
Program Data 85
Enter Address 131
Program Data 170

Read Reference Shifting
During read operations the memory cell threshold voltage is compared with a reference voltage. The comparator output then produces the logic one level for a cell threshold higher than the reference and the logic zero level for a cell threshold lower than the reference.

The test byte provides means to shift the reference voltage in positive or negative direction in three steps: ±0.3 V, ± 0.6 V and ± 0.9 V.

During a read operation a positive-shifted reference voltage establishes a margin test for logic ones, whereas a negative-shifted reference does so for logic zeroes. This margin test is performed digitally by IM bus operations only, without the need to switch analog power supplies.

	7 6 5 4 3 2 1 0
+ 0.9 V:	x 0 1 0 x 1 x 1
+ 0.6 V:	x 0 1 0 x 0 x 1
+ 0.3 V:	x 0 1 0 x 1 x 0
− 0.3 V:	x 1 1 0 x 0 x 0
− 0.6 V:	x 0 1 1 x 0 x 0
− 0.9 V:	x 1 1 1 x 0 x 0

Redundancy Disable
With bit one of the test byte set, the redundant rows can be accessed neither during byte program operations nor during any read operation, even if the redundancy registers are properly loaded. This test byte function has no effect on block programming operations.

Ramp Disable
The MDA 2062 contains circuitry to shape the internal program supply voltage to be a ramp function during programming operations. This feature is considered to be essential to a high erase/write endurance of the memory cells.

Bit 3 of the test byte disables this ramp function so that the internal program supply, according to the timing diagram Fig. 10, is immediately disconnected from the V_{DD} supply and connected to the V_P supply at the 4th falling edge of the 1 kHz memory clock, and is immediately disconnected from the V_P supply and re-connected to the V_{DD} supply at the 14th falling edge of the 1 kHz clock after the last rising Ident signal edge of the IM bus operation starting the program cycle. By this feature other than the built-in ramp function (approx. 100 µs/V) can be applied via the V_P supply pin.

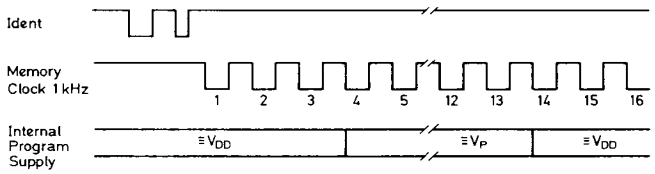

Fig. 10: Ramp disable timing diagram

7. Description of the IM Bus

The INTERMETALL Bus (IM Bus for short) has been designed to control the DIGIT 2000 ICs by the CCU Central Control Unit. Via this bus the CCU can write data to the ICs or read data from them. This means the CCU acts as a master whereas all controlled ICs are slaves.

The IM Bus consists of three lines for the signals Ident (ID), Clock (CL) and Data (D). The clock frequency range is 50 Hz to 170 kHz. Ident and clock are unidirectional from the CCU to the slave ICs, Data is bidirectional. Bidirectionality is achieved by using open-drain outputs with On-resistances of 150 Ω maximum. The 2.5 kΩ pull-up resistor common to all outputs is incorporated in the CCU.

The timing of a complete IM Bus transaction is shown in Fig. 11 and Table 1. In the non-operative state the signals of all three bus lines are High. To start a transaction the CCU sets the ID signal to Low level, indicating an address transmission, and sets the CL signal to Low level as well to switch the first bit on the Data line. Thereafter eight ad-

dress bits are transmitted beginning with the LSB. Data takeover in the slave ICs occurs at the positive edge of the clock signal. At the end of the address byte the ID signal goes High, initiating the address comparison in the slave circuits. In the addressed slave the IM bus interface switches over to Data read or write, because these functions are correlated to the address.

Also controlled by the address the CCU now transmits eight or sixteen clock pulses, and accordingly one or two bytes of data are written into the addressed IC or read out from it, beginning with the LSB.

The completion of the bus transaction is signalled by a short Low-state pulse of the ID signal. This initiates the storing of the transferred data.

It is permissible to interrupt a bus transaction for up to 10 ms.

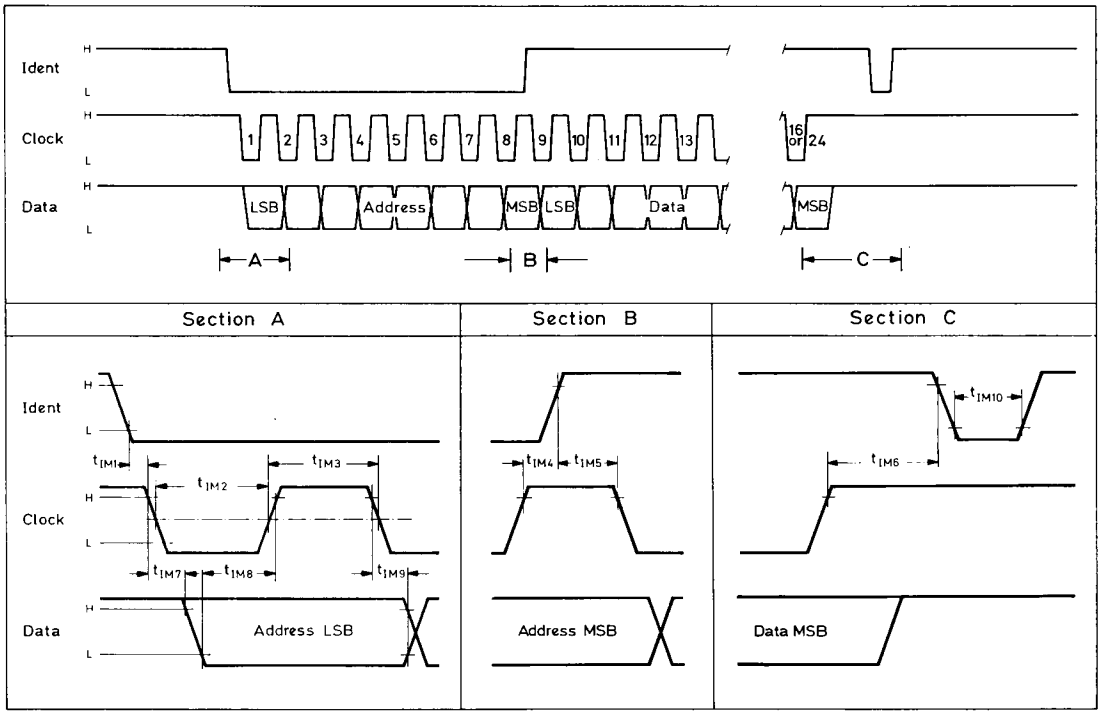

Fig. 11: Waveforms of the IM bus signals

Table 1: Timing of the IM bus signals

Time	t_{IM1}	t_{IM2}	t_{IM3}	t_{IM4}	t_{IM5}	t_{IM6}	t_{IM7}	t_{IM8}	t_{IM9}	t_{IM10}
Min. µs	0	3.0	3.0	0	1.5	6.0	0	0	0	3.0

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