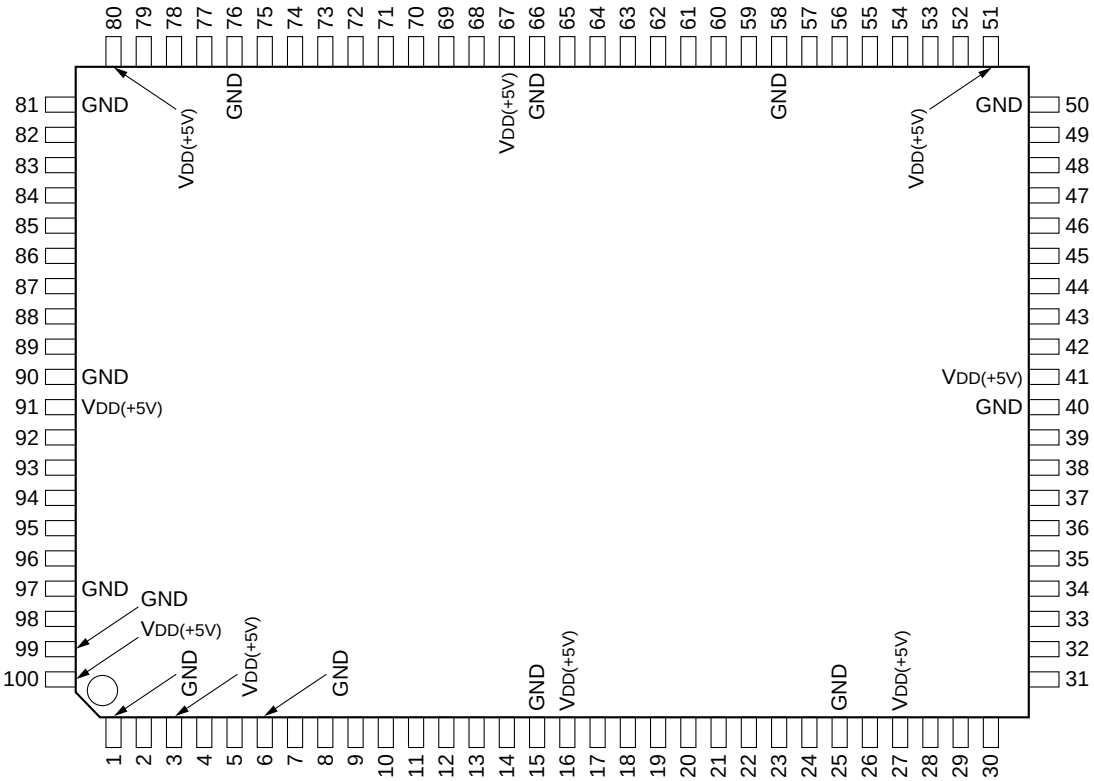
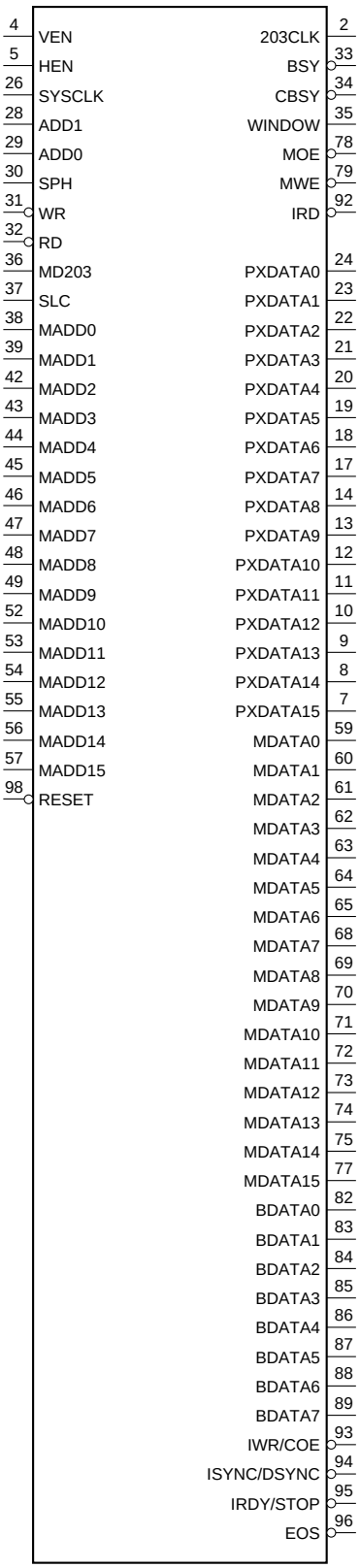
****

C-MOS RASTER/BLOCK CONVERTER

–TOP VIEW–



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	GND	26	I	SYSCLK	51	—	V_{DD}	76	—	GND
2	O	203CLK	27	—	V_{DD}	52	I	MADD10	77	I/O	MDATA15
3	—	V_{DD}	28	I	ADD1	53	I	MADD11	78	O	$\overline{\text{MOE}}$
4	I	VEN	29	I	ADD0	54	I	MADD12	79	O	$\overline{\text{MWE}}$
5	I	HEN	30	I	SPH	55	I	MADD13	80	—	V_{DD}
6	—	GND	31	I	$\overline{\text{WR}}$	56	I	MADD14	81	—	GND
7	I/O	PXDATA15	32	I	$\overline{\text{RD}}$	57	I	MADD15	82	I/O	BDATA0
8	I/O	PXDATA14	33	O	$\overline{\text{BSY}}$	58	—	GND	83	I/O	BDATA1
9	I/O	PXDATA13	34	O	$\overline{\text{CBSY}}$	59	I/O	MDATA0	84	I/O	BDATA2
10	I/O	PXDATA12	35	O	WINDOW	60	I/O	MDATA1	85	I/O	BDATA3
11	I/O	PXDATA11	36	I	MD203	61	I/O	MDATA2	86	I/O	BDATA4
12	I/O	PXDATA10	37	I	SLC	62	I/O	MDATA3	87	I/O	BDATA5
13	I/O	PXDATA9	38	I	MADD0	63	I/O	MDATA4	88	I/O	BDATA6
14	I/O	PXDATA8	39	I	MADD1	64	I/O	MDATA5	89	I/O	BDATA7
15	—	GND	40	—	GND	65	I/O	MDATA6	90	—	GND
16	—	V_{DD}	41	—	V_{DD}	66	—	GND	91	—	V_{DD}
17	I/O	PXDATA7	42	I	MADD2	67	—	V_{DD}	92	O	$\overline{\text{IRD}}$
18	I/O	PXDATA6	43	I	MADD3	68	I/O	MDATA7	93	I/O	$\overline{\text{IWR}}$/$\overline{\text{COE}}$
19	I/O	PXDATA5	44	I	MADD4	69	I/O	MDATA8	94	I/O	$\overline{\text{ISYNC}}$/$\overline{\text{DSYNC}}$
20	I/O	PXDATA4	45	I	MADD5	70	I/O	MDATA9	95	I/O	$\overline{\text{IRDY}}$/$\overline{\text{STOP}}$
21	I/O	PXDATA3	46	I	MADD6	71	I/O	MDATA10	96	I/O	$\overline{\text{EOS}}$
22	I/O	PXDATA2	47	I	MADD7	72	I/O	MDATA11	97	—	GND
23	I/O	PXDATA1	48	I	MADD8	73	I/O	MDATA12	98	I	$\overline{\text{RESET}}$
24	I/O	PXDATA0	49	I	MADD9	74	I/O	MDATA13	99	—	GND
25	—	GND	50	—	GND	75	I/O	MDATA14	100	—	V_{DD}



INPUT

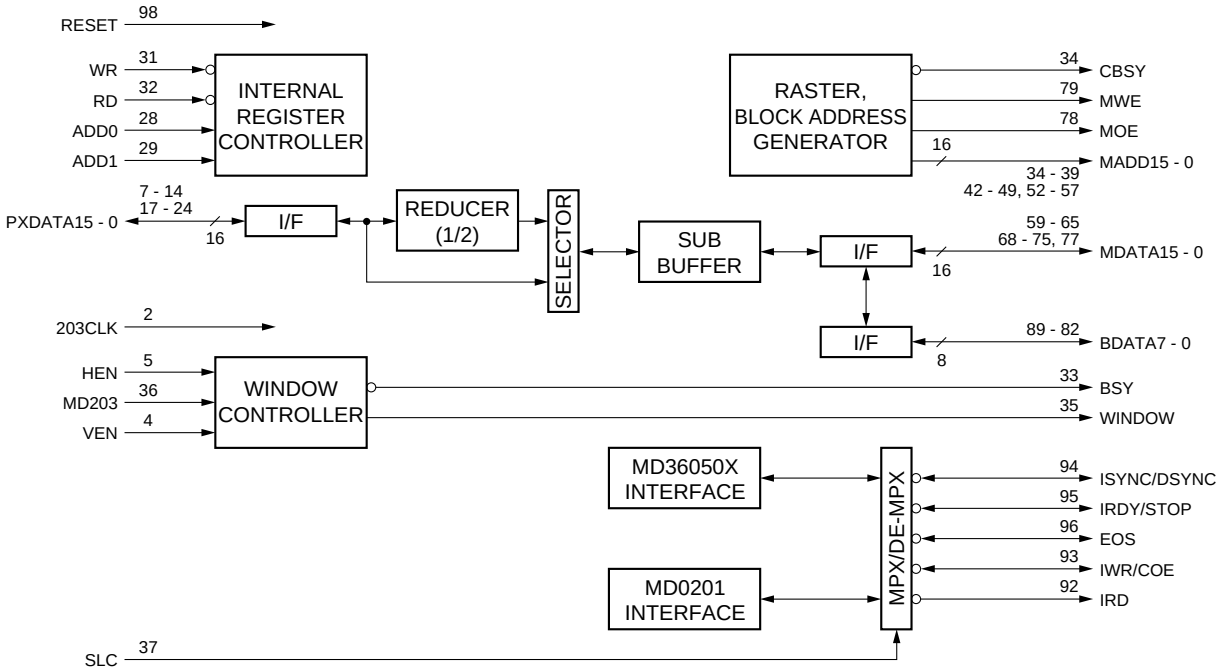
ADD1, ADD0	;	INTERNAL REGISTER SELECT ADDRESS
HEN	;	HORIZONTAL ENABLE
MADD15 - MADD0	;	SRAM 16-BIT ADDRESS
MD203	;	MD0203/MD0206 SELECT
$\overline{\text{RESET}}$	;	RESET
$\overline{\text{RD}}$	;	DATA READ
SLC	;	CODER SELECT
SPH	;	PIXEL/HOST SELECT
SYSCLK	;	SYSTEM CLOCK
VEN	;	VERTICAL ENABLE
$\overline{\text{WR}}$	;	DATA WRITE

OUTPUT

203CLK	;	CLOCK FOR MD0203
$\overline{\text{BSY}}$	;	BUSY
$\overline{\text{CBSY}}$	;	COMPRESS/DECOMPRESS BUSY
$\overline{\text{IRD}}$	;	(NOT IN USED)
$\overline{\text{MOE}}$	;	SRAM OUTPUT ENABLE
$\overline{\text{MWE}}$	;	SRAM WRITE ENABLE
WINDOW	;	DATA EXISTENCE

INPUT/OUTPUT

BDATA7 - BDATA0	;	8-BIT INTERFACE DATA
$\overline{\text{EOS}}$	;	END-OF-SCAN
$\overline{\text{IRDY}}/\overline{\text{STOP}}$	;	DATA ACCESS INHIBIT
$\overline{\text{ISYNC}}/\overline{\text{DSYNC}}$	;	CODER CONTROLLING BLOCK SYNC
$\overline{\text{IWR}}/\overline{\text{COE}}$	;	CODER BUS OUTPUT ENABLE
MDATA15 - MDATA0	;	SRAM 16-BIT DATA
PXDATA15 - PXDATA0	;	16-BIT PIXEL DATA


RESET
98
WR
31
RD
32
ADD0
28
ADD1
29
INTERNAL
REGISTER
CONTROLLER
RASTER,
BLOCK ADDRESS
GENERATOR
34
CBSY
79
MWE
78
MOE
16
MADD15 - 0
34 - 39
42 - 49, 52 - 57
7 - 14
17 - 24
PXDATA15 - 0
16
I/F
REDUCER
(1/2)
SELECTOR
SUB
BUFFER
I/F
59 - 65
68 - 75, 77
MDATA15 - 0
16
203CLK
2
I/F
89 - 82
BDATA7 - 0
8
HEN
5
MD203
36
VEN
4
WINDOW
CONTROLLER
33
BSY
35
WINDOW
MD36050X
INTERFACE
MPX/DE-MPX
94
ISYNC/DSYNC
95
IRDY/STOP
96
EOS
93
IWR/COE
92
IRD
MD0201
INTERFACE
SLC
37